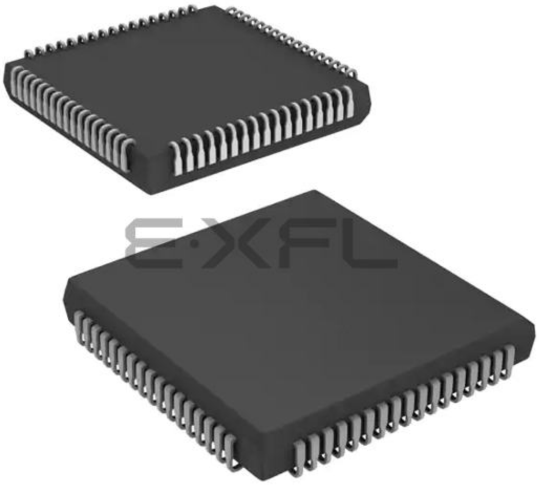
# Microchip Technology - A40MX04-1PLG68I Datasheet



## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 57 |
| Number of Gates | 6000 |
| Voltage - Supply | 3V ~ 3.6V, 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 68-LCC (J-Lead) |
| Supplier Device Package | 68-PLCC (24.23x24.23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-1plg68i |

- The Transient Current, page 13 is new (SAR 36930).
- Package names were revised according to standards established in *Package Mechanical Drawings* (SAR 34774)

## 1.7 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document

- In Table 20, page 23, the limits in VI were changed from -0.5 to VCCI + 0.5 to -0.5 to VCCA + 0.5

In Table 22, page 25, $V_{OH}$ was changed from 3.7 to 2.4 for the min in industrial and military. $V_{IH}$ had $V_{CCI}$ and that was changed to VCCA

## 1.8 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- The Ease of Integration, page 1 was updated
- The Temperature Grade Offerings, page 5 is new
- The Speed Grade Offerings, page 5 is new
- The General Description, page 6 was updated
- The MultiPlex I/O Modules, page 11 was updated
- The User Security, page 12 was updated
- Table 6, page 13 was updated
- The Power Dissipation, page 14 was updated.
- The Static Power Component, page 14 was updated
- The Equivalent Capacitance, page 15 was updated
- Figure 13, page 17 was updated
- Table 10, page 18 was updated.
- Figure 14, page 18 was updated.
- Table 11, page 19 was updated.

3. All outputs unloaded. All inputs = VCC/VCCI or GND

## 3.8 3.3 V Operating Conditions

The following table shows 3.3 V operating conditions.

***Table 16 •*** **Absolute Maximum Ratings for 40MX Devices***

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCC | DC Supply Voltage | –0.5 to +7.0 | V |
| VI | Input Voltage | –0.5 to VCC + 0.5 | V |
| VO | Output Voltage | –0.5 to VCC + 0.5 | V |
| $t_{STG}$ | Storage Temperature | –65 to + 150 | °C |

**Note:** *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

***Table 17 •*** **Absolute Maximum Ratings for 42MX Devices***

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCCI | DC Supply Voltage for I/Os | –0.5 to +7.0 | V |
| VCCA | DC Supply Voltage for Array | –0.5 to +7.0 | V |
| VI | Input Voltage | –0.5 to VCCI+0.5 | V |
| VO | Output Voltage | –0.5 to VCCI+0.5 | V |
| $t_{STG}$ | Storage Temperature | –65 to +150 | °C |

**Note:** *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

***Table 18 •*** **Recommended Operating Conditions**

| Parameter | Commercial | Industrial | Military | Units |
|---|---|---|---|---|
| Temperature Range* | 0 to +70 | –40 to +85 | –55 to +125 | °C |
| VCC (40MX) | 3.0 to 3.6 | 3.0 to 3.6 | 3.0 to 3.6 | V |
| VCCA (42MX) | 3.0 to 3.6 | 3.0 to 3.6 | 3.0 to 3.6 | V |
| VCCI (42MX) | 3.0 to 3.6 | 3.0 to 3.6 | 3.0 to 3.6 | V |

**Note:** *Ambient temperature ($T_A$) is used for commercial and industrial grades; case temperature ($T_C$) is used for military grades.

All the following tables show various specifications and operating conditions of 40MX and 42MX FPGAs.

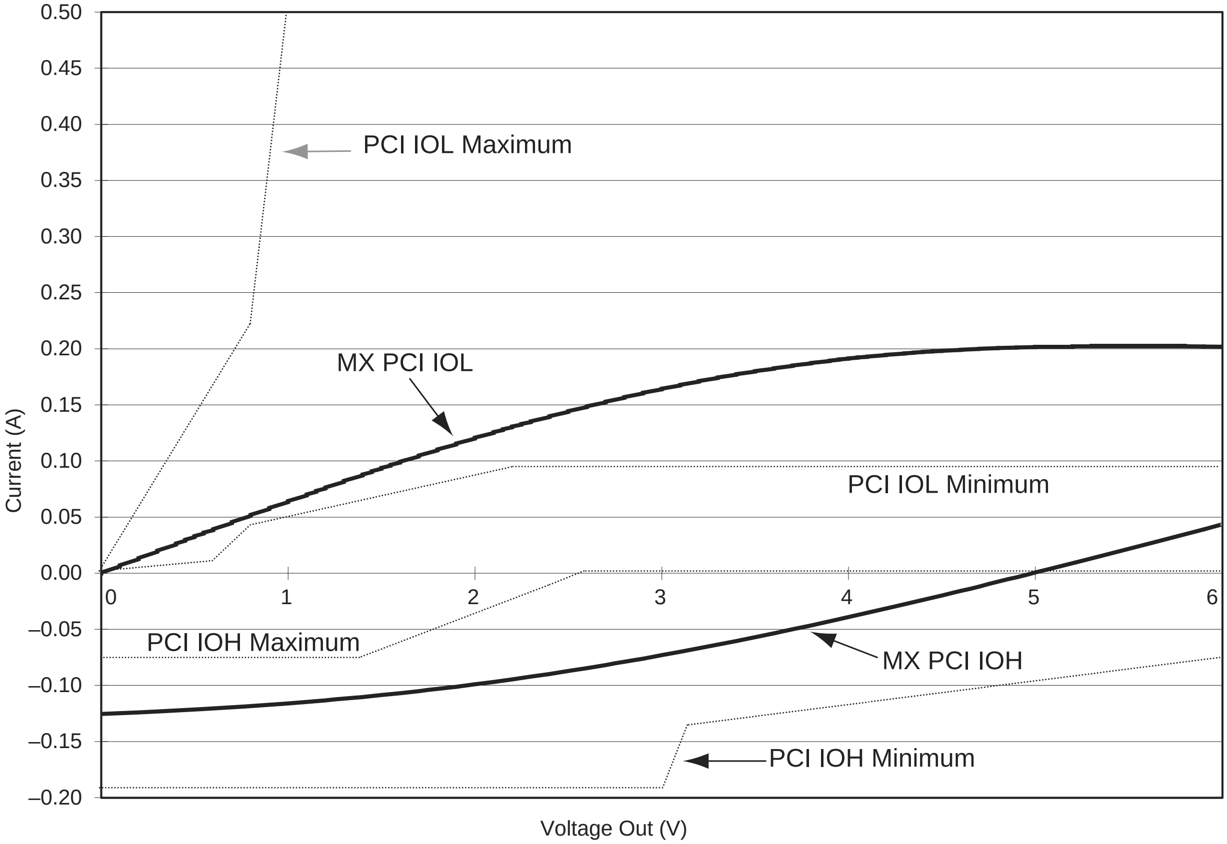
reliability. Devices should not be operated outside the recommended operating conditions.

***Table 21 •*** **Recommended Operating Conditions**

| **Parameter** | **Commercial** | **Industrial** | **Military** | **Units** |
|---|---|---|---|---|
| Temperature Range* | 0 to +70 | –40 to +85 | –55 to +125 | °C |
| VCCA | 4.75 to 5.25 | 4.5 to 5.5 | 4.5 to 5.5 | V |
| VCCI | 3.14 to 3.47 | 3.0 to 3.6 | 3.0 to 3.6 | V |

**Note:** *Ambient temperature ($T_A$) is used for commercial and industrial grades; case temperature ($T_C$) is used for military grades.

***Figure 16 •*** **Typical Output Drive Characteristics (Based Upon Measured Data)**



## 3.9.4 Junction Temperature ($T_J$)

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a(1)$$

**EQ 4**

where:

- $T_a$ = Ambient Temperature
- $\Delta T$ = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$ (2)
- P = Power
- $\theta_{ja}$ = Junction to ambient of package. $\theta_{ja}$ numbers are located in Table 27, page 29.

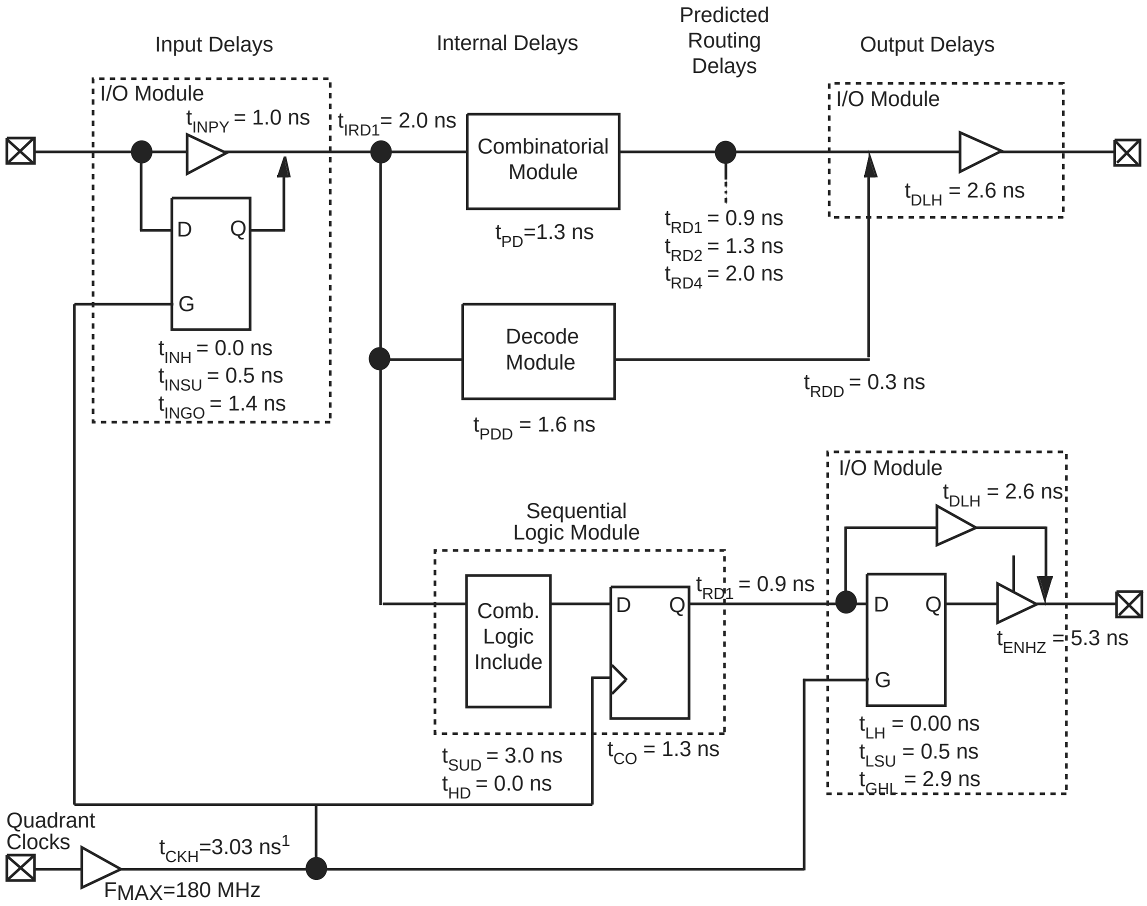
## 3.9.5 Package Thermal Characteristics

The device junction-to-case thermal characteristic is $\theta_{jc}$, and the junction-to-ambient air characteristic is $\theta_{ja}$. The thermal characteristics for $\theta_{ja}$ are shown with two different air flow rates.

The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of $\theta_{ja}$.

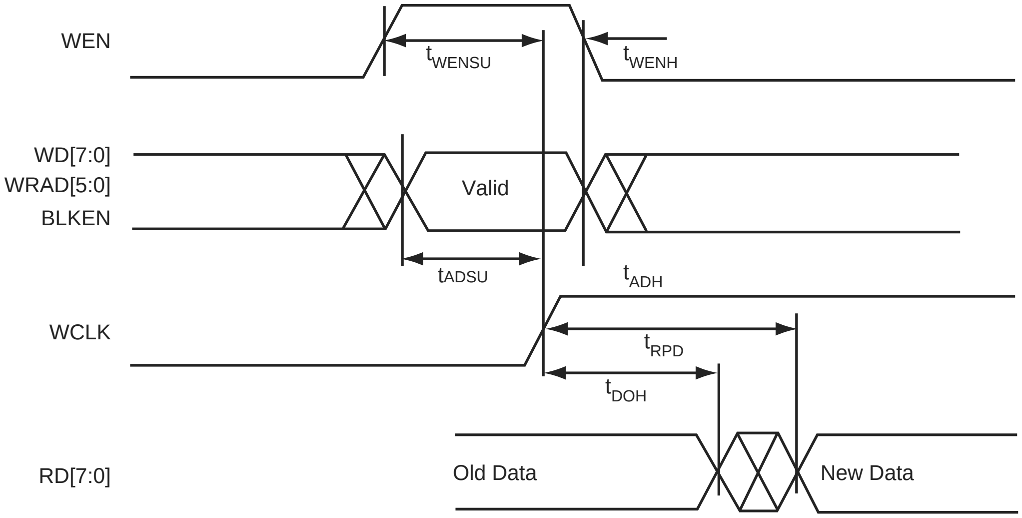
***Figure 19 •*** **42MX Timing Model (Logic Functions Using Quadrant Clocks)**



**Note:** 1. Load-dependent

**Note:** 2. Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions

***Figure 33 •*** **42MX SRAM Asynchronous Read Operation—Type 2 (Write Address Controlled)**



## 3.10.7 Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution, which is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi’s patented antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 µm lithography, offer nominal levels of 100 Ω resistance and 7.0 fF capacitance per antifuse.

MX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90 percent of interconnects using only two antifuses.

# 3.11 Timing Characteristics

Device timing characteristics fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all MX devices. Internal routing delays are device-dependent; actual delays are not determined until after place-and-route of the user's design is complete. Delay values may then be determined by using the Designer software utility or by performing simulation with post-layout delays.

## 3.11.1 Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment in Microsemi's Designer software prior to placement and routing. Up to 6% of the nets in a design may be designated as critical.

## 3.11.2 Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks add

***Table 40 •*** **A42MX16 Timing Characteristics (Nominal 5.0 V Operation)** ***(continued)*****(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| $t_{RD3}$ | FO = 3 Routing Delay | | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | | 1.6 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | | 2.6 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| **Logic Module Sequential Timing**[3,4] | | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Set-Up | | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.1 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | | 4.5 | | 5.0 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | | 6.8 | | 7.6 | | 8.6 | | 10.1 | | 14.1 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Buffer Latch Set-Up | | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTSU}$ | Output Buffer Latch Set-Up | | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | | 215 | | 195 | | 179 | | 156 | | 94 | MHz |
| **Input Module Propagation Delays** | | | | | | | | | | | | | |
| $t_{INYH}$ | Pad-to-Y HIGH | | | 1.1 | | 1.2 | | 1.3 | | 1.6 | | 2.2 | ns |
| $t_{INYL}$ | Pad-to-Y LOW | | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{INGH}$ | G to Y HIGH | | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| $t_{INGL}$ | G to Y LOW | | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| **Input Module Predicted Routing Delays**[2] | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 4.0 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 2.1 | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 2.3 | | 2.6 | | 3.0 | | 3.5 | | 4.9 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.4 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 3.6 | | 4.0 | | 4.6 | | 5.4 | | 7.5 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 32 | | 2.6 | | 2.9 | | 3.3 | | 3.9 | | 5.4 | ns |
| | | FO = 384 | | 2.9 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 32 | | 3.8 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | ns |
| | | FO = 384 | | 4.5 | | 5.0 | | 5.6 | | 6.6 | | 9.2 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 32 | 3.2 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | | ns |
| | | FO = 384 | 3.7 | | 4.1 | | 4.6 | | 5.4 | | 7.6 | | ns |

***Table 44 •*** **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| | | | **–3 Speed** | | **–2 Speed** | | **–1 Speed** | | **Std Speed** | | **–F Speed** | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Asynchronous SRAM Operations** | | | | | | | | | | | | | |
| $t_{RPD}$ | Asynchronous Access Time | | | 8.1 | | 9.0 | | 10.2 | | 12.0 | | 16.8 | ns |
| $t_{RDADV}$ | Read Address Valid | | 8.8 | | 9.8 | | 11.1 | | 13.0 | | 18.2 | | ns |
| $t_{ADSU}$ | Address/Data Set-Up Time | | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.4 | | ns |
| $t_{ADH}$ | Address/Data Hold Time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RENSUA}$ | Read Enable Set-Up to Address Valid | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | | ns |
| $t_{RENHA}$ | Read Enable Hold | | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | | ns |
| $t_{WENSU}$ | Write Enable Set-Up | | 2.7 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | | ns |
| $t_{WENH}$ | Write Enable Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{DOH}$ | Data Out Hold Time | | | 1.2 | | 1.3 | | 1.5 | | 1.8 | | 2.5 | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | | |
| $t_{INPY}$ | Input Data Pad-to-Y | | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{INGO}$ | Input Latch Gate-to-Output | | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| $t_{INH}$ | Input Latch Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Latch Set-Up | | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{ILA}$ | Latch Active Pulse Width | | 4.7 | | 5.2 | | 5.9 | | 6.9 | | 9.7 | | ns |
| **Input Module Predicted Routing Delays**[2] | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 2.3 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 2.6 | | 2.9 | | 3.3 | | 3.9 | | 5.5 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 3.0 | | 3.3 | | 3.8 | | 4.4 | | 6.2 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 4.3 | | 4.8 | | 5.5 | | 6.4 | | 9.0 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 32 | | 2.7 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| | | FO = 635 | | 3.0 | | 3.3 | | 3.8 | | 4.4 | | 6.2 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 32 | | 3.8 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | ns |
| | | FO = 635 | | 4.9 | | 5.4 | | 6.1 | | 7.2 | | 10.1 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 32 | 1.8 | | 2.0 | | 2.2 | | 2.6 | | 3.6 | | ns |
| | | FO = 635 | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | | ns |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 1.8 | | 2.0 | | 2.2 | | 2.6 | | 3.6 | | ns |
| | | FO = 635 | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 0.8 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| | | FO = 635 | | 0.8 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |

**Table 45 •** **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Synchronous SRAM Operations (continued)** | | | | | | | | | | | | |
| $t_{ADH}$ | Address/Data Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RENSU}$ | Read Enable Set-Up | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.8 | | ns |
| $t_{RENH}$ | Read Enable Hold | 4.8 | | 5.3 | | 6.0 | | 7.0 | | 9.8 | | ns |
| $t_{WENSU}$ | Write Enable Set-Up | 3.8 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | | ns |
| $t_{WENH}$ | Write Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{BENS}$ | Block Enable Set-Up | 3.9 | | 4.3 | | 4.9 | | 5.7 | | 8.0 | | ns |
| $t_{BENH}$ | Block Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| **Asynchronous SRAM Operations** | | | | | | | | | | | | |
| $t_{RPD}$ | Asynchronous Access Time | | 11.3 | | 12.6 | | 14.3 | | 16.8 | | 23.5 | ns |
| $t_{RDADV}$ | Read Address Valid | 12.3 | | 13.7 | | 15.5 | | 18.2 | | 25.5 | | ns |
| $t_{ADSU}$ | Address/Data Set-Up Time | 2.3 | | 2.5 | | 2.8 | | 3.4 | | 4.8 | | ns |
| $t_{ADH}$ | Address/Data Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RENSUA}$ | Read Enable Set-Up to Address Valid | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.8 | | ns |
| $t_{RENHA}$ | Read Enable Hold | 4.8 | | 5.3 | | 6.0 | | 7.0 | | 9.8 | | ns |
| $t_{WENSU}$ | Write Enable Set-Up | 3.8 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | | ns |
| $t_{WENH}$ | Write Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{DOH}$ | Data Out Hold Time | | 1.8 | | 2.0 | | 2.1 | | 2.5 | | 3.5 | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INPY}$ | Input Data Pad-to-Y | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 3.0 | ns |
| $t_{INGO}$ | Input Latch Gate-to-Output | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{INH}$ | Input Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Latch Set-Up | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{ILA}$ | Latch Active Pulse Width | 6.5 | | 7.3 | | 8.2 | | 9.7 | | 13.5 | | ns |

***Table 45 •*** **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| | | | **–3 Speed** | | **–2 Speed** | | **–1 Speed** | | **Std Speed** | | **–F Speed** | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Input Module Predicted Routing Delays[2]** | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 3.2 | | 3.5 | | 4.1 | | 4.8 | | 6.7 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 7.7 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 4.2 | | 4.6 | | 5.3 | | 6.2 | | 8.7 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 6.1 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 32 | | 4.6 | | 5.1 | | 5.7 | | 6.7 | | 9.3 | ns |
| | | FO = 635 | | 5.0 | | 5.6 | | 6.3 | | 7.4 | | 10.3 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 32 | | 5.3 | | 5.9 | | 6.7 | | 7.8 | | 11.0 | ns |
| | | FO = 635 | | 6.8 | | 7.6 | | 8.6 | | 10.1 | | 14.1 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 32 | 2.5 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | | ns |
| | | FO = 635 | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | | ns |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 2.5 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | | ns |
| | | FO = 635 | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.2 | ns |
| | | FO = 635 | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.2 | ns |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 635 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 4.0 | | 4.4 | | 5.0 | | 5.9 | | 8.2 | | ns |
| | | FO = 635 | 4.6 | | 5.2 | | 5.9 | | 6.9 | | 9.6 | | ns |
| $t_P$ | Minimum Period ($1/f_{MAX}$) | FO = 32 | 9.2 | | 10.2 | | 11.1 | | 12.7 | | 21.2 | | ns |
| | | FO = 635 | 9.9 | | 11.0 | | 12.0 | | 13.8 | | 23.0 | | ns |
| $f_{MAX}$ | Maximum Datapath Frequency | FO = 32 | | 108 | | 98 | | 90 | | 79 | | 47 | MHz |
| | | FO = 635 | | 100 | | 91 | | 83 | | 73 | | 44 | MHz |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.4 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 4.2 | | 4.6 | | 5.2 | | 6.2 | | 8.6 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.7 | | 4.2 | | 4.7 | | 5.5 | | 7.7 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 4.1 | | 4.6 | | 5.2 | | 6.1 | | 8.5 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.34 | | 8.2 | | 9.3 | | 10.9 | | 15.3 | ns |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 6.9 | | 7.6 | | 8.7 | | 10.2 | | 14.3 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 4.9 | | 5.5 | | 6.2 | | 7.3 | | 10.2 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 4.9 | | 5.5 | | 6.2 | | 7.3 | | 10.2 | ns |
| $t_{LSU}$ | I/O Latch Output Set-Up | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{LH}$ | I/O Latch Output Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | | 7.9 | | 8.8 | | 10.0 | | 11.8 | | 16.5 | ns |

*Table 48 •* **PL68**

| PL68 | | |
|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** |
| 24 | I/O | I/O |
| 25 | VCC | VCC |
| 26 | I/O | I/O |
| 27 | I/O | I/O |
| 28 | I/O | I/O |
| 29 | I/O | I/O |
| 30 | I/O | I/O |
| 31 | I/O | I/O |
| 32 | GND | GND |
| 33 | I/O | I/O |
| 34 | I/O | I/O |
| 35 | I/O | I/O |
| 36 | I/O | I/O |
| 37 | I/O | I/O |
| 38 | VCC | VCC |
| 39 | I/O | I/O |
| 40 | I/O | I/O |
| 41 | I/O | I/O |
| 42 | I/O | I/O |
| 43 | I/O | I/O |
| 44 | I/O | I/O |
| 45 | I/O | I/O |
| 46 | I/O | I/O |
| 47 | I/O | I/O |
| 48 | I/O | I/O |
| 49 | GND | GND |
| 50 | I/O | I/O |
| 51 | I/O | I/O |
| 52 | CLK, I/O | CLK, I/O |
| 53 | I/O | I/O |
| 54 | MODE | MODE |
| 55 | VCC | VCC |
| 56 | SDI, I/O | SDI, I/O |
| 57 | DCLK, I/O | DCLK, I/O |
| 58 | PRA, I/O | PRA, I/O |
| 59 | PRB, I/O | PRB, I/O |
| 60 | I/O | I/O |

*Table 51 •* **PQ144**

| PQ144 | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| 43 | I/O |
| 44 | GNDQ |
| 45 | GNDI |
| 46 | NC |
| 47 | I/O |
| 48 | I/O |
| 49 | I/O |
| 50 | I/O |
| 51 | I/O |
| 52 | I/O |
| 53 | I/O |
| 54 | VCC |
| 55 | VCCI |
| 56 | NC |
| 57 | I/O |
| 58 | I/O |
| 59 | I/O |
| 60 | I/O |
| 61 | I/O |
| 62 | I/O |
| 63 | I/O |
| 64 | GND |
| 65 | GNDI |
| 66 | I/O |
| 67 | I/O |
| 68 | I/O |
| 69 | I/O |
| 70 | I/O |
| 71 | SDO |
| 72 | I/O |
| 73 | I/O |
| 74 | I/O |
| 75 | I/O |
| 76 | I/O |
| 77 | I/O |
| 78 | I/O |
| 79 | GNDQ |

***Table 53 •*** **PQ208**

| **PQ208** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX16 Function** | **A42MX24 Function** | **A42MX36 Function** |
| 169 | I/O | WD, I/O | WD, I/O |
| 170 | I/O | I/O | I/O |
| 171 | NC | I/O | QCLKD, I/O |
| 172 | I/O | I/O | I/O |
| 173 | I/O | I/O | I/O |
| 174 | I/O | I/O | I/O |
| 175 | I/O | I/O | I/O |
| 176 | I/O | WD, I/O | WD, I/O |
| 177 | I/O | WD, I/O | WD, I/O |
| 178 | PRA, I/O | PRA, I/O | PRA, I/O |
| 179 | I/O | I/O | I/O |
| 180 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 181 | NC | I/O | I/O |
| 182 | NC | VCCI | VCCI |
| 183 | VCCA | VCCA | VCCA |
| 184 | GND | GND | GND |
| 185 | I/O | I/O | I/O |
| 186 | CLKB, I/O | CLKB, I/O | CLKB, I/O |
| 187 | I/O | I/O | I/O |
| 188 | PRB, I/O | PRB, I/O | PRB, I/O |
| 189 | I/O | I/O | I/O |
| 190 | I/O | WD, I/O | WD, I/O |
| 191 | I/O | WD, I/O | WD, I/O |
| 192 | I/O | I/O | I/O |
| 193 | NC | I/O | I/O |
| 194 | NC | WD, I/O | WD, I/O |
| 195 | NC | WD, I/O | WD, I/O |
| 196 | I/O | I/O | QCLKC, I/O |
| 197 | NC | I/O | I/O |
| 198 | I/O | I/O | I/O |
| 199 | I/O | I/O | I/O |
| 200 | I/O | I/O | I/O |
| 201 | NC | I/O | I/O |
| 202 | VCCI | VCCI | VCCI |
| 203 | I/O | WD, I/O | WD, I/O |
| 204 | I/O | WD, I/O | WD, I/O |
| 205 | I/O | I/O | I/O |

*Table 54 •* **PQ240**

| **PQ240** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 126 | WD, I/O |
| 127 | I/O |
| 128 | VCCI |
| 129 | I/O |
| 130 | I/O |
| 131 | I/O |
| 132 | WD, I/O |
| 133 | WD, I/O |
| 134 | I/O |
| 135 | QCLKB, I/O |
| 136 | I/O |
| 137 | I/O |
| 138 | I/O |
| 139 | I/O |
| 140 | I/O |
| 141 | I/O |
| 142 | WD, I/O |
| 143 | WD, I/O |
| 144 | I/O |
| 145 | I/O |
| 146 | I/O |
| 147 | I/O |
| 148 | I/O |
| 149 | I/O |
| 150 | VCCI |
| 151 | VCCA |
| 152 | GND |
| 153 | I/O |
| 154 | I/O |
| 155 | I/O |
| 156 | I/O |
| 157 | I/O |
| 158 | I/O |
| 159 | WD, I/O |
| 160 | WD, I/O |
| 161 | I/O |
| 162 | I/O |

***Table 57 •*** **TQ176**

| **TQ176** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 10 | NC | I/O | I/O |
| 11 | NC | I/O | I/O |
| 12 | I/O | I/O | I/O |
| 13 | NC | VCCA | VCCA |
| 14 | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O |
| 17 | I/O | I/O | I/O |
| 18 | GND | GND | GND |
| 19 | NC | I/O | I/O |
| 20 | NC | I/O | I/O |
| 21 | I/O | I/O | I/O |
| 22 | NC | I/O | I/O |
| 23 | GND | GND | GND |
| 24 | NC | VCCI | VCCI |
| 25 | VCCA | VCCA | VCCA |
| 26 | NC | I/O | I/O |
| 27 | NC | I/O | I/O |
| 28 | VCCI | VCCA | VCCA |
| 29 | NC | I/O | I/O |
| 30 | I/O | I/O | I/O |
| 31 | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O |
| 33 | NC | NC | I/O |
| 34 | I/O | I/O | I/O |
| 35 | I/O | I/O | I/O |
| 36 | I/O | I/O | I/O |
| 37 | NC | I/O | I/O |
| 38 | NC | NC | I/O |
| 39 | I/O | I/O | I/O |
| 40 | I/O | I/O | I/O |
| 41 | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | I/O | I/O | I/O |
| 45 | GND | GND | GND |
| 46 | I/O | I/O | TMS, I/O |

***Table 57 •*** **TQ176**

| **TQ176** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 84 | I/O | I/O | WD, I/O |
| 85 | I/O | I/O | WD, I/O |
| 86 | NC | I/O | I/O |
| 87 | SDO, I/O | SDO, I/O | SDO, TDO, I/O |
| 88 | I/O | I/O | I/O |
| 89 | GND | GND | GND |
| 90 | I/O | I/O | I/O |
| 91 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | NC | I/O | I/O |
| 97 | NC | I/O | I/O |
| 98 | I/O | I/O | I/O |
| 99 | I/O | I/O | I/O |
| 100 | I/O | I/O | I/O |
| 101 | NC | NC | I/O |
| 102 | I/O | I/O | I/O |
| 103 | NC | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | GND | GND | GND |
| 107 | NC | I/O | I/O |
| 108 | NC | I/O | TCK, I/O |
| 109 | LP | LP | LP |
| 110 | VCCA | VCCA | VCCA |
| 111 | GND | GND | GND |
| 112 | VCCI | VCCI | VCCI |
| 113 | VCCA | VCCA | VCCA |
| 114 | NC | I/O | I/O |
| 115 | NC | I/O | I/O |
| 116 | NC | VCCA | VCCA |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O |

***Table 58 •*** **CQ208**

| **CQ208** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 148 | I/O |
| 149 | I/O |
| 150 | GND |
| 151 | I/O |
| 152 | I/O |
| 153 | I/O |
| 154 | I/O |
| 155 | I/O |
| 156 | I/O |
| 157 | GND |
| 158 | I/O |
| 159 | SDI, I/O |
| 160 | I/O |
| 161 | WD, I/O |
| 162 | WD, I/O |
| 163 | I/O |
| 164 | VCCI |
| 165 | I/O |
| 166 | I/O |
| 167 | I/O |
| 168 | WD, I/O |
| 169 | WD, I/O |
| 170 | I/O |
| 171 | QCLKD, I/O |
| 172 | I/O |
| 173 | I/O |
| 174 | I/O |
| 175 | I/O |
| 176 | WD, I/O |
| 177 | WD, I/O |
| 178 | PRA, I/O |
| 179 | I/O |
| 180 | CLKA, I/O |
| 181 | I/O |
| 182 | VCCI |
| 183 | VCCA |
| 184 | GND |

***Table 59 •*** **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 207 | I/O |
| 208 | I/O |
| 209 | QCLKC, I/O |
| 210 | I/O |
| 211 | WD, I/O |
| 212 | WD, I/O |
| 213 | I/O |
| 214 | I/O |
| 215 | WD, I/O |
| 216 | WD, I/O |
| 217 | I/O |
| 218 | PRB, I/O |
| 219 | I/O |
| 220 | CLKB, I/O |
| 221 | I/O |
| 222 | GND |
| 223 | GND |
| 224 | VCCA |
| 225 | VCCI |
| 226 | I/O |
| 227 | CLKA, I/O |
| 228 | I/O |
| 229 | PRA, I/O |
| 230 | I/O |
| 231 | I/O |
| 232 | WD, I/O |
| 233 | WD, I/O |
| 234 | I/O |
| 235 | I/O |
| 236 | I/O |
| 237 | I/O |
| 238 | I/O |
| 239 | I/O |
| 240 | QCLKD, I/O |
| 241 | I/O |
| 242 | WD, I/O |
| 243 | GND |

***Table 61 •*** **PG132**

| **PG132** | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| N10 | I/O |
| M10 | I/O |
| N11 | I/O |
| L10 | I/O |
| M11 | I/O |
| N12 | SDO |
| M12 | I/O |
| L11 | I/O |
| N13 | I/O |
| M13 | I/O |
| K11 | I/O |
| L12 | I/O |
| L13 | I/O |
| K13 | I/O |
| H10 | I/O |
| J12 | I/O |
| J13 | I/O |
| H11 | I/O |
| H12 | I/O |
| H13 | VKS |
| G13 | VPP |

***Figure 53 •*** **CQ172**

***Table 62 •*** **CQ172**

| **CQ172** | |
|---|---|
| **Pin Number** | **A42MX16 Function** |
| 1 | MODE |
| 2 | I/O |
| 3 | I/O |
| 4 | I/O |
| 5 | I/O |
| 6 | I/O |
| 7 | GND |
| 8 | I/O |
| 9 | I/O |
| 10 | I/O |
| 11 | I/O |
| 12 | VCC |
| 13 | I/O |
| 14 | I/O |
| 15 | I/O |
| 16 | I/O |
| 17 | GND |
| 18 | I/O |
| 19 | I/O |
| 20 | I/O |