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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	6000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-2pl84

Table 23 • DC Specification (5.0 V PCI Signaling)¹

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
C _{IN}	Input Pin Capacitance			10	—	10	pF
C _{CLK}	CLK Pin Capacitance		5	12	—	10	pF
L _{PIN}	Pin Inductance			20	—	< 8 nH ⁴	nH

1. PCI Local Bus Specification, Version 2.1, Section 4.2.1.1.

2. Maximum rating for VCCI –0.5 V to 7.0 V

3. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V.

4. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

Table 24 • AC Specifications (5.0V PCI Signaling)*

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
ICL	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1) / 0.015$		–60	–10	mA
Slew (r)	Output Rise Slew Rate	0.4 V to 2.4 V load	1	5	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	2.4 V to 0.4 V load	1	5	2.8	4.3	V/ns

Note: *PCI Local Bus Specification, Version 2.1, Section 4.2.1.2.

A sample calculation of the absolute maximum power dissipation allowed for a TQ176 package at commercial temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (^\circ\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (^\circ\text{C})}{\theta_{ja} (^\circ\text{C/W})} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{(28^\circ\text{C})/\text{W}} = 2.86\text{W}$$

EQ 5

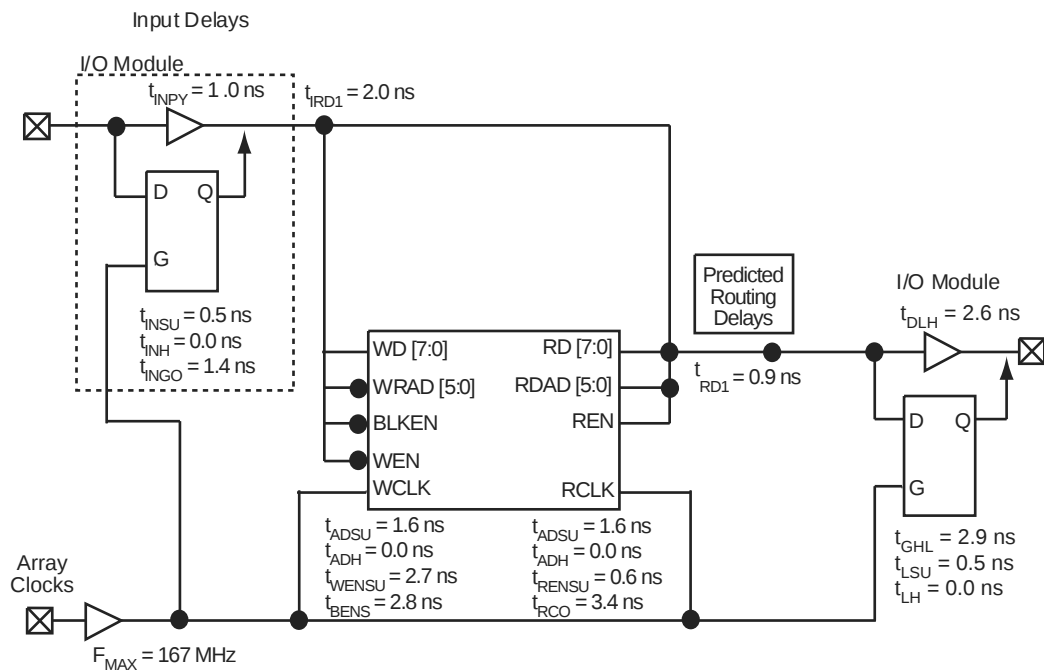
The maximum power dissipation for military-grade devices is a function of θ_{jc} . A sample calculation of the absolute maximum power dissipation allowed for CQFP 208-pin package at military temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (^\circ\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (^\circ\text{C})}{\theta_{jc} (^\circ\text{C/W})} = \frac{150^\circ\text{C} - 125^\circ\text{C}}{(6.3^\circ\text{C})/\text{W}} = 3.97\text{W}$$

EQ 6

Table 27 • Package Thermal Characteristics

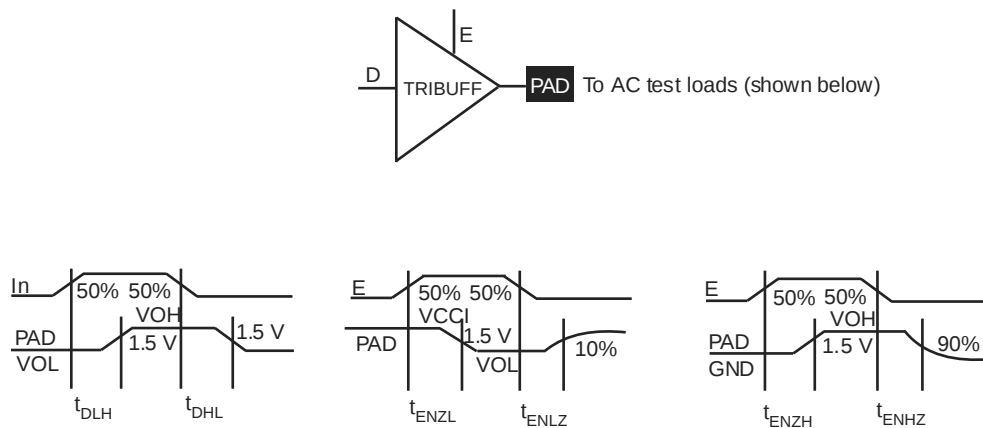
Plastic Packages	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	1.0 m/s 200 ft/min.	2.5 m/s 500 ft/min.	
Plastic Quad Flat Pack	100	12.0	27.8	23.4	21.2	$^\circ\text{C/W}$
Plastic Quad Flat Pack	144	10.0	26.2	22.8	21.1	$^\circ\text{C/W}$
Plastic Quad Flat Pack	160	10.0	26.2	22.8	21.1	$^\circ\text{C/W}$
Plastic Quad Flat Pack	208	8.0	26.1	22.5	20.8	$^\circ\text{C/W}$
Plastic Quad Flat Pack	240	8.5	25.6	22.3	20.8	$^\circ\text{C/W}$
Plastic Leaded Chip Carrier	44	16.0	20.0	24.5	22.0	$^\circ\text{C/W}$
Plastic Leaded Chip Carrier	68	13.0	25.0	21.0	19.4	$^\circ\text{C/W}$
Plastic Leaded Chip Carrier	84	12.0	22.5	18.9	17.6	$^\circ\text{C/W}$
Thin Plastic Quad Flat Pack	176	11.0	24.7	19.9	18.0	$^\circ\text{C/W}$
Very Thin Plastic Quad Flat Pack	80	12.0	38.2	31.9	29.4	$^\circ\text{C/W}$
Very Thin Plastic Quad Flat Pack	100	10.0	35.3	29.4	27.1	$^\circ\text{C/W}$
Plastic Ball Grid Array	272	3.0	18.3	14.9	13.9	$^\circ\text{C/W}$
Ceramic Packages						
Ceramic Pin Grid Array	132	4.8	25.0	20.6	18.7	$^\circ\text{C/W}$
Ceramic Quad Flat Pack	208	2.0	22.0	19.8	18.0	$^\circ\text{C/W}$
Ceramic Quad Flat Pack	256	2.0	20.0	16.5	15.0	$^\circ\text{C/W}$

Figure 20 • 42MX Timing Model (SRAM Functions)

Note: Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions.

3.10.1 Parameter Measurement

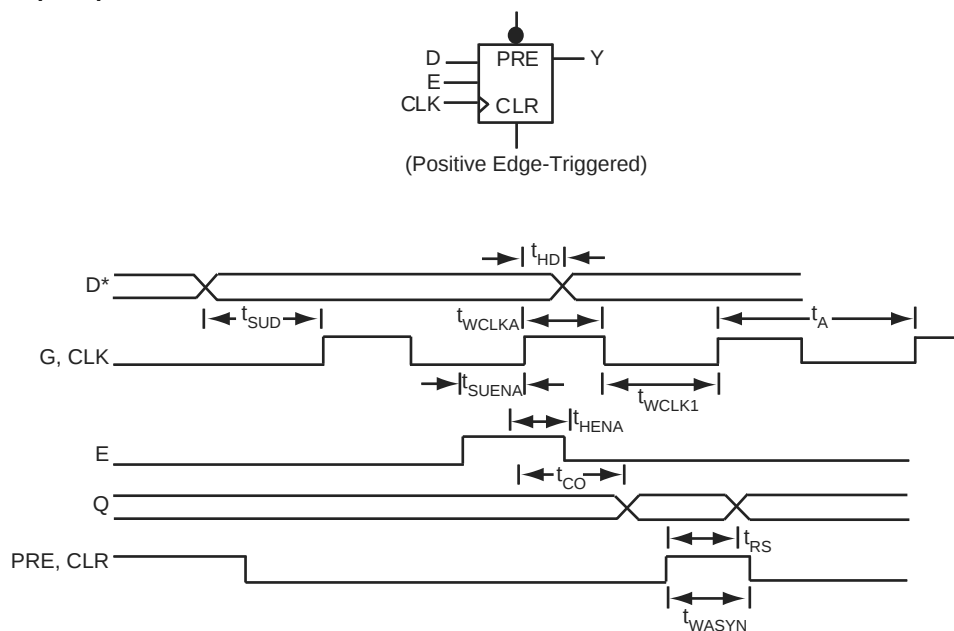
The following figures show parameter measurement details.

Figure 21 • Output Buffer Delays

3.10.2 Sequential Module Timing Characteristics

The following figure shows sequential module timing characteristics.

Figure 25 • Flip-Flops and Latches



Note: *D represents all data functions involving A, B, and S for multiplexed flip-flops.

3.10.3 Sequential Timing Characteristics

The following figures show sequential timing characteristics.

Figure 26 • Input Buffer Latches

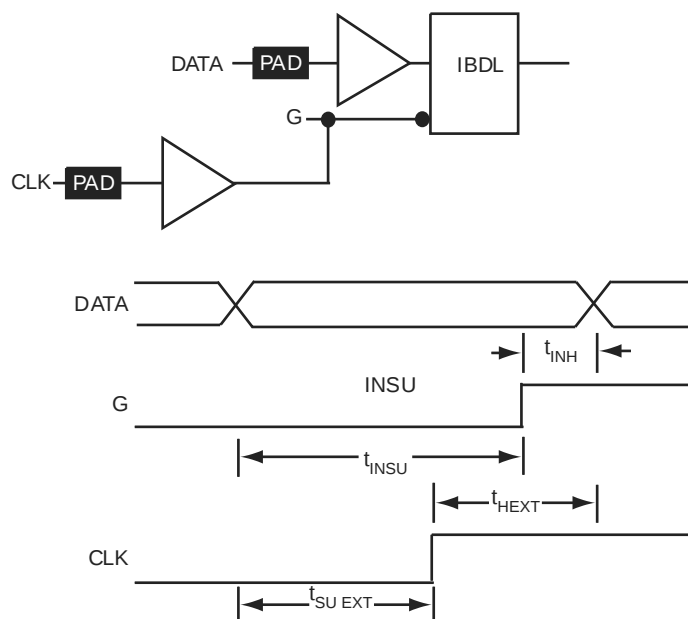


Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RD1}	FO = 1 Routing Delay		2.0		2.2		2.5		3.0		4.2	ns
t _{RD2}	FO = 2 Routing Delay		2.7		3.1		3.5		4.1		5.7	ns
t _{RD3}	FO = 3 Routing Delay		3.4		3.9		4.4		5.2		7.3	ns
t _{RD4}	FO = 4 Routing Delay		4.2		4.8		5.4		6.3		8.9	ns
t _{RD8}	FO = 8 Routing Delay		7.1		8.2		9.2		10.9		15.2	ns
Logic Module Sequential Timing²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		4.3		4.9		5.6		6.6		9.2	ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		4.3		4.9		5.6		6.6		9.2	ns
t _{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		4.6		5.3		6.0		7.0		9.8	ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		4.6		5.3		6.0		7.0		9.8	ns
t _A	Flip-Flop Clock Input Period		6.8		7.8		8.9		10.4		14.6	ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		109		101		92		80		48	MHz
Input Module Propagation Delays												
t _{INYH}	Pad-to-Y HIGH		1.0		1.1		1.3		1.5		2.1	ns
t _{INYL}	Pad-to-Y LOW		0.9		1.0		1.1		1.3		1.9	ns
Input Module Predicted Routing Delays¹												
t _{IRD1}	FO = 1 Routing Delay		2.9		3.4		3.8		4.5		6.3	ns
t _{IRD2}	FO = 2 Routing Delay		3.6		4.2		4.8		5.6		7.8	ns
t _{IRD3}	FO = 3 Routing Delay		4.4		5.0		5.7		6.7		9.4	ns
t _{IRD4}	FO = 4 Routing Delay		5.1		5.9		6.7		7.8		11.0	ns
t _{IRD8}	FO = 8 Routing Delay		8.0		9.26		10.5		12.6		17.3	ns
Global Clock Network												
t _{CKH}	Input LOW to HIGH	FO = 16	6.4		7.4		8.3		9.8		13.7	ns
		FO = 128	6.4		7.4		8.3		9.8		13.7	
t _{CKL}	Input HIGH to LOW	FO = 16	6.7		7.8		8.8		10.4		14.5	ns
		FO = 128	6.7		7.8		8.8		10.4		14.5	
t _{PWH}	Minimum Pulse Width HIGH	FO = 16	3.1		3.6		4.1		4.8		6.7	ns
		FO = 128	3.3		3.8		4.3		5.1		7.1	
t _{PWL}	Minimum Pulse Width LOW	FO = 16	3.1		3.6		4.1		4.8		6.7	ns
		FO = 128	3.3		3.8		4.3		5.1		7.1	
t _{CKSW}	Maximum Skew	FO = 16	0.6		0.6		0.7		0.8		1.2	ns
		FO = 128	0.8		0.9		1.0		1.2		1.6	

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		3.3		3.8		4.3		5.0		7.0		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		3.3		3.8		4.3		5.0		7.0		ns
t _A	Flip-Flop Clock Input Period		4.8		5.6		6.3		7.5		10.4		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)			181		167		154		134		80	MHz
Input Module Propagation Delays													
t _{INyh}	Pad-to-Y HIGH			0.7		0.8		0.9		1.1		1.5	ns
t _{INyl}	Pad-to-Y LOW			0.6		0.7		0.8		1.0		1.3	ns
Input Module Predicted Routing Delays ¹													
t _{IRD1}	FO = 1 Routing Delay			2.1		2.4		2.2		3.2		4.5	ns
t _{IRD2}	FO = 2 Routing Delay			2.6		3.0		3.4		4.0		5.6	ns
t _{IRD3}	FO = 3 Routing Delay			3.1		3.6		4.1		4.8		6.7	ns
t _{IRD4}	FO = 4 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t _{IRD8}	FO = 8 Routing Delay			5.7		6.6		7.5		8.8		12.4	ns
Global Clock Network													
t _{CKH}	Input Low to HIGH	FO = 16		4.6		5.3		6.0		7.0		9.8	ns
		FO = 128		4.6		5.3		6.0		7.0		9.8	
t _{CKL}	Input High to LOW	FO = 16		4.8		5.6		6.3		7.4		10.4	ns
		FO = 128		4.8		5.6		6.3		7.4		10.4	
t _{PWH}	Minimum Pulse Width HIGH	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.1		3.6		5.1		
t _{PWL}	Minimum Pulse Width LOW	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.01		3.6		5.1		
t _{CKSW}	Maximum Skew	FO = 16		0.4		0.5		0.5		0.6		0.8	ns
		FO = 128		0.5		0.6		0.7		0.8		1.2	
t _P	Minimum Period	FO = 16	4.7		5.4		6.1		7.2		10.0		ns
		FO = 128	4.8		5.6		6.3		7.5		10.4		
f _{MAX}	Maximum Frequency	FO = 16		188		175		160		139		83	MHz
		FO = 128		181		168		154		134		80	
TTL Output Module Timing ⁴													
t _{DLH}	Data-to-Pad HIGH			3.3		3.8		4.3		5.1		7.2	ns
t _{DHL}	Data-to-Pad LOW			4.0		4.6		5.2		6.1		8.6	ns
t _{ENZH}	Enable Pad Z to HIGH			3.7		4.3		4.9		5.8		8.0	ns
t _{ENZL}	Enable Pad Z to LOW			4.7		5.4		6.1		7.2		10.1	ns
t _{ENHZ}	Enable Pad HIGH to Z			7.9		9.1		10.4		12.2		17.1	ns

Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		2.4		2.7		3.1		3.6		5.1	ns
t _{DHL}	Data-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t _{ENZH}	Enable Pad Z to HIGH		2.7		2.9		3.3		3.9		5.5	ns
t _{ENZL}	Enable Pad Z to LOW		2.9		3.2		3.7		4.3		6.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		4.9		5.4		6.2		7.3		10.2	ns
t _{ENLZ}	Enable Pad LOW to Z		5.3		5.9		6.7		7.9		11.1	ns
t _{GLH}	G-to-Pad HIGH		4.2		4.6		5.2		6.1		8.6	ns
t _{GHL}	G-to-Pad LOW		4.2		4.6		5.2		6.1		8.6	ns
t _{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.2		5.8		6.6		7.7		10.8	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.4		8.2		9.3		10.9		15.3	ns
d _{TLH}	Capacity Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF
d _{THL}	Capacity Loading, HIGH to LOW		0.04		0.04		0.04		0.05		0.07	ns/pF

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays ¹												
t _{PD1}	Single Module		1.6		1.8		2.1		2.5		3.5	ns
t _{CO}	Sequential Clock-to-Q		1.8		2.0		2.3		2.7		3.8	ns
t _{GO}	Latch G-to-Q		1.7		1.9		2.1		2.5		3.5	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		2.0		2.2		2.5		2.9		4.1	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		1.0		1.1		1.2		1.4		2.0	ns
t _{RD2}	FO = 2 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t _{RD3}	FO = 3 Routing Delay		1.6		1.8		2.0		2.4		3.3	ns

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		3.4		3.8		5.5		6.4		9.0	ns
t _{DHL}	Data-to-Pad LOW		4.1		4.5		4.2		5.0		7.0	ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t _{ENZL}	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t _{ENHZ}	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t _{ENLZ}	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t _{GLH}	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t _{GHL}	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t _{LSU}	I/O Latch Set-Up		0.7		0.8		0.9		1.0		1.4	ns
t _{LH}	I/O Latch Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d _{TLH}	Capacity Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{THL}	Capacity Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Logic Module Propagation Delays ¹													
t _{PD1}	Single Module		1.4		1.5		1.7		2.0		2.8		ns
t _{CO}	Sequential Clock-to-Q		1.4		1.6		1.8		2.1		3.0		ns
t _{GO}	Latch G-to-Q		1.4		1.5		1.7		2.0		2.8		ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.6		1.7		2.0		2.3		3.3		ns
Logic Module Predicted Routing Delays ²													
t _{RD1}	FO = 1 Routing Delay		0.8		0.9		1.0		1.2		1.6		ns
t _{RD2}	FO = 2 Routing Delay		1.0		1.2		1.3		1.5		2.1		ns

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay		1.8		2.0		2.3		2.7		3.8		ns
t _{IRD2}	FO = 2 Routing Delay		2.1		2.3		2.6		3.1		4.3		ns
t _{IRD3}	FO = 3 Routing Delay		2.3		2.5		2.9		3.4		4.8		ns
t _{IRD4}	FO = 4 Routing Delay		2.5		2.8		3.2		3.7		5.2		ns
t _{IRD8}	FO = 8 Routing Delay		3.4		3.8		4.3		5.1		7.1		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32	2.6		2.9		3.3		3.9		5.4		ns
		FO = 486	2.9		3.2		3.6		4.3		5.9		ns
t _{CKL}	Input HIGH to LOW	FO = 32	3.7		4.1		4.6		5.4		7.6		ns
		FO = 486	4.3		4.7		5.4		6.3		8.8		ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	2.2	2.4	2.7		3.2		4.5				ns
		FO = 486	2.4	2.6	3.0		3.5		4.9				ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	2.2	2.4	2.7		3.2		4.5				ns
		FO = 486	2.4	2.6	3.0		3.5		4.9				ns
t _{CKSW}	Maximum Skew	FO = 32	0.5		0.6		0.7		0.8		1.1		ns
		FO = 486	0.5		0.6		0.7		0.8		1.1		ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0	0.0	0.0		0.0		0.0				ns
		FO = 486	0.0	0.0	0.0		0.0		0.0				ns
t _{HEXT}	Input Latch External Hold	FO = 32	2.8	3.1	3.5		4.1		5.7				ns
		FO = 486	3.3	3.7	4.2		4.9		6.9				ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	4.7	5.2	5.7		6.5		10.9				ns
		FO = 486	5.1	5.7	6.2		7.1		11.9				ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 635	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	2.8		3.2		3.6		4.2		5.9		ns
		FO = 635	3.3		3.7		4.2		4.9		6.9		ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	5.5		6.1		6.6		7.6		12.7		ns
		FO = 635	6.0		6.6		7.2		8.3		13.8		ns
f _{MAX}	Maximum Datapath Frequency	FO = 32		180		164		151		131		79	MHz
		FO = 635		166		151		139		121		73	MHz
TTL Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH			2.6		2.8		3.2		3.8		5.3	ns
t _{DHL}	Data-to-Pad LOW			3.0		3.3		3.7		4.4		6.2	ns
t _{ENZH}	Enable Pad Z to HIGH			2.7		3.0		3.3		3.9		5.5	ns
t _{ENZL}	Enable Pad Z to LOW			3.0		3.3		3.7		4.3		6.1	ns
t _{ENHZ}	Enable Pad HIGH to Z			5.3		5.8		6.6		7.8		10.9	ns

Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
47	I/O	I/O	I/O	WD, I/O
48	I/O	I/O	I/O	I/O
49	I/O	GND	GND	GND
50	I/O	I/O	I/O	WD, I/O
51	I/O	I/O	I/O	WD, I/O
52	I/O	SDO, I/O	SDO, I/O	SDO, TDO, I/O
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	GND	I/O	I/O	I/O
61	GND	I/O	I/O	I/O
62	I/O	I/O	I/O	TCK, I/O
63	I/O	LP	LP	LP
64	CLK, I/O	VCCA	VCCA	VCCA
65	I/O	VCCI	VCCI	VCCI
66	MODE	I/O	I/O	I/O
67	VCC	I/O	I/O	I/O
68	VCC	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	GND	GND	GND
71	I/O	I/O	I/O	I/O
72	SDI, I/O	I/O	I/O	I/O
73	DCLK, I/O	I/O	I/O	I/O
74	PRA, I/O	I/O	I/O	I/O
75	PRB, I/O	I/O	I/O	I/O
76	I/O	SDI, I/O	SDI, I/O	SDI, I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	WD, I/O
79	I/O	I/O	I/O	WD, I/O
80	I/O	I/O	I/O	WD, I/O
81	I/O	PRA, I/O	PRA, I/O	PRA, I/O
82	GND	I/O	I/O	I/O
83	I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O

Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	VCCA	VCCA
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	VCCA	VCCA
139	VCCI	VCCI	VCCI
140	GND	GND	GND
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	GND	GND	GND
146	NC	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	NC	VCCA	VCCA
151	NC	I/O	I/O
152	NC	I/O	I/O
153	NC	I/O	I/O
154	NC	I/O	I/O
155	GND	GND	GND
156	I/O	I/O	I/O
157	I/O	I/O	I/O
158	I/O	I/O	I/O
159	MODE	MODE	MODE
160	GND	GND	GND

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
89	VCCI
90	VCCA
91	LP
92	TCK, I/O
93	I/O
94	GND
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	VCCI
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	VCCA
119	GND
120	GND
121	GND
122	I/O
123	SDO, TDO, I/O
124	I/O
125	WD, I/O

Table 55 • VQ80

VQ80		
Pin Number	A40MX02 Function	A40MX04 Function
13	VCC	VCC
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	NC	I/O
18	NC	I/O
19	NC	I/O
20	VCC	VCC
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	GND	GND
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	VCC	VCC
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O
41	NC	I/O
42	NC	I/O
43	NC	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	GND	GND
48	I/O	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
207	I/O
208	I/O
209	QCLKC, I/O
210	I/O
211	WD, I/O
212	WD, I/O
213	I/O
214	I/O
215	WD, I/O
216	WD, I/O
217	I/O
218	PRB, I/O
219	I/O
220	CLKB, I/O
221	I/O
222	GND
223	GND
224	VCCA
225	VCCI
226	I/O
227	CLKA, I/O
228	I/O
229	PRA, I/O
230	I/O
231	I/O
232	WD, I/O
233	WD, I/O
234	I/O
235	I/O
236	I/O
237	I/O
238	I/O
239	I/O
240	QCLKD, I/O
241	I/O
242	WD, I/O
243	GND

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
C3	GND
C4	I/O
C5	WD, I/O
C6	I/O
C7	QCLKC, I/O
C8	I/O
C9	I/O
C10	CLKB
C11	PRA, I/O
C12	WD, I/O
C13	I/O
C14	QCLKD, I/O
C15	I/O
C16	WD, I/O
C17	SDI, I/O
C18	I/O
C19	I/O
C20	I/O
D1	I/O
D2	I/O
D3	I/O
D4	I/O
D5	VCCI
D6	I/O
D7	I/O
D8	VCCA
D9	WD, I/O
D10	VCCI
D11	I/O
D12	VCCI
D13	I/O
D14	VCCI
D15	I/O
D16	VCCA
D17	GND
D18	I/O
D19	I/O

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
V16	I/O
V17	I/O
V18	SDO, TDO, I/O
V19	I/O
V20	I/O
W1	GND
W2	GND
W3	I/O
W4	TMS, I/O
W5	I/O
W6	I/O
W7	I/O
W8	WD, I/O
W9	WD, I/O
W10	I/O
W11	I/O
W12	I/O
W13	WD, I/O
W14	I/O
W15	I/O
W16	WD, I/O
W17	I/O
W18	WD, I/O
W19	GND
W20	GND
Y1	GND
Y2	GND
Y3	I/O
Y4	TDI, I/O
Y5	WD, I/O
Y6	I/O
Y7	QCLKA, I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	I/O

Table 61 • PG132

PG132	
Pin Number	A42MX09 Function
F2	I/O
F1	I/O
G1	I/O
G4	VSV
H1	I/O
H2	I/O
H3	I/O
H4	I/O
J1	I/O
K1	I/O
L1	I/O
K2	I/O
M1	I/O
K3	I/O
L2	I/O
N1	I/O
L3	BININ
M2	BINOUT
N2	I/O
M3	I/O
L4	I/O
N3	I/O
M4	I/O
N4	I/O
M5	I/O
K6	I/O
N5	I/O
N6	I/O
L6	I/O
M6	I/O
M7	I/O
N7	I/O
N8	I/O
M8	I/O
L8	I/O
K8	I/O
N9	I/O

Table 61 • PG132

PG132	
Pin Number	A42MX09 Function
N10	I/O
M10	I/O
N11	I/O
L10	I/O
M11	I/O
N12	SDO
M12	I/O
L11	I/O
N13	I/O
M13	I/O
K11	I/O
L12	I/O
L13	I/O
K13	I/O
H10	I/O
J12	I/O
J13	I/O
H11	I/O
H12	I/O
H13	VKS
G13	VPP

Table 62 • CQ172

21	I/O
22	GND
23	VCCI
24	VSV
25	I/O
26	I/O
27	VCC
28	I/O
29	I/O
30	I/O
31	I/O
32	GND
33	I/O
34	I/O
35	I/O
36	I/O
37	GND
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	BININ
45	BINOUT
46	I/O
47	I/O
48	I/O
49	I/O
50	VCCI
51	I/O
52	I/O
53	I/O
54	I/O
55	GND
56	I/O
57	I/O
58	I/O
59	I/O