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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	6000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-2plg84i">https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-2plg84i</a>

Figure 51	BG272 .....	145
Figure 52	PG132 .....	153
Figure 53	CQ172 .....	158

- The Transient Current, page 13 is new (SAR 36930).
- Package names were revised according to standards established in *Package Mechanical Drawings* (SAR 34774)

## 1.7 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document

- In Table 20, page 23, the limits in VI were changed from -0.5 to VCCI + 0.5 to -0.5 to VCCA + 0.5
- In Table 22, page 25,  $V_{OH}$  was changed from 3.7 to 2.4 for the min in industrial and military.  $V_{IH}$  had  $V_{CCI}$  and that was changed to VCCA

## 1.8 Revision 6.0

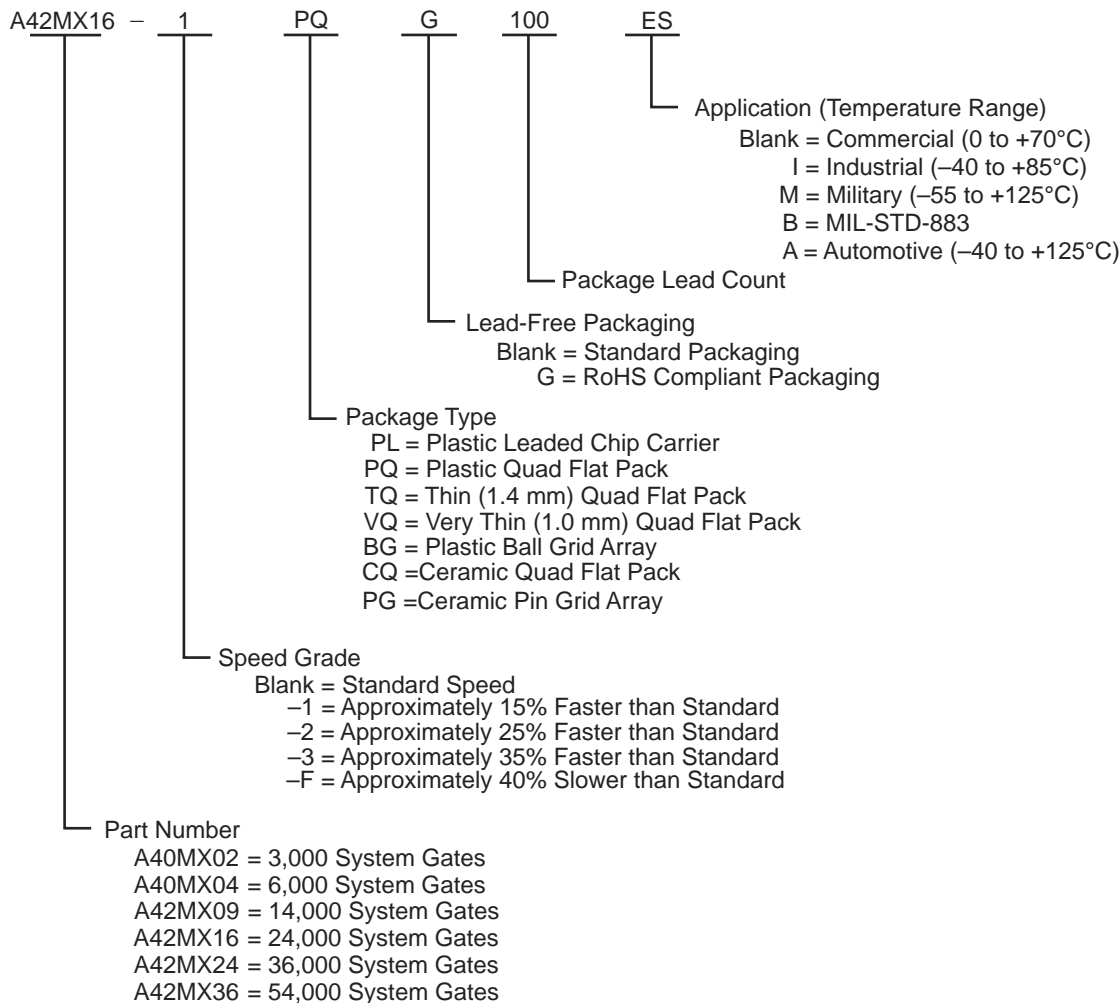
The following is a summary of the changes in revision 6.0 of this document.

- The Ease of Integration, page 1 was updated
- The Temperature Grade Offerings, page 5 is new
- The Speed Grade Offerings, page 5 is new
- The General Description, page 6 was updated
- The MultiPlex I/O Modules, page 11 was updated
- The User Security, page 12 was updated
- Table 6, page 13 was updated
- The Power Dissipation, page 14 was updated.
- The Static Power Component, page 14 was updated
- The Equivalent Capacitance, page 15 was updated
- Figure 13, page 17 was updated
- Table 10, page 18 was updated.
- Figure 14, page 18 was updated.
- Table 11, page 19 was updated.

## 2.3 Ordering Information

The following figure shows ordering information. All the following tables show plastic and ceramic device resources, temperature and speed grade offerings.

**Figure 1 • Ordering Information**



## 2.4 Plastic Device Resources

**Table 2 • Plastic Device Resources**

Device	User I/Os											
	PLCC 44-Pin	PLCC 68-Pin	PLCC 84-Pin	PQFP 100-Pin	PQFP 144- Pin	PQFP 160-Pin	PQFP 208- Pin	PQFP 240-Pin	VQFP 80-Pin	VQFP 100- Pin	TQFP 176- Pin	PBGA 272- Pin
A40MX02	34	57	—	57	—	—	—	—	57	—	—	—
A40MX04	34	57	69	69	—	—	—	—	69	—	—	—
A42MX09	—	—	72	83	95	101	—	—	—	83	104	—
A42MX16	—	—	72	83	—	125	140	—	—	83	140	—
A42MX24	—	—	72	—	—	125	176	—	—	—	150	—
A42MX36	—	—	—	—	—	—	176	202	—	—	—	202

**Note: Package Definitions:** PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array

## 2.5 Ceramic Device Resources

**Table 3 • Ceramic Device Resources**

Device	User I/Os			
	CPGA 132-Pin	CQFP 172-Pin	CQFP 208-Pin	CQFP 256-Pin
A42MX09	95			
A42MX16		131		
A42MX36			176	202

**Note: Package Definitions:** CQFP = Ceramic Quad Flat Pack

$f_{q2}$  = Average second routed array clock rate in MHz)

**Table 7 • Fixed Capacitance Values for MX FPGAs (pF)**

Device Type	r1 routed_Clk1	r2 routed_Clk2
A40MX02	41.4	N/A
A40MX04	68.6	N/A
A42MX09	118	118
A42MX16	165	165
A42MX24	185	185
A42MX36	220	220

### 3.4.6 Test Circuitry and Silicon Explorer II Probe

MX devices contain probing circuitry that provides built-in access to every node in a design, via the use of Silicon Explorer II. Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer software, allow users to examine any of the internal nets of the device while it is operating in a prototyping or a production system. The user can probe into an MX device without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle and providing a true representation of the device under actual functional situations.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

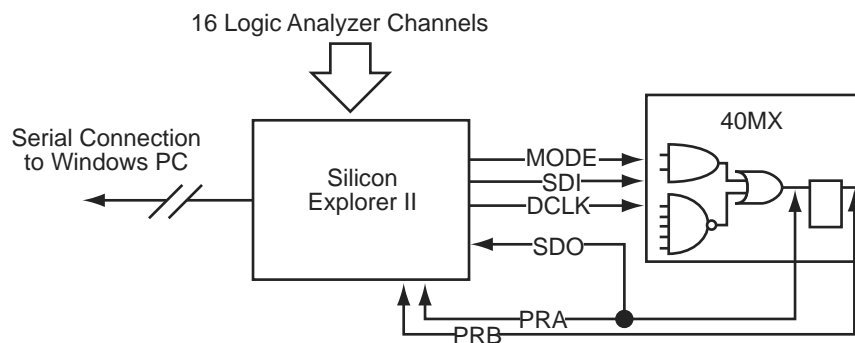
Silicon Explorer II is used to control the MODE, DCLK, SDI and SDO pins in MX devices to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the MODE pin is held HIGH.

Figure 12, page 16 illustrates the interconnection between Silicon Explorer II and 40MX devices, while Figure 13, page 17 illustrates the interconnection between Silicon Explorer II and 42MX devices

To allow for probing capabilities, the security fuses must not be programmed. (See User Security, page 12 for the security fuses of 40MX and 42MX devices). Table 8, page 17 summarizes the possible device configurations for probing.

PRA and PRB pins are dual-purpose pins. When the "Reserve Probe Pin" is checked in the Designer software, PRA and PRB pins are reserved as dedicated outputs for probing. If PRA and PRB pins are required as user I/Os to achieve successful layout and "Reserve Probe Pin" is checked, the layout tool will override the option and place user I/Os on PRA and PRB pins.

**Figure 12 • Silicon Explorer II Setup with 40MX**



### 3.4.9 JTAG Mode Activation

The JTAG test logic circuit is activated in the Designer software by selecting **Tools > Device Selection**. This brings up the Device Selection dialog box as shown in the following figure. The JTAG test logic circuit can be enabled by clicking the “Reserve JTAG Pins” check box. The following table explains the pins' behavior in either mode.

**Figure 15 • Device Selection Wizard**

**Table 11 • Boundary Scan Pin Configuration and Functionality**

Reserve JTAG	Checked	Unchecked
TCK	BST input; must be terminated to logical HIGH or LOW to avoid floating	User I/O
TDI, TMS	BST input; may float or be tied to HIGH	User I/O
TDO	BST output; may float or be connected to TDI of another device	User I/O

### 3.4.10 TRST Pin and TAP Controller Reset

An active reset (TRST) pin is not supported; however, MX devices contain power-on circuitry that resets the boundary scan circuitry upon power-up. Also, the TMS pin is equipped with an internal pull-up resistor. This allows the TAP controller to remain in or return to the Test-Logic-Reset state when there is no input or when a logical 1 is on the TMS pin. To reset the controller, TMS must be HIGH for at least five TCK cycles.

### 3.4.11 Boundary Scan Description Language (BSDL) File

Conforming to the IEEE Standard 1149.1 requires that the operation of the various JTAG components be documented. The BSDL file provides the standard format to describe the JTAG components that can be used by automatic test equipment software. The file includes the instructions that are supported, instruction bit pattern, and the boundary-scan chain order. For an in-depth discussion on BSDL files, see the *BSDL Files Format Description* application note.

BSDL files are grouped into two categories - generic and device-specific. The generic files assign all user I/Os as inouts. Device-specific files assign user I/Os as inputs, outputs or inouts.

Generic files for MX devices are available on the Microsemi SoC Product Group's website:

<http://www.microsemi.com/soc/techdocs/models/bsdl.html>.

## 3.5 Development Tool Support

The MX family of FPGAs is fully supported by Libero® Integrated Design Environment (IDE). Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes SynplifyPro from Synopsys, ModelSim® HDL Simulator from Mentor Graphics® and Viewdraw.

Libero IDE includes place-and-route and provides a comprehensive suite of backend support tools for FPGA development, including timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor.

3. All outputs unloaded. All inputs = VCC/VCCI or GND

## 3.8 3.3 V Operating Conditions

The following table shows 3.3 V operating conditions.

**Table 16 • Absolute Maximum Ratings for 40MX Devices\***

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	−0.5 to +7.0	V
VI	Input Voltage	−0.5 to VCC + 0.5	V
VO	Output Voltage	−0.5 to VCC + 0.5	V
t <sub>STG</sub>	Storage Temperature	−65 to + 150	°C

**Note:** \*Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

**Table 17 • Absolute Maximum Ratings for 42MX Devices\***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	−0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	−0.5 to +7.0	V
VI	Input Voltage	−0.5 to VCCI+0.5	V
VO	Output Voltage	−0.5 to VCCI+0.5	V
t <sub>STG</sub>	Storage Temperature	−65 to +150	°C

**Note:** \*Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

**Table 18 • Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	−40 to +85	−55 to +125	°C
VCC (40MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCA (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCI (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

**Note:** \*Ambient temperature (T<sub>A</sub>) is used for commercial and industrial grades; case temperature (T<sub>C</sub>) is used for military grades.

All the following tables show various specifications and operating conditions of 40MX and 42MX FPGAs.



**Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>ENLZ</sub>	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d <sub>TLH</sub>	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d <sub>THL</sub>	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

**Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 3.0 V, T<sub>J</sub> = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing <sup>4</sup>												
t <sub>DLH</sub>	Data-to-Pad HIGH		5.5		6.4		7.2		8.5		11.9	ns
t <sub>DHL</sub>	Data-to-Pad LOW		4.8		5.5		6.2		7.3		10.2	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		4.7		5.5		6.2		7.3		10.2	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		6.8		7.9		8.9		10.5		14.7	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7	ns
d <sub>TLH</sub>	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d <sub>THL</sub>	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading.

**Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T<sub>J</sub> = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays <sup>1</sup>												
t <sub>PD1</sub>	Single Module		1.2		1.3		1.5		1.8		2.5	ns
t <sub>CO</sub>	Sequential Clock-to-Q		1.3		1.4		1.6		1.9		2.7	ns
t <sub>GO</sub>	Latch G-to-Q		1.2		1.4		1.6		1.8		2.6	ns
t <sub>RS</sub>	Flip-Flop (Latch) Reset-to-Q		1.2		1.6		1.8		2.1		2.9	ns
Logic Module Predicted Routing Delays <sup>2</sup>												
t <sub>RD1</sub>	FO = 1 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		0.9		1.0		1.2		1.4		1.9	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.2		1.3		1.5		1.7		2.4	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.4		1.5		1.7		2.0		2.9	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.3		2.6		2.9		3.4		4.8	ns
Logic Module Sequential Timing <sup>3, 4</sup>												
t <sub>SUD</sub>	Flip-Flop (Latch) Data Input Set-Up	0.3		0.4		0.4		0.5		0.7		ns
t <sub>HD</sub>	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>SUENA</sub>	Flip-Flop (Latch) Enable Set-Up	0.4		0.5		0.5		0.6		0.8		ns
t <sub>HENA</sub>	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>WCLKA</sub>	Flip-Flop (Latch) Clock Active Pulse Width	3.4		3.8		4.3		5.0		7.0		ns

**Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T<sub>J</sub> = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing <sup>5</sup>												
t <sub>DLH</sub>	Data-to-Pad HIGH		3.2		3.6		4.0		4.7		6.6	ns
t <sub>DHL</sub>	Data-to-Pad LOW		2.5		2.7		3.1		3.6		5.1	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		2.7		3.0		3.4		4.0		5.6	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		3.0		3.3		3.8		4.4		6.2	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		5.4		6.0		6.8		8.0		11.2	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		5.0		5.6		6.3		7.4		10.4	ns
t <sub>GLH</sub>	G-to-Pad HIGH		5.1		5.6		6.4		7.5		10.5	ns
t <sub>GHL</sub>	G-to-Pad LOW		5.1		5.6		6.4		7.5		10.5	ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.7		6.3		7.1		8.4		11.9	ns
t <sub>ACO</sub>	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.0		8.9		10.1		11.9		16.7	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF

1. For dual-module macros, use t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>, point and position whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

**Table 41 • A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T<sub>J</sub> = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays <sup>1</sup>												
t <sub>PD1</sub>	Single Module		1.9		2.1		2.4		2.8		4.0	ns
t <sub>CO</sub>	Sequential Clock-to-Q		2.0		2.2		2.5		3.0		4.2	ns
t <sub>GO</sub>	Latch G-to-Q		1.9		2.1		2.4		2.8		4.0	ns
t <sub>RS</sub>	Flip-Flop (Latch) Reset-to-Q		2.2		2.4		2.8		3.3		4.6	ns
Logic Module Predicted Routing Delays <sup>2</sup>												
t <sub>RD1</sub>	FO = 1 Routing Delay		1.1		1.2		1.4		1.6		2.3	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.5		1.6		1.8		2.1		3.0	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.8		2.0		2.3		2.7		3.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		2.2		2.4		2.7		3.2		4.5	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		3.6		4.0		4.5		5.3		7.5	ns

Input, output, tristate or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/Os pins are configured by the Designer software as shown in Table 46, page 84.

**Table 46 • Configuration of Unused I/Os**

Device	Configuration
A40MX02, A40MX04	Pulled LOW
A42MX09, A42MX16	Pulled LOW
A42MX24, A42MX36	Tristated

In all cases, it is recommended to tie all unused MX I/O pins to LOW on the board. This applies to all dual-purpose pins when configured as I/Os as well.

#### **LP, Low Power Mode**

Controls the low power mode of all 42MX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation in 200  $\mu$ s after the LP pin is driven to a logic LOW.

#### **MODE, Mode**

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). The MODE pin is held HIGH to provide verification capability. The MODE pin should be terminated to GND through a 10k $\Omega$  resistor so that the MODE pin can be pulled HIGH when required.

#### **NC, No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

#### **PRA, I/O**

#### **PRB, I/OProbe A/B**

The Probe pin is used to output data from any user-defined design node within the device. Each diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. The Probe pin is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

#### **QCLKA/B/C/D, I/O Quadrant Clock**

Quadrant clock inputs for A42MX36 devices. When not used as a register control signal, these pins can function as user I/Os.

#### **SDI, I/O Serial Data Input**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

#### **SDO, I/O Serial Data Output**

Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. SDO is available for 42MX devices only.

When Silicon Explorer II is being used, SDO will act as an output while the "checksum" command is run. It will return to user I/O when "checksum" is complete.

#### **TCK, I/O Test Clock**

**Table 47 • PL44**

<b>PL44</b>		
<b>Pin Number</b>	<b>A40MX02 Function</b>	<b>A40MX04 Function</b>
21	GND	GND
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	VCC	VCC
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	CLK, I/O	CLK, I/O
34	MODE	MODE
35	VCC	VCC
36	SDI, I/O	SDI, I/O
37	DCLK, I/O	DCLK, I/O
38	PRA, I/O	PRA, I/O
39	PRB, I/O	PRB, I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	GND	GND
44	I/O	I/O

Figure 39 • PL68

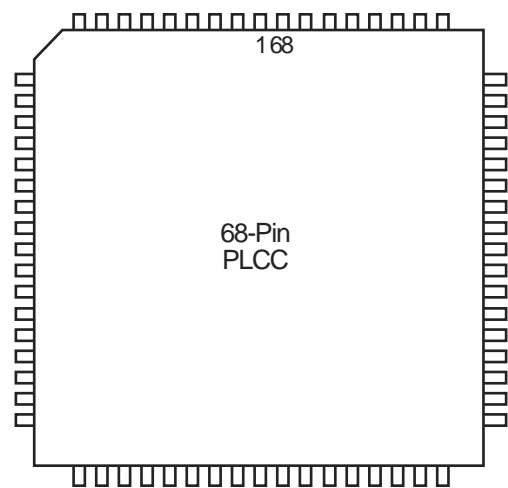


Table 48 • PL68

PL68		
Pin Number	A40MX02 Function	A40MX04 Function
1	I/O	I/O
2	I/O	I/O
3	I/O	I/O
4	VCC	VCC
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	GND	GND
15	GND	GND
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	VCC	VCC
22	I/O	I/O
23	I/O	I/O

Table 48 • PL68

PL68		
Pin Number	A40MX02 Function	A40MX04 Function
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	GND	GND
67	I/O	I/O
68	I/O	I/O

Figure 40 • PL84

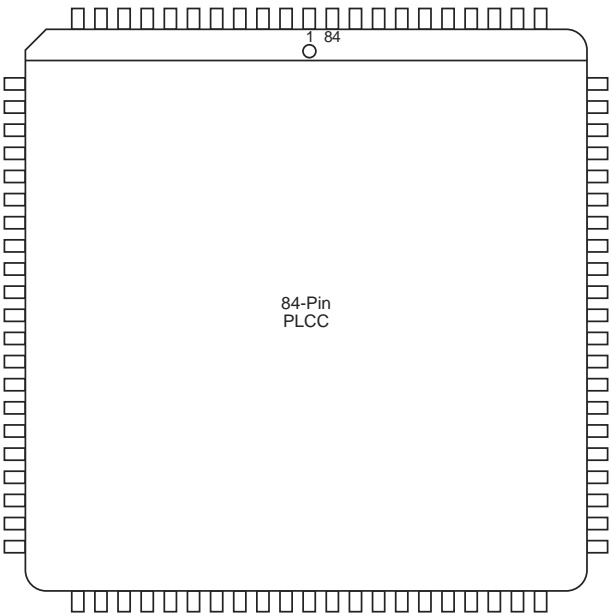


Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	I/O	I/O	I/O	I/O
2	I/O	CLKB, I/O	CLKB, I/O	CLKB, I/O
3	I/O	I/O	I/O	I/O
4	VCC	PRB, I/O	PRB, I/O	PRB, I/O
5	I/O	I/O	I/O	WD, I/O
6	I/O	GND	GND	GND
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	WD, I/O
9	I/O	I/O	I/O	WD, I/O

**Table 50 • PQ 100**

<b>PQ100</b>				
<b>Pin Number</b>	<b>A40MX02 Function</b>	<b>A40MX04 Function</b>	<b>A42MX09 Function</b>	<b>A42MX16 Function</b>
93	VCC	VCC	I/O	I/O
94	VCC	VCC	PRB, I/O	PRB, I/O
95	NC	I/O	I/O	I/O
96	NC	I/O	GND	GND
97	NC	I/O	I/O	I/O
98	SDI, I/O	SDI, I/O	I/O	I/O
99	DCLK, I/O	DCLK, I/O	I/O	I/O
100	PRA, I/O	PRA, I/O	I/O	I/O



**Table 52 • PQ160**

<b>PQ160</b>			
<b>Pin Number</b>	<b>A42MX09 Function</b>	<b>A42MX16 Function</b>	<b>A42MX24 Function</b>
58	VCCI	VCCI	VCCI
59	GND	GND	GND
60	VCCA	VCCA	VCCA
61	LP	LP	LP
62	I/O	I/O	TCK, I/O
63	I/O	I/O	I/O
64	GND	GND	GND
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	I/O	I/O	I/O
69	GND	GND	GND
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	I/O	I/O	I/O
77	NC	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	GND	GND	GND
81	I/O	I/O	I/O
82	SDO, I/O	SDO, I/O	SDO, TDO, I/O
83	I/O	I/O	WD, I/O
84	I/O	I/O	WD, I/O
85	I/O	I/O	I/O
86	NC	VCCI	VCCI
87	I/O	I/O	I/O
88	I/O	I/O	WD, I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O

**Table 53 • PQ208**

<b>PQ208</b>			
<b>Pin Number</b>	<b>A42MX16 Function</b>	<b>A42MX24 Function</b>	<b>A42MX36 Function</b>
21	I/O	I/O	I/O
22	GND	GND	GND
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	GND	GND	GND
28	VCCI	VCCI	VCCI
29	VCCA	VCCA	VCCA
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	VCCA	VCCA	VCCA
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	NC	I/O	I/O
42	NC	I/O	I/O
43	NC	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	NC	I/O	I/O
52	GND	GND	GND
53	GND	GND	GND
54	I/O	TMS, I/O	TMS, I/O
55	I/O	TDI, I/O	TDI, I/O
56	I/O	I/O	I/O
57	I/O	WD, I/O	WD, I/O

**Table 60 • BG272**

<b>BG272</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
D20	I/O
E1	I/O
E2	I/O
E3	I/O
E4	VCCA
E17	VCCI
E18	I/O
E19	I/O
E20	I/O
F1	I/O
F2	I/O
F3	I/O
F4	VCCI
F17	I/O
F18	I/O
F19	I/O
F20	I/O
G1	I/O
G2	I/O
G3	I/O
G4	VCCI
G17	VCCI
G18	I/O
G19	I/O
G20	I/O
H1	I/O
H2	I/O
H3	I/O
H4	VCCA
H17	I/O
H18	I/O
H19	I/O
H20	I/O
J1	I/O
J2	I/O
J3	I/O
J4	VCCI

**Table 60 • BG272**

<b>BG272</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
T19	I/O
T20	I/O
U1	I/O
U2	I/O
U3	I/O
U4	I/O
U5	VCCI
U6	WD, I/O
U7	I/O
U8	I/O
U9	WD, I/O
U10	VCCA
U11	VCCI
U12	I/O
U13	I/O
U14	QCLKB, I/O
U15	I/O
U16	VCCI
U17	I/O
U18	GND
U19	I/O
U20	I/O
V1	I/O
V2	I/O
V3	GND
V4	GND
V5	I/O
V6	I/O
V7	I/O
V8	WD, I/O
V9	I/O
V10	I/O
V11	I/O
V12	I/O
V13	WD, I/O
V14	I/O
V15	WD, I/O

**Table 62 • CQ172**

60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	GND
66	VCC
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	GND
76	I/O
77	I/O
78	I/O
79	I/O
80	VCCI
81	I/O
82	I/O
83	I/O
84	I/O
85	SDO
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	GND