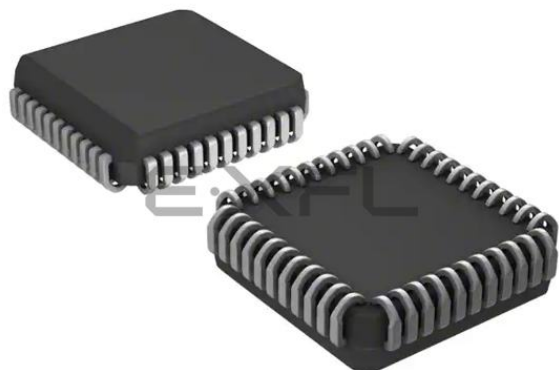




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

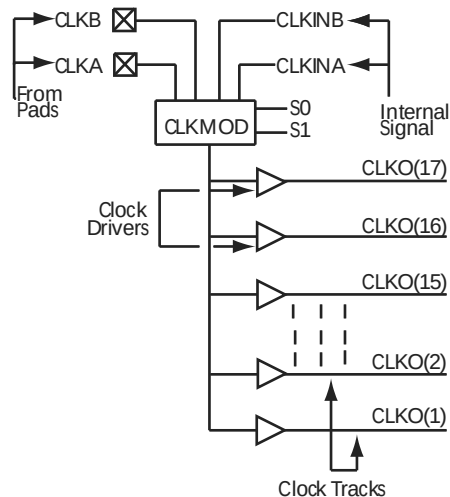
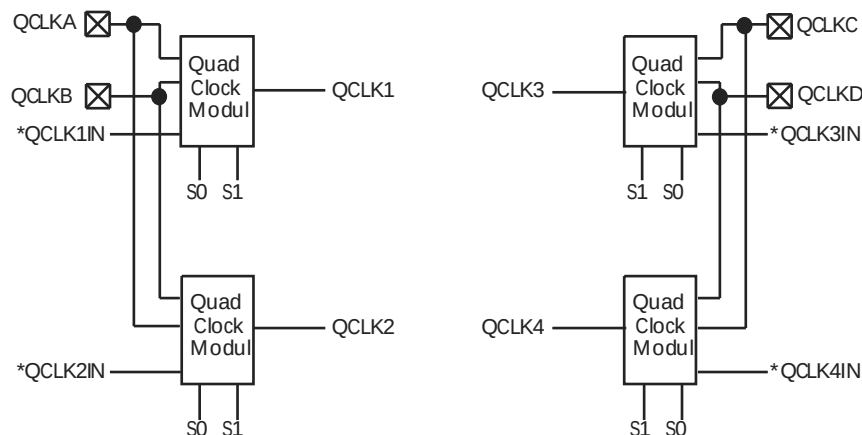
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	34
Number of Gates	6000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-3pl44i

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Figure 8 • Clock Networks of 42MX Devices**Figure 9 • Quadrant Clock Network of A42MX36 Devices**

Note: *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

3.2.5 MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 10, page 12 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (See the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 10, page 12). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. See the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 μ A.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 11, page 12). When the PCI fuse is not programmed, the output drive is standard.

Silicon Sculptor programs devices independently to achieve the fastest programming times possible. After being programmed, each fuse is verified to insure that it has been programmed correctly. Furthermore, at the end of programming, there are integrity tests that are run to ensure no extra fuses have been programmed. Not only does it test fuses (both programmed and non-programmed), Silicon Sculptor also allows self-test to verify its own hardware extensively.

The procedure for programming an MX device using Silicon Sculptor is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via In-House Programming from the factory.

For more details on programming MX devices, see the *AC225: Programming Antifuse Devices* application note and the *Silicon Sculptor 3 Programmers User Guide*.

3.3.4 Power Supply

MX devices are designed to operate in both 5.0V and 3.3V environments. In particular, 42MX devices can operate in mixed 5.0 V/3.3 V systems. The following table describes the voltage support of MX devices.

Table 6 • Voltage Support of MX Devices

Device	VCC	VCCA	VCCI	Maximum Input Tolerance	Nominal Output Voltage
40MX	5.0 V	–	–	5.5 V	5.0 V
	3.3 V	–	–	3.6 V	3.3 V
42MX	–	5.0 V	5.0 V	5.5 V	5.0 V
	–	3.3 V	3.3 V	3.6 V	3.3 V
	–	5.0 V	3.3 V	5.5 V	3.3 V

For A42MX24 and A42MX36 devices the VCCA supply has to be monotonic during power up in order for the POR to issue reset to the JTAG state machine correctly. For more information, see the *AC291: 42MX Family Devices Power-Up Behavior*.

3.3.5 Power-Up/Down in Mixed-Voltage Mode

When powering up 42MX in mixed voltage mode (VCCA = 5.0 V and VCCI = 3.3 V), VCCA must be greater than or equal to VCCI throughout the power-up sequence. If VCCI exceeds VCCA during power-up, one of two things will happen:

- The input protection diode on the I/Os will be forward biased
- The I/Os will be at logical High

In either case, ICC rises to high levels. For power-down, any sequence with VCCA and VCCI can be implemented.

3.3.6 Transient Current

Due to the simultaneous random logic switching activity during power-up, a transient current may appear on the core supply (VCC). Customers must use a regulator for the VCC supply that can source a minimum of 100 mA for transient current during power-up. Failure to provide enough power can prevent the system from powering up properly and result in functional failure. However, there are no reliability concerns, since transient current is distributed across the die instead of confined to a localized spot.

Since the transient current is not due to I/O switching, its value and duration are independent of the VCCI.

- VCCA = Power supply in volts (V)
- F = Switching frequency in megahertz (MHz)

3.4.4 Equivalent Capacitance

Equivalent capacitance is calculated by measuring ICC_{active} at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

3.4.5 C_{EQ} Values for Microsemi MX FPGAs

Modules (C_{EQM}) 3.5

Input Buffers (C_{EQI}) 6.9

Output Buffers (C_{EQO}) 18.2

Routed Array Clock Buffer Loads (C_{EQCR}) 1.4

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. The equation below shows a piece-wise linear summation over all components.

$$\begin{aligned} \text{Power} = & VCCA^2 * [(m \times C_{EQM} * f_m)_{\text{modules}} + (n * C_{EQI} * f_n)_{\text{inputs}} + (p * (C_{EQO} + C_L) * f_p)_{\text{outputs}} + \\ & 0.5 * (q_1 * C_{EQCR} * f_{q1})_{\text{routed_Clk1}} + (r_1 * f_{q1})_{\text{routed_Clk1}} + \\ & 0.5 * (q_2 * C_{EQCR} * f_{q2})_{\text{routed_Clk2}} + (r_2 * f_{q2})_{\text{routed_Clk2}}] \end{aligned} \quad \text{EQ 3}$$

where:

m = Number of logic modules switching at frequency f_m

n = Number of input buffers switching at frequency f_n

p = Number of output buffers switching at frequency f_p

q₁ = Number of clock loads on the first routed array clock

q₂ = Number of clock loads on the second routed array clock

r₁ = Fixed capacitance due to first routed array clock

r₂ = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output load capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi's integrated verification and logic analysis tool. Another tool included in the Libero software is the SmartGen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Microsemi's Libero software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synopsys, and Cadence design systems.

See the Libero IDE web content at www.microsemi.com/soc/products/software/libero/default.aspx for further information on licensing and current operating system support.

3.6 Related Documents

The following sections give the list of related documents which can be referred for this datasheet.

3.6.1 Application Notes

- *AC278: BSDL Files Format Description*
- *AC225: Programming Antifuse Devices*
- *AC168: Implementation of Security in Microsemi Antifuse FPGAs*

3.6.2 User Guides and Manuals

- *Antifuse Macro Library Guide*
- *Silicon Sculptor Programmers User Guide*

3.6.3 Miscellaneous

Libero IDE Flow Diagram

3.7 5.0 V Operating Conditions

The following tables show 5.0 V operating conditions.

Table 12 • Absolute Maximum Ratings for 40MX Devices*

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCC+0.5	V
VO	Output Voltage	–0.5 to VCC+0.5	V
t _{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 13 • Absolute Maximum Ratings for 42MX Devices*

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCCI+0.5	V
VO	Output Voltage	–0.5 to VCCI+0.5	V
t _{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 14 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCA (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V

Note: * Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

3.7.1 5 V TTL Electrical Specifications

The following tables show 5 V TTL electrical specifications.

Table 15 • 5V TTL Electrical Specifications

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	IOH = –10 mA	2.4		2.4						V
	IOH = –4 mA					3.7		3.7		V
VOL ¹	IOL = 10 mA		0.5		0.5					V
	IOL = 6 mA					0.4		0.4		V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX) ²		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL	VIN = 0.5 V		–10		–10		–10		–10	μA
IIH	VIN = 2.7 V		–10		–10		–10		–10	μA
Input Transition Time, T_R and T_F			500		500		500		500	ns
C _{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC ³	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		20		25		25		25	mA
Low power mode Standby Current	42MX devices only		0.5		ICC – 5.0		ICC – 5.0		ICC – 5.0	mA
IIO, I/O source sink current	Can be derived from the <i>IBIS model</i> (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCC/VCCI = min

2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{THL}	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		3.2		3.6		4.0		4.7		6.6	ns
t _{DHL}	Data-to-Pad LOW		2.5		2.7		3.1		3.6		5.1	ns
t _{ENZH}	Enable Pad Z to HIGH		2.7		3.0		3.4		4.0		5.6	ns
t _{ENZL}	Enable Pad Z to LOW		3.0		3.3		3.8		4.4		6.2	ns
t _{ENHZ}	Enable Pad HIGH to Z		5.4		6.0		6.8		8.0		11.2	ns
t _{ENLZ}	Enable Pad LOW to Z		5.0		5.6		6.3		7.4		10.4	ns
t _{GLH}	G-to-Pad HIGH		5.1		5.6		6.4		7.5		10.5	ns
t _{GHL}	G-to-Pad LOW		5.1		5.6		6.4		7.5		10.5	ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.7		6.3		7.1		8.4		11.9	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.0		8.9		10.1		11.9		16.7	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, point and position whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

Table 41 • A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays ¹												
t _{PD1}	Single Module		1.9		2.1		2.4		2.8		4.0	ns
t _{CO}	Sequential Clock-to-Q		2.0		2.2		2.5		3.0		4.2	ns
t _{GO}	Latch G-to-Q		1.9		2.1		2.4		2.8		4.0	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		2.2		2.4		2.8		3.3		4.6	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		1.1		1.2		1.4		1.6		2.3	ns
t _{RD2}	FO = 2 Routing Delay		1.5		1.6		1.8		2.1		3.0	ns
t _{RD3}	FO = 3 Routing Delay		1.8		2.0		2.3		2.7		3.8	ns
t _{RD4}	FO = 4 Routing Delay		2.2		2.4		2.7		3.2		4.5	ns
t _{RD8}	FO = 8 Routing Delay		3.6		4.0		4.5		5.3		7.5	ns

Table 41 • A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description	–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{ACO} Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		11.3		12.5		14.2		16.7		23.3	ns
d _{TLH} Capacitive Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{THL} Capacitive Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

1. For dual-module macros use tPD1 + tRD1 + taped, to + tRD1 + taped, or tPD1 + tRD1 + tusk, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions ¹												
t _{PD}	Internal Array Module Delay	1.2		1.3		1.5		1.8		2.5		ns
t _{PDD}	Internal Decode Module Delay	1.4		1.6		1.8		2.1		3.0		ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay	0.8		0.9		1.0		1.2		1.7		ns
t _{RD2}	FO = 2 Routing Delay	1.0		1.2		1.3		1.5		2.1		ns
t _{RD3}	FO = 3 Routing Delay	1.3		1.4		1.6		1.9		2.6		ns
t _{RD4}	FO = 4 Routing Delay	1.5		1.7		1.9		2.2		3.1		ns
t _{RD5}	FO = 8 Routing Delay	2.4		2.7		3.0		3.6		5.0		ns
Logic Module Sequential Timing ^{3, 4}												
t _{CO}	Flip-Flop Clock-to-Output	1.3		1.4		1.6		1.9		2.7		ns
t _{GO}	Latch Gate-to-Output	1.2		1.3		1.5		1.8		2.5		ns
t _{SUD}	Flip-Flop (Latch) Set-Up Time	0.3		0.4		0.4		0.5		0.7		ns
t _{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RO}	Flip-Flop (Latch) Reset-to-Output	1.4		1.6		1.8		2.1		2.9		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.4		0.5		0.5		0.6		0.8		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.3		6.5		9.0		ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 635	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	2.8		3.2		3.6		4.2		5.9		ns
		FO = 635	3.3		3.7		4.2		4.9		6.9		ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	5.5		6.1		6.6		7.6		12.7		ns
		FO = 635	6.0		6.6		7.2		8.3		13.8		ns
f _{MAX}	Maximum Datapath Frequency	FO = 32		180		164		151		131		79	MHz
		FO = 635		166		151		139		121		73	MHz
TTL Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH			2.6		2.8		3.2		3.8		5.3	ns
t _{DHL}	Data-to-Pad LOW			3.0		3.3		3.7		4.4		6.2	ns
t _{ENZH}	Enable Pad Z to HIGH			2.7		3.0		3.3		3.9		5.5	ns
t _{ENZL}	Enable Pad Z to LOW			3.0		3.3		3.7		4.3		6.1	ns
t _{ENHZ}	Enable Pad HIGH to Z			5.3		5.8		6.6		7.8		10.9	ns

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{ACO} Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.9		12.1		13.7		16.1		22.5	ns
d _{TLH} Capacitive Loading, LOW to HIGH		0.10		0.11		0.12		0.14		0.20	ns/pF
d _{THL} Capacitive Loading, HIGH to LOW		0.10		0.11		0.12		0.14		0.20	ns/pF
CMOS Output Module Timing⁵											
t _{DLH} Data-to-Pad HIGH		4.9		5.5		6.2		7.3		10.3	ns
t _{DHL} Data-to-Pad LOW		3.4		3.8		4.3		5.1		7.1	ns
t _{ENZH} Enable Pad Z to HIGH		3.7		4.1		4.7		5.5		7.7	ns
t _{ENZL} Enable Pad Z to LOW		4.1		4.6		5.2		6.1		8.5	ns
t _{ENHZ} Enable Pad HIGH to Z		7.4		8.2		9.3		10.9		15.3	ns
t _{ENLZ} Enable Pad LOW to Z		6.9		7.6		8.7		10.2		14.3	ns
t _{GLH} G-to-Pad HIGH		7.0		7.8		8.9		10.4		14.6	ns
t _{GHL} G-to-Pad LOW		7.0		7.8		8.9		10.4		14.6	ns
t _{LSU} I/O Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t _{LH} I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO} I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.9		8.8		10.0		11.8		16.5	ns

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

3.12 Pin Descriptions

This section lists the pin descriptions for 40MX and 42MX series FPGAs.

CLK/A/B, I/O Global Clock

Clock inputs for clock distribution networks. CLK is for 40MX while CLKA and CLKB are for 42MX devices. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK, I/O Diagnostic Clock

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND, Ground

Input LOW supply voltage.

I/O, Input/Output

Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
10	I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O
11	I/O	I/O	I/O	I/O
12	NC	MODE	MODE	MODE
13	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	I/O	I/O	I/O	I/O
18	GND	I/O	I/O	I/O
19	GND	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	VCCA	VCCI	VCCI
23	I/O	VCCI	VCCA	VCCA
24	I/O	I/O	I/O	I/O
25	VCC	I/O	I/O	I/O
26	VCC	I/O	I/O	I/O
27	I/O	I/O	I/O	I/O
28	I/O	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	I/O	I/O	I/O	I/O
31	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	VCC	I/O	I/O	I/O
34	I/O	I/O	I/O	TMS, I/O
35	I/O	I/O	I/O	TDI, I/O
36	I/O	I/O	I/O	WD, I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	WD, I/O
39	I/O	I/O	I/O	WD, I/O
40	GND	I/O	I/O	I/O
41	I/O	I/O	I/O	I/O
42	I/O	I/O	I/O	I/O
43	I/O	VCCA	VCCA	VCCA
44	I/O	I/O	I/O	WD, I/O
45	I/O	I/O	I/O	WD, I/O
46	VCC	I/O	I/O	WD, I/O

Table 50 • PQ 100

PQ100				
Pin Number	A40MX02 Function	A40MX04 Function	A42MX09 Function	A42MX16 Function
56	VCC	VCC	I/O	I/O
57	I/O	I/O	GND	GND
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	I/O	I/O	I/O	I/O
61	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	GND	GND	I/O	I/O
64	I/O	I/O	LP	LP
65	I/O	I/O	VCCA	VCCA
66	I/O	I/O	VCCI	VCCI
67	I/O	I/O	VCCA	VCCA
68	I/O	I/O	I/O	I/O
69	VCC	VCC	I/O	I/O
70	I/O	I/O	I/O	I/O
71	I/O	I/O	I/O	I/O
72	I/O	I/O	GND	GND
73	I/O	I/O	I/O	I/O
74	I/O	I/O	I/O	I/O
75	I/O	I/O	I/O	I/O
76	I/O	I/O	I/O	I/O
77	NC	NC	I/O	I/O
78	NC	NC	I/O	I/O
79	NC	NC	SDI, I/O	SDI, I/O
80	NC	I/O	I/O	I/O
81	NC	I/O	I/O	I/O
82	NC	I/O	I/O	I/O
83	I/O	I/O	I/O	I/O
84	I/O	I/O	GND	GND
85	I/O	I/O	I/O	I/O
86	GND	GND	I/O	I/O
87	GND	GND	PRA, I/O	PRA, I/O
88	I/O	I/O	I/O	I/O
89	I/O	I/O	CLKA, I/O	CLKA, I/O
90	CLK, I/O	CLK, I/O	VCCA	VCCA
91	I/O	I/O	I/O	I/O
92	MODE	MODE	CLKB, I/O	CLKB, I/O

Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
117	GNDI
118	NC
119	I/O
120	I/O
121	I/O
122	I/O
123	PROBA
124	I/O
125	CLKA
126	VCC
127	VCCI
128	NC
129	I/O
130	CLKB
131	I/O
132	PROBB
133	I/O
134	I/O
135	I/O
136	GND
137	GNDI
138	NC
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	DCLK

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
21	I/O	I/O	I/O
22	GND	GND	GND
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	GND	GND	GND
28	VCCI	VCCI	VCCI
29	VCCA	VCCA	VCCA
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	VCCA	VCCA	VCCA
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	NC	I/O	I/O
42	NC	I/O	I/O
43	NC	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	NC	I/O	I/O
52	GND	GND	GND
53	GND	GND	GND
54	I/O	TMS, I/O	TMS, I/O
55	I/O	TDI, I/O	TDI, I/O
56	I/O	I/O	I/O
57	I/O	WD, I/O	WD, I/O

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
169	I/O	WD, I/O	WD, I/O
170	I/O	I/O	I/O
171	NC	I/O	QCLKD, I/O
172	I/O	I/O	I/O
173	I/O	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	I/O	WD, I/O	WD, I/O
177	I/O	WD, I/O	WD, I/O
178	PRA, I/O	PRA, I/O	PRA, I/O
179	I/O	I/O	I/O
180	CLKA, I/O	CLKA, I/O	CLKA, I/O
181	NC	I/O	I/O
182	NC	VCCI	VCCI
183	VCCA	VCCA	VCCA
184	GND	GND	GND
185	I/O	I/O	I/O
186	CLKB, I/O	CLKB, I/O	CLKB, I/O
187	I/O	I/O	I/O
188	PRB, I/O	PRB, I/O	PRB, I/O
189	I/O	I/O	I/O
190	I/O	WD, I/O	WD, I/O
191	I/O	WD, I/O	WD, I/O
192	I/O	I/O	I/O
193	NC	I/O	I/O
194	NC	WD, I/O	WD, I/O
195	NC	WD, I/O	WD, I/O
196	I/O	I/O	QCLKC, I/O
197	NC	I/O	I/O
198	I/O	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	NC	I/O	I/O
202	VCCI	VCCI	VCCI
203	I/O	WD, I/O	WD, I/O
204	I/O	WD, I/O	WD, I/O
205	I/O	I/O	I/O

Table 55 • VQ80

VQ80		
Pin Number	A40MX02 Function	A40MX04 Function
49	I/O	I/O
50	CLK, I/O	CLK, I/O
51	I/O	I/O
52	MODE	MODE
53	VCC	VCC
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	GND	GND
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	VCC	VCC
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
A6	I/O
A7	WD, I/O
A8	WD, I/O
A9	I/O
A10	I/O
A11	CLKA
A12	I/O
A13	I/O
A14	I/O
A15	I/O
A16	WD, I/O
A17	I/O
A18	I/O
A19	GND
A20	GND
B1	GND
B2	GND
B3	DCLK, I/O
B4	I/O
B5	I/O
B6	I/O
B7	WD, I/O
B8	I/O
B9	PRB, I/O
B10	I/O
B11	I/O
B12	WD, I/O
B13	I/O
B14	I/O
B15	WD, I/O
B16	I/O
B17	WD, I/O
B18	I/O
B19	GND
B20	GND
C1	I/O
C2	MODE

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
M10	GND
M11	GND
M12	GND
M17	I/O
M18	I/O
M19	I/O
M20	I/O
N1	I/O
N2	I/O
N3	I/O
N4	VCCI
N17	VCCI
N18	I/O
N19	I/O
N20	I/O
P1	I/O
P2	I/O
P3	I/O
P4	VCCA
P17	I/O
P18	I/O
P19	I/O
P20	I/O
R1	I/O
R2	I/O
R3	I/O
R4	VCCI
R17	VCCI
R18	I/O
R19	I/O
R20	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T17	VCCA
T18	I/O

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
Y13	I/O
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	WD, I/O
Y19	GND
Y20	GND

Figure 52 • PG132

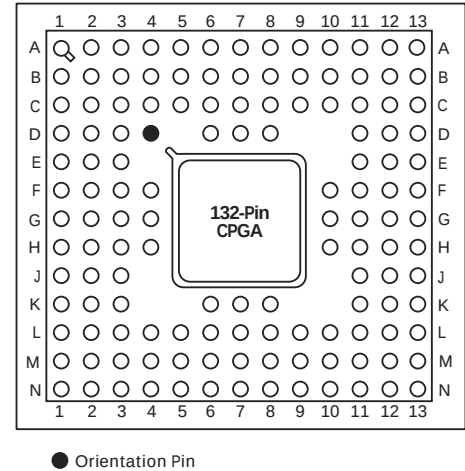


Table 61 • PG132

PG132	
Pin Number	A42MX09 Function
–	PMPOUT
B2	I/O
A1	MODE
B1	I/O
D3	I/O
C2	I/O
C1	I/O
D2	I/O
D1	I/O
E2	I/O
E1	I/O
F3	I/O