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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	6000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-fplg84

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2.6 Temperature Grade Offerings

Table 4 • Temperature Grade Offerings

Package	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PLCC 44	C, I, M	C, I, M				
PLCC 68	C, I, A, M	C, I, M				
PLCC 84		C, I, A, M	C, I, A, M	C, I, M	C, I, M	
PQFP 100	C, I, A, M	C, I, A, M	C, I, A, M	C, I, M		
PQFP 144			C			
PQFP 160			C, I, A, M	C, I, M	C, I, A, M	
PQFP 208				C, I, A, M	C, I, A, M	C, I, A, M
PQFP 240						C, I, A, M
VQFP 80	C, I, A, M	C, I, A, M				
VQFP 100			C, I, A, M	C, I, A, M		
TQFP 176			C, I, A, M	C, I, A, M	C, I, A, M	
PBGA 272						C, I, M
CQFP 172				C, M, B		
CQFP 208						C, M, B
CQFP 256						C, M, B
CPGA 132			C, M, B			

Note: C = Commercial
 I = Industrial
 A = Automotive
 M = Military
 B = MIL-STD-883 Class B

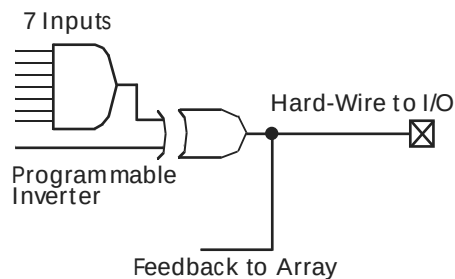
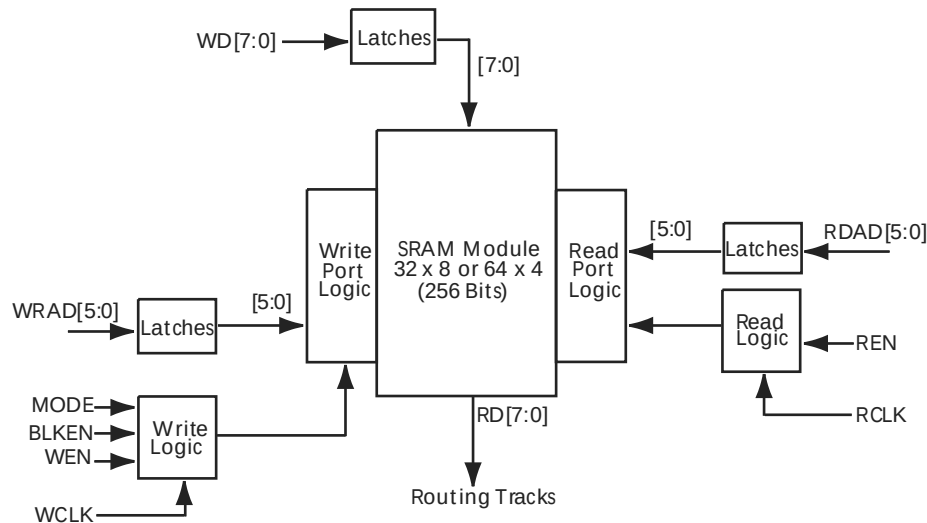
2.7 Speed Grade Offerings

Table 5 • Speed Grade Offerings

	– F	Std	–1	–2	–3
C	P	P	P	P	P
I		P	P	P	P
A		P			
M		P	P		
B		P	P		

Note: See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local *Microsemi Sales representative* for device availability.

Figure 5 • A42MX24 and A42MX36 D-Module Implementation**Figure 6 • A42MX36 Dual-Port SRAM Block**

3.2.3 Routing Structure

The MX architecture uses vertical and horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may be continuous or split into segments. Varying segment lengths allow the interconnect of over 90% of design tracks to occur with only two antifuse connections. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

3.2.3.1 Horizontal Routing

Horizontal routing tracks span the whole row length or are divided into multiple segments and are located in between the rows of modules. Any segment that spans more than one-third of the row length is considered a long horizontal segment. A typical channel is shown in Figure 7, page 10. Within horizontal routing, dedicated routing tracks are used for global clock networks and for power and ground tie-off tracks. Non-dedicated tracks are used for signal nets.

3.2.3.2 Vertical Routing

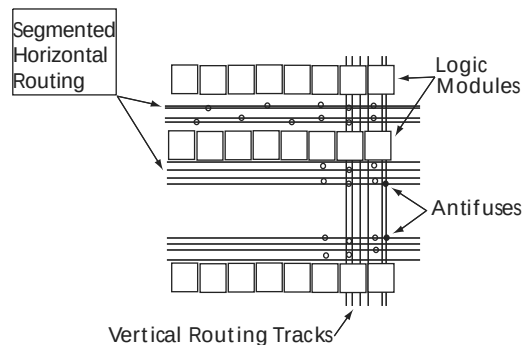
Another set of routing tracks run vertically through the module. There are three types of vertical tracks: input, output, and long. Long tracks span the column length of the module, and can be divided into multiple segments. Each segment in an input track is dedicated to the input of a particular module; each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing.

Each output segment spans four channels (two above and two below), except near the top and bottom of the array, where edge effects occur. Long vertical tracks contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 7, page 10.

3.2.3.3 Antifuse Structures

An antifuse is a “normally open” structure. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient programming algorithms. There are no pre-existing connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For instance, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Figure 7 • MX Routing Structure



3.2.4 Clock Networks

The 40MX devices have one global clock distribution network (CLK). A signal can be put on the CLK network by being routed through the CLKBUF buffer.

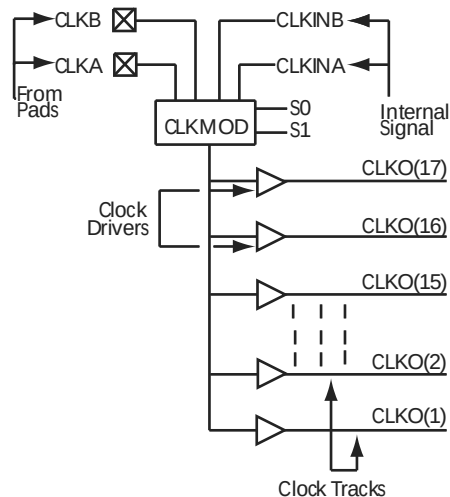
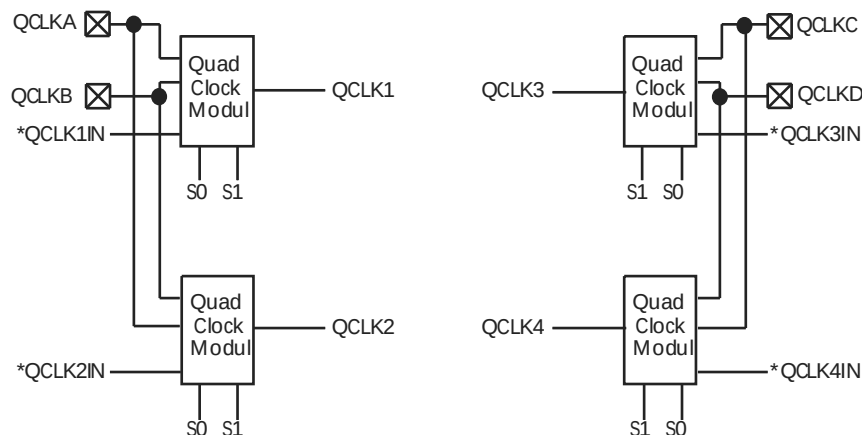
In 42MX devices, there are two low-skew, high-fanout clock distribution networks, referred to as CLKA and CLKB. Each network has a clock module (CLKMOD) that can select the source of the clock signal from any of the following (Figure 8, page 11):

- Externally from the CLKA pad, using CLKBUF buffer
- Externally from the CLKB pad, using CLKBUF buffer
- Internally from the CLKINTA input, using CLKINT buffer
- Internally from the CLKINTB input, using CLKINT buffer

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

Clock input pads in both 40MX and 42MX devices can also be used as normal I/Os, bypassing the clock networks.

The A42MX36 device has four additional register control resources, called quadrant clock networks (Figure 9, page 11). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

Figure 8 • Clock Networks of 42MX Devices**Figure 9 • Quadrant Clock Network of A42MX36 Devices**

Note: *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

3.2.5 MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 10, page 12 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (See the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 10, page 12). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. See the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 μ A.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 11, page 12). When the PCI fuse is not programmed, the output drive is standard.

Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary-scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

Figure 14 • 42MX IEEE 1149.1 Boundary Scan Circuitry

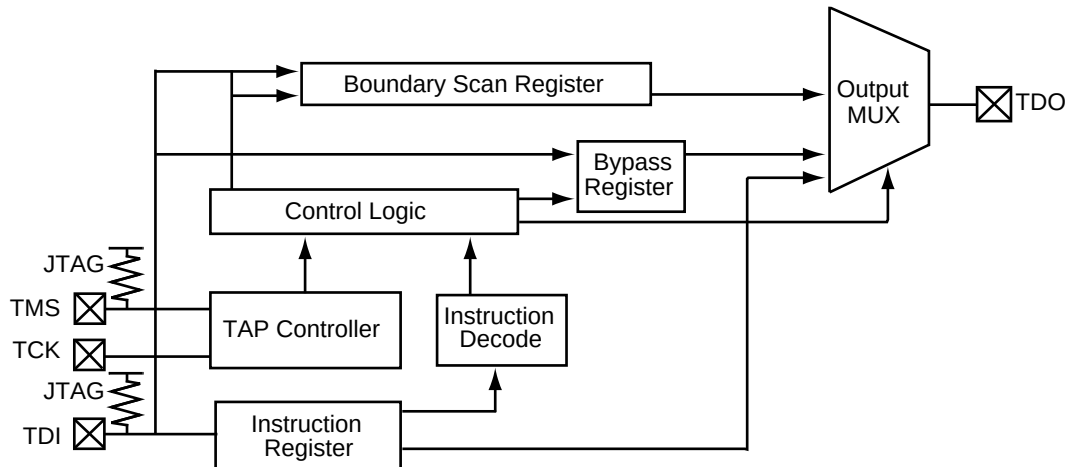


Table 9 • Test Access Port Descriptions

Port	Description
TMS (Test Mode Select)	Serial input for the test logic control bits. Data is captured on the rising edge of the test logic clock (TCK).
TCK (Test Clock Input)	Dedicated test logic clock used serially to shift test instruction, test data, and control inputs on the rising edge of the clock, and serially to shift the output data on the falling edge of the clock. The maximum clock frequency for TCK is 20 MHz.
TDI (Test Data Input)	Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock.
TDO (Test Data Output)	Serial output for test instruction and data from the test logic. TDO is set to an Inactive Drive state (high impedance) when data scanning is not in progress.

Table 10 • Supported BST Public Instructions

Instruction	IR Code (IR2.IR0)	Instruction Type	Description
EXTEST	000	Mandatory	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
SAMPLE/PRELOAD	001	Mandatory	Allows a snapshot of the signals at the device pins to be captured and examined during operation
HIGH Z	101	Optional	Tristates all I/Os to allow external signals to drive pins. See the IEEE Standard 1149.1 specification.
CLAMP	110	Optional	Allows state of signals driven from component pins to be determined from the Boundary-Scan Register. See the IEEE Standard 1149.1 specification for details.
BYPASS	111	Mandatory	Enables the bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the test chain.

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 14 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCA (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V

Note: * Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

3.7.1 5 V TTL Electrical Specifications

The following tables show 5 V TTL electrical specifications.

Table 15 • 5V TTL Electrical Specifications

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	IOH = –10 mA	2.4		2.4						V
	IOH = –4 mA					3.7		3.7		V
VOL ¹	IOL = 10 mA		0.5		0.5					V
	IOL = 6 mA					0.4		0.4		V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX) ²		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL	VIN = 0.5 V		–10		–10		–10		–10	μA
IIH	VIN = 2.7 V		–10		–10		–10		–10	μA
Input Transition Time, T_R and T_F			500		500		500		500	ns
C _{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC ³	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		20		25		25		25	mA
Low power mode Standby Current	42MX devices only		0.5		ICC – 5.0		ICC – 5.0		ICC – 5.0	mA
IIO, I/O source sink current	Can be derived from the <i>IBIS model</i> (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCC/VCCI = min

2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

3.9.3 Output Drive Characteristics for 3.3 V PCI Signaling

Table 25 • DC Specification (3.3 V PCI Signaling)¹

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
VCCI	Supply Voltage for I/Os		3.0	3.6	3.0	3.6 ²	V
VIH	Input High Voltage		0.5	VCC + 0.5	0.5	VCCI + 0.3	V
VIL	Input Low Voltage		−0.5	0.8	−0.3	0.8	V
IIH	Input High Leakage Current	VIN = 2.7 V		70		10	μA
IIL	Input Leakage Current			−70		−10	μA
VOH	Output High Voltage	IOUT = −2 mA	0.9		3.3		V
VOL	Output Low Voltage	IOUT = 3 mA, 6 mA		0.1		0.1 VCCI	V
CIN	Input Pin Capacitance			10		10	pF
CLK	CLK Pin Capacitance		5	12		10	pF
L _{PIN}	Pin Inductance			20		< 8 nH ³	nH

1. PCI Local Bus Specification, Version 2.1, Section 4.2.2.1.

2. Maximum rating for VCCI −0.5 V to 7.0V.

3. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

Table 26 • AC Specifications for (3.3 V PCI Signaling)*

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
ICL	Low Clamp Current	−5 < VIN ≤ −1	−25 + (VIN + 1) / 0.015		−60	−10	mA
Slew (r)	Output Rise Slew Rate	0.2 V to 0.6 V load	1	4	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	0.6 V to 0.2 V load	1	4	2.8	4.0	V/ns

Note: *PCI Local Bus Specification, Version 2.1, Section 4.2.2.2.

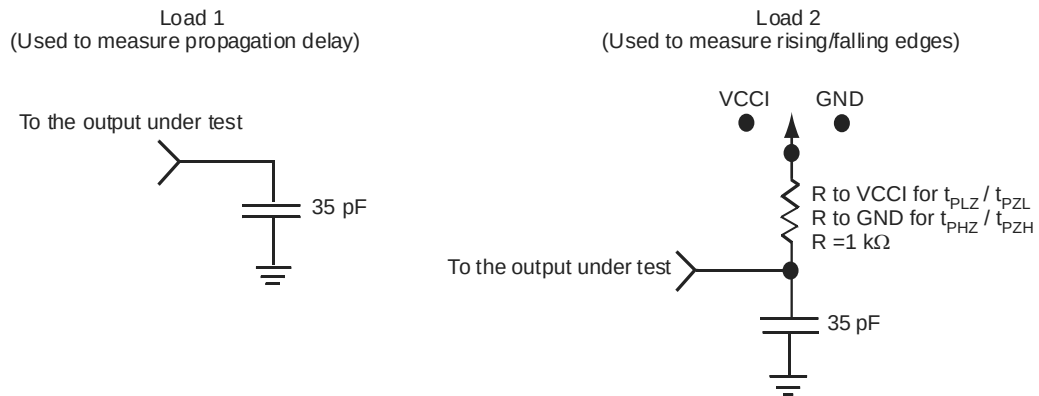
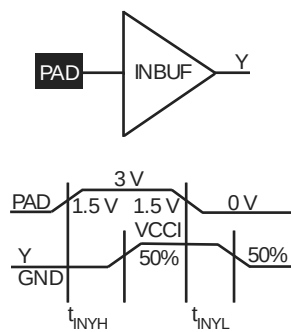
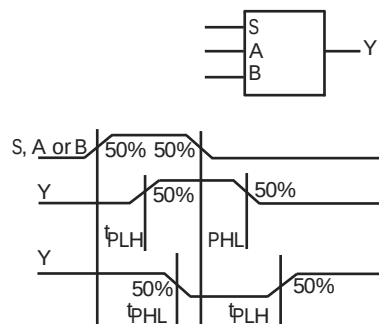
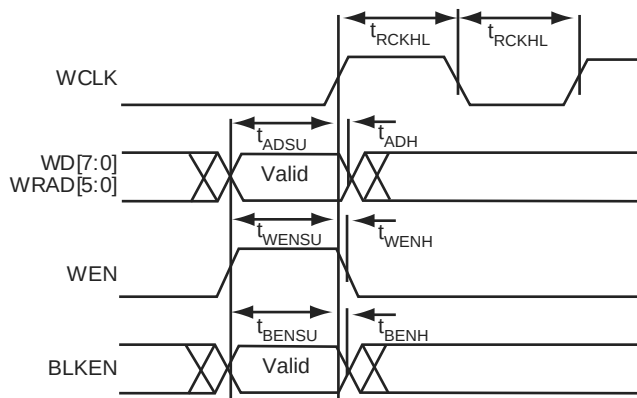
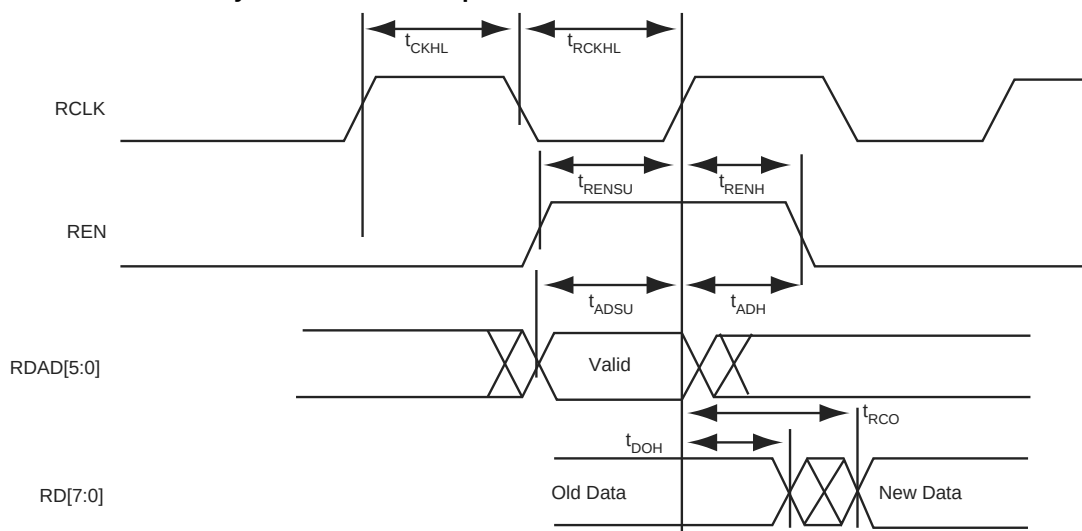
Figure 22 • AC Test Loads**Figure 23 • Input Buffer Delays****Figure 24 • Module Delays**

Figure 30 • 42MX SRAM Write Operation

Note: Identical timing for falling edge clock

Figure 31 • 42MX SRAM Synchronous Read Operation

Note: Identical timing for falling edge clock

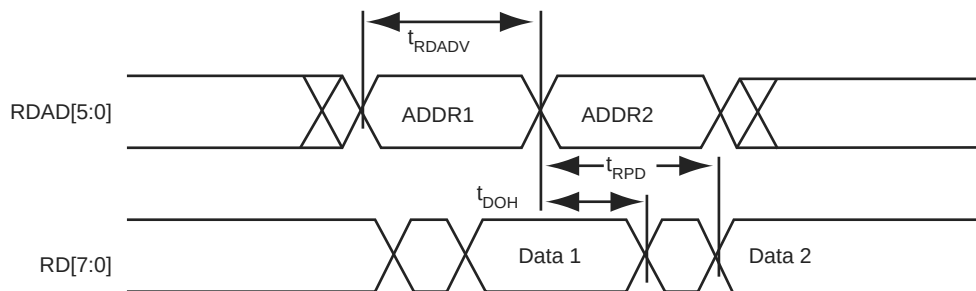
Figure 32 • 42MX SRAM Asynchronous Read Operation—Type 1 (Read Address Controlled)

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RD1}	FO = 1 Routing Delay		2.0		2.2		2.5		3.0		4.2	ns
t _{RD2}	FO = 2 Routing Delay		2.7		3.1		3.5		4.1		5.7	ns
t _{RD3}	FO = 3 Routing Delay		3.4		3.9		4.4		5.2		7.3	ns
t _{RD4}	FO = 4 Routing Delay		4.2		4.8		5.4		6.3		8.9	ns
t _{RD8}	FO = 8 Routing Delay		7.1		8.2		9.2		10.9		15.2	ns
Logic Module Sequential Timing²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		4.3		4.9		5.6		6.6		9.2	ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		4.3		4.9		5.6		6.6		9.2	ns
t _{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		4.6		5.3		6.0		7.0		9.8	ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		4.6		5.3		6.0		7.0		9.8	ns
t _A	Flip-Flop Clock Input Period		6.8		7.8		8.9		10.4		14.6	ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		109		101		92		80		48	MHz
Input Module Propagation Delays												
t _{INYH}	Pad-to-Y HIGH		1.0		1.1		1.3		1.5		2.1	ns
t _{INYL}	Pad-to-Y LOW		0.9		1.0		1.1		1.3		1.9	ns
Input Module Predicted Routing Delays¹												
t _{IRD1}	FO = 1 Routing Delay		2.9		3.4		3.8		4.5		6.3	ns
t _{IRD2}	FO = 2 Routing Delay		3.6		4.2		4.8		5.6		7.8	ns
t _{IRD3}	FO = 3 Routing Delay		4.4		5.0		5.7		6.7		9.4	ns
t _{IRD4}	FO = 4 Routing Delay		5.1		5.9		6.7		7.8		11.0	ns
t _{IRD8}	FO = 8 Routing Delay		8.0		9.26		10.5		12.6		17.3	ns
Global Clock Network												
t _{CKH}	Input LOW to HIGH	FO = 16	6.4		7.4		8.3		9.8		13.7	ns
		FO = 128	6.4		7.4		8.3		9.8		13.7	
t _{CKL}	Input HIGH to LOW	FO = 16	6.7		7.8		8.8		10.4		14.5	ns
		FO = 128	6.7		7.8		8.8		10.4		14.5	
t _{PWH}	Minimum Pulse Width HIGH	FO = 16	3.1		3.6		4.1		4.8		6.7	ns
		FO = 128	3.3		3.8		4.3		5.1		7.1	
t _{PWL}	Minimum Pulse Width LOW	FO = 16	3.1		3.6		4.1		4.8		6.7	ns
		FO = 128	3.3		3.8		4.3		5.1		7.1	
t _{CKSW}	Maximum Skew	FO = 16	0.6		0.6		0.7		0.8		1.2	ns
		FO = 128	0.8		0.9		1.0		1.2		1.6	

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH	5.5		6.4		7.2		8.5		11.9		ns
t _{DHL}	Data-to-Pad LOW	4.8		5.5		6.2		7.3		10.2		ns
t _{ENZH}	Enable Pad Z to HIGH	4.7		5.5		6.2		7.3		10.2		ns
t _{ENZL}	Enable Pad Z to LOW	6.8		7.9		8.9		10.5		14.7		ns
t _{ENHZ}	Enable Pad HIGH to Z	11.1		12.8		14.5		17.1		23.9		ns
t _{ENLZ}	Enable Pad LOW to Z	8.2		9.5		10.7		12.6		17.7		ns
d _{TLH}	Delta LOW to HIGH	0.05		0.05		0.06		0.07		0.10		ns/pF
d _{THL}	Delta HIGH to LOW	0.03		0.03		0.04		0.04		0.06		ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro
4. Delays based on 35 pF loading

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t _{PD2}	Dual-Module Macros		2.3		3.1		3.5		4.1		5.7	ns
t _{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays ¹												
t _{RD1}	FO = 1 Routing Delay		1.2		1.6		1.8		2.1		3.0	ns
t _{RD2}	FO = 2 Routing Delay		1.9		2.2		2.5		2.9		4.1	ns
t _{RD3}	FO = 3 Routing Delay		2.4		2.8		3.2		3.7		5.2	ns
t _{RD4}	FO = 4 Routing Delay		2.9		3.4		3.9		4.5		6.3	ns
t _{RD8}	FO = 8 Routing Delay		5.0		5.8		6.6		7.8		10.9	ns
Logic Module Sequential Timing ²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		3.1		3.5		4.0		4.7		6.6	ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		3.1		3.5		4.0		4.7		6.6	ns

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RD3}	FO = 3 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t _{RD4}	FO = 4 Routing Delay		1.6		1.7		2.0		2.3		3.2	ns
t _{RD8}	FO = 8 Routing Delay		2.6		2.9		3.2		3.8		5.3	ns
Logic Module Sequential Timing^{3,4}												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		0.3		0.4		0.4		0.5		0.7	ns
t _{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		0.7		0.8		0.9		1.0		1.4	ns
t _{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		3.4		3.8		4.3		5.0		7.1	ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		4.5		5.0		5.6		6.6		9.2	ns
t _A	Flip-Flop Clock Input Period		6.8		7.6		8.6		10.1		14.1	ns
t _{INH}	Input Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{INSU}	Input Buffer Latch Set-Up		0.5		0.5		0.6		0.7		1.0	ns
t _{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{OUTSU}	Output Buffer Latch Set-Up		0.5		0.5		0.6		0.7		1.0	ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency		215		195		179		156		94	MHz
Input Module Propagation Delays												
t _{INYH}	Pad-to-Y HIGH		1.1		1.2		1.3		1.6		2.2	ns
t _{INYL}	Pad-to-Y LOW		0.8		0.9		1.0		1.2		1.7	ns
t _{INGH}	G to Y HIGH		1.4		1.6		1.8		2.1		2.9	ns
t _{INGL}	G to Y LOW		1.4		1.6		1.8		2.1		2.9	ns
Input Module Predicted Routing Delays²												
t _{IRD1}	FO = 1 Routing Delay		1.8		2.0		2.3		2.7		4.0	ns
t _{IRD2}	FO = 2 Routing Delay		2.1		2.3		2.6		3.1		4.3	ns
t _{IRD3}	FO = 3 Routing Delay		2.3		2.6		3.0		3.5		4.9	ns
t _{IRD4}	FO = 4 Routing Delay		2.6		3.0		3.3		3.9		5.4	ns
t _{IRD8}	FO = 8 Routing Delay		3.6		4.0		4.6		5.4		7.5	ns
Global Clock Network												
t _{CKH}	Input LOW to HIGH	FO = 32	2.6		2.9		3.3		3.9		5.4	ns
		FO = 384	2.9		3.2		3.6		4.3		6.0	ns
t _{CKL}	Input HIGH to LOW	FO = 32	3.8		4.2		4.8		5.6		7.8	ns
		FO = 384	4.5		5.0		5.6		6.6		9.2	ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	3.2		3.5		4.0		4.7		6.6	ns
		FO = 384	3.7		4.1		4.6		5.4		7.6	ns

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PWL}	Minimum Pulse Width LOW	FO = 32	3.2		3.5		4.0		4.7		6.6		ns
		FO = 384	3.7		4.1		4.6		5.4		7.6		ns
t _{CKSW}	Maximum Skew	FO = 32		0.3		0.4		0.4		0.5		0.7	ns
		FO = 384		0.3		0.4		0.4		0.5		0.7	ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 384	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	2.8		3.1		5.5		4.1		5.7		ns
		FO = 384	3.2		3.5		4.0		4.7		6.6		ns
t _P	Minimum Period	FO = 32	4.2		4.67		5.1		5.8		9.7		ns
		FO = 384	4.6		5.1		5.6		6.4		10.7		ns
f _{MAX}	Maximum Frequency	FO = 32		237		215		198		172		103	MHz
		FO = 384		215		195		179		156		94	MHz

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵ (Continued)												
t _{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t _{GLH}	G-to-Pad HIGH		2.9		3.3		3.7		4.4		6.1	ns
t _{GHL}	G-to-Pad LOW		2.9		3.3		3.7		4.4		6.1	ns
t _{LSU}	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		3.5		3.9		4.5		5.2		7.3	ns
t _{DHL}	Data-to-Pad LOW		2.5		2.7		3.1		3.6		5.1	ns
t _{ENZH}	Enable Pad Z to HIGH		2.7		3.0		3.3		3.9		5.5	ns
t _{ENZL}	Enable Pad Z to LOW		2.9		3.3		3.7		4.3		6.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		5.3		5.8		6.6		7.8		10.9	ns
t _{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t _{GLH}	G-to-Pad HIGH		5.0		5.6		6.3		7.5		10.4	ns
t _{GHL}	G-to-Pad LOW		5.0		5.6		6.3		7.5		10.4	ns
t _{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions ¹												
t _{PD}	Internal Array Module Delay		1.9		2.1		2.3		2.7		3.8	ns
t _{PDD}	Internal Decode Module Delay		2.2		2.5		2.8		3.3		4.7	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.7	ns
t _{RD2}	FO = 2 Routing Delay		1.8		2.0		2.3		2.7		3.7	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.5		2.8		3.4		4.7	ns
t _{RD4}	FO = 4 Routing Delay		2.8		3.1		3.5		4.1		5.7	ns

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
21	I/O	I/O	I/O
22	GND	GND	GND
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	GND	GND	GND
28	VCCI	VCCI	VCCI
29	VCCA	VCCA	VCCA
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	VCCA	VCCA	VCCA
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	NC	I/O	I/O
42	NC	I/O	I/O
43	NC	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	NC	I/O	I/O
52	GND	GND	GND
53	GND	GND	GND
54	I/O	TMS, I/O	TMS, I/O
55	I/O	TDI, I/O	TDI, I/O
56	I/O	I/O	I/O
57	I/O	WD, I/O	WD, I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
126	WD, I/O
127	I/O
128	VCCI
129	I/O
130	I/O
131	I/O
132	WD, I/O
133	WD, I/O
134	I/O
135	QCLKB, I/O
136	I/O
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	WD, I/O
143	WD, I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	VCCI
151	VCCA
152	GND
153	I/O
154	I/O
155	I/O
156	I/O
157	I/O
158	I/O
159	WD, I/O
160	WD, I/O
161	I/O
162	I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
237	GND
238	MODE
239	VCCA
240	GND

Figure 46 • VQ80

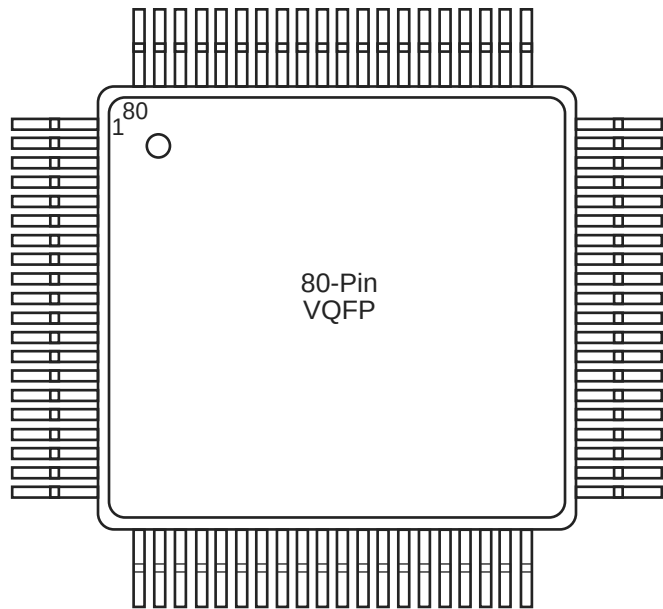


Table 55 • VQ80

VQ80		
Pin Number	A40MX02 Function	A40MX04 Function
1	I/O	I/O
2	NC	I/O
3	NC	I/O
4	NC	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	GND
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O