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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	6000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	80-TQFP
Supplier Device Package	80-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-fvq80

Figures

Figure 1	Ordering Information	3
Figure 2	42MX C-Module Implementation	7
Figure 3	42MX C-Module Implementation	7
Figure 4	42MX S-Module Implementation	8
Figure 5	A42MX24 and A42MX36 D-Module Implementation	9
Figure 6	A42MX36 Dual-Port SRAM Block	9
Figure 7	MX Routing Structure	10
Figure 8	Clock Networks of 42MX Devices	11
Figure 9	Quadrant Clock Network of A42MX36 Devices	11
Figure 10	42MX I/O Module	12
Figure 11	PCI Output Structure of A42MX24 and A42MX36 Devices	12
Figure 12	Silicon Explorer II Setup with 40MX	16
Figure 13	Silicon Explorer II Setup with 42MX	17
Figure 14	42MX IEEE 1149.1 Boundary Scan Circuitry	18
Figure 15	Device Selection Wizard	19
Figure 16	Typical Output Drive Characteristics (Based Upon Measured Data)	28
Figure 17	40MX Timing Model*	30
Figure 18	42MX Timing Model	30
Figure 19	42MX Timing Model (Logic Functions Using Quadrant Clocks)	31
Figure 20	42MX Timing Model (SRAM Functions)	32
Figure 21	Output Buffer Delays	32
Figure 22	AC Test Loads	33
Figure 23	Input Buffer Delays	33
Figure 24	Module Delays	33
Figure 25	Flip-Flops and Latches	34
Figure 26	Input Buffer Latches	34
Figure 27	Output Buffer Latches	35
Figure 28	Decode Module Timing	35
Figure 29	SRAM Timing Characteristics	35
Figure 30	42MX SRAM Write Operation	36
Figure 31	42MX SRAM Synchronous Read Operation	36
Figure 32	42MX SRAM Asynchronous Read Operation—Type 1 (Read Address Controlled)	36
Figure 33	42MX SRAM Asynchronous Read Operation—Type 2 (Write Address Controlled)	37
Figure 34	42MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 5.0\text{ V}$)	38
Figure 35	40MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)	39
Figure 36	42MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$)	39
Figure 37	40MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$)	40
Figure 38	PL44	86
Figure 39	PL68	88
Figure 40	PL84	90
Figure 41	PQ100	93
Figure 42	PQ144	97
Figure 43	PQ160	102
Figure 44	PQ208	107
Figure 45	PQ240	113
Figure 46	VQ80	120
Figure 47	VQ100	123
Figure 48	TQ176	126
Figure 49	CQ208	131
Figure 50	CQ256	138

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- Table 15, page 21 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 22, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 23, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

1.2 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Added CQFP package information for A42MX16 device in Product Profile, page 1 and Ceramic Device Resources, page 4 (SAR 79522).
- Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in Temperature Grade Offerings, page 5 (SAR 79519)
- Changed Silicon Sculptor II to Silicon Sculptor in Programming, page 12 (SAR 38754)
- Added Figure 53, page 158 CQ172 package (SAR 79522).

1.3 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Added Figure 42, page 97 PQ144 Package for A42MX09 device (SAR 69776)
- Added Figure 52, page 153 PQ132 Package for A42MX09 device (SAR 69776)

1.4 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Added information on power-up behavior for A42MX24 and A42MX36 devices to the Power Supply, page 13 (SAR 42096)
- Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793)

1.5 Revision 11.0

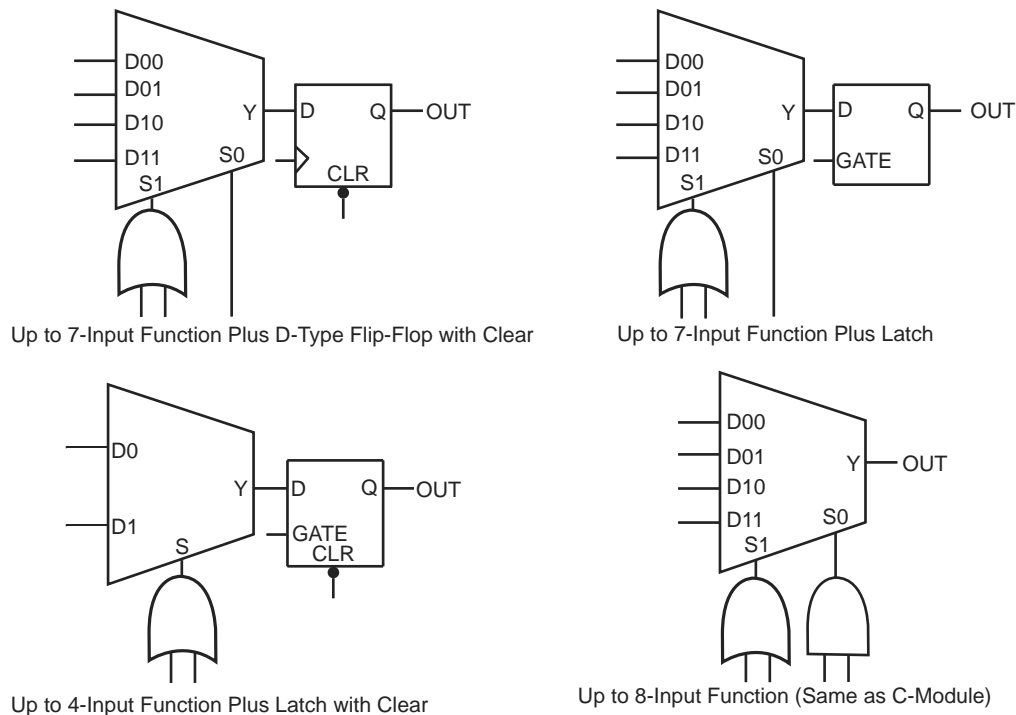
The following is a summary of the changes in revision 11.0 of this document.

- The FuseLock logo and accompanying text was removed from the User Security, page 12. This marking is no longer used on Microsemi devices (PCN 0915)
- The Development Tool Support, page 19 was updated (SAR 38512)

1.6 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- Ordering Information, page 3 was updated to include lead-free package ordering codes (SAR 21968)
- The User Security, page 12 was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673)

Figure 4 • 42MX S-Module Implementation

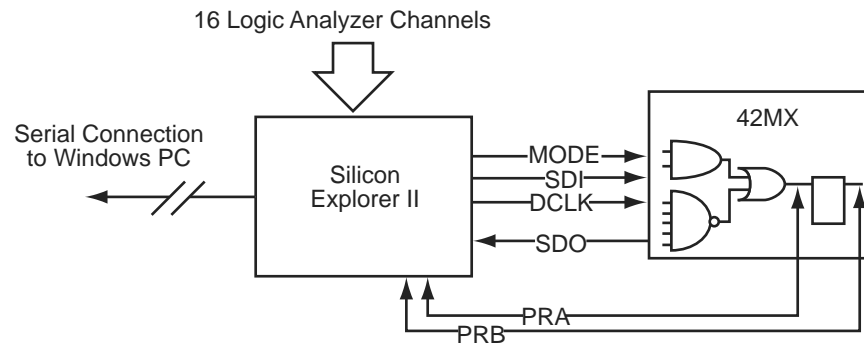
A42MX24 and A42MX36 devices contain D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry, providing a fast, wide-input AND function similar to that found in CPLD architectures (Figure 5, page 9). The D-module allows A42MX24 and A42MX36 devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin, and can also be fed back into the array to be incorporated into other logic.

3.2.2 Dual-Port SRAM Modules

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the A42MX36 dual-port SRAM block is shown in Figure 6, page 9.

The A42MX36 SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]), which are connected to segmented vertical routing tracks.

The A42MX36 dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring FIFO and LIFO queues. The ACTgen Macro Builder within Microsemi's designer software provides capability to quickly design memory functions with the SRAM blocks. Unused SRAM blocks can be used to implement registers for other user logic within the design.

Figure 13 • Silicon Explorer II Setup with 42MX**Table 8 • Device Configuration Options for Probe Capability**

Security Fuse(s) Programmed	Mode	PRA, PRB ¹	SDI, SDO, DCLK ¹
No	LOW	User I/Os ²	User I/Os ²
No	HIGH	Probe Circuit Outputs	Probe Circuit Inputs
Yes	–	Probe Circuit Secured	Probe Circuit Secured

1. Avoid using SDI, SDO, DCLK, PRA and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.
2. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. See the Pin Descriptions, page 83 for information on unused I/O pins

3.4.7 Design Consideration

It is recommended to use a series 70Ω termination resistor on every probe connector (SDI, SDO, MODE, DCLK, PRA and PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

3.4.8 IEEE Standard 1149.1 Boundary Scan Test (BST) Circuitry

42MX24 and 42MX36 devices are compatible with IEEE Standard 1149.1 (informally known as Joint Testing Action Group Standard or JTAG), which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic MX boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers and instruction register (Figure 14, page 18). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and some optional instructions. Table 9, page 18 describes the ports that control JTAG testing, while Table 10, page 18 describes the test instructions supported by these MX devices.

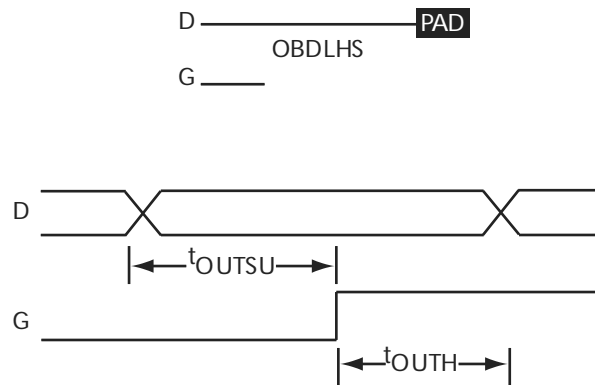
Each test section is accessed through the TAP, which has four associated pins: TCK (test clock input), TDI and TDO (test data input and output), and TMS (test mode selector).

The TAP controller is a four-bit state machine. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles.

42MX24 and 42MX36 devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

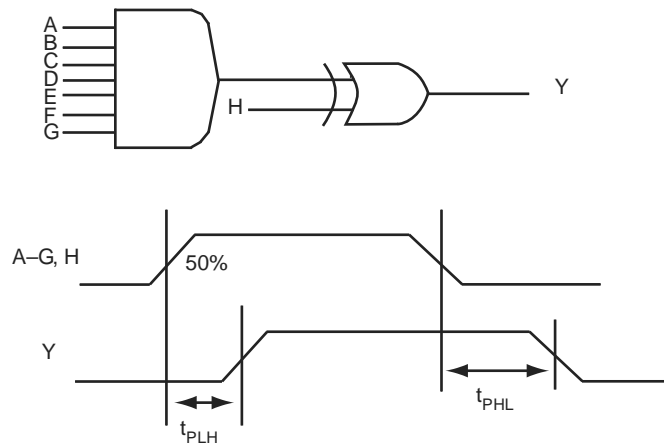
Figure 27 • Output Buffer Latches



3.10.4 Decode Module Timing

The following figure shows decode module timing.

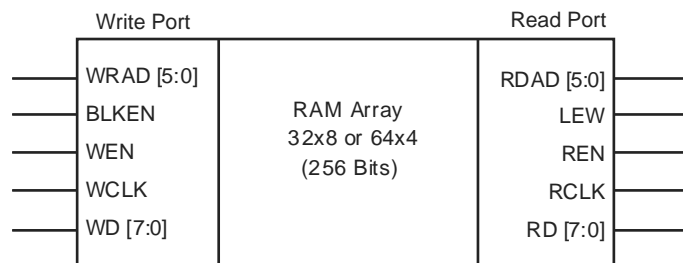
Figure 28 • Decode Module Timing



3.10.5 SRAM Timing Characteristics

The following figure shows SRAM timing characteristics.

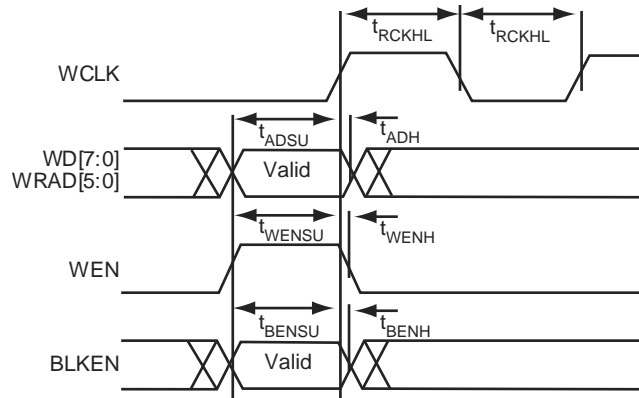
Figure 29 • SRAM Timing Characteristics



3.10.6 Dual-Port SRAM Timing Waveforms

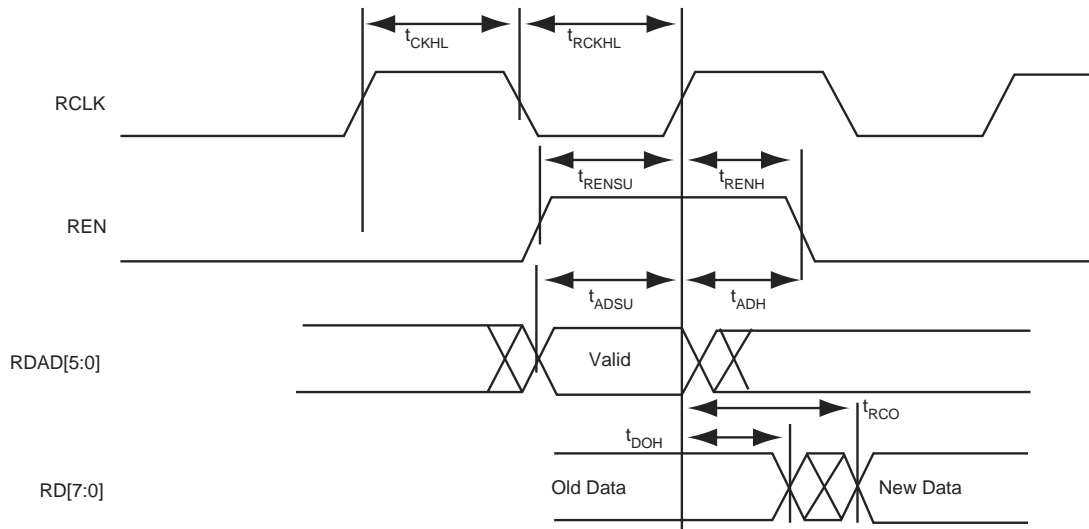
The following figures show dual-port SRAM timing waveforms.

Figure 30 • 42MX SRAM Write Operation



Note: Identical timing for falling edge clock

Figure 31 • 42MX SRAM Synchronous Read Operation



Note: Identical timing for falling edge clock

Figure 32 • 42MX SRAM Asynchronous Read Operation—Type 1 (Read Address Controlled)

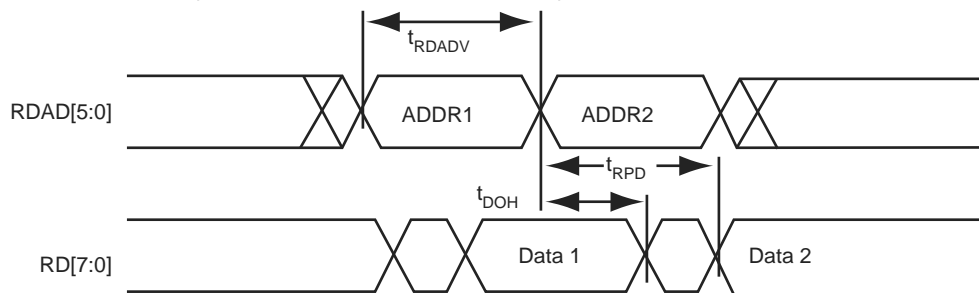
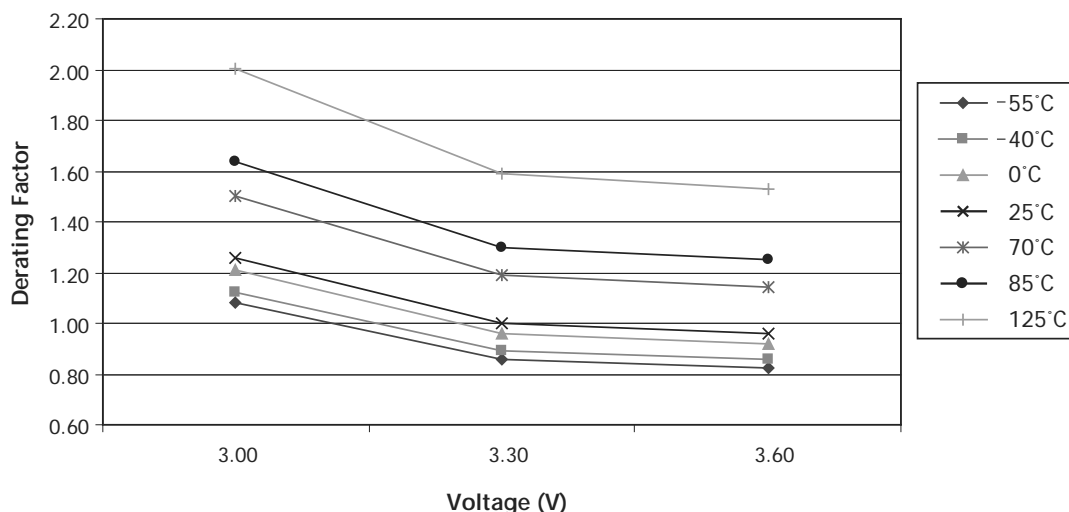


Table 31 • 40MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$)

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
3.60	0.83	0.85	0.92	0.96	1.14	1.25	1.53

Figure 37 • 40MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$)

Note: This derating factor applies to all routing and propagation delays

3.11.5 PCI System Timing Specification

The following tables list the critical PCI timing parameters and the corresponding timing parameters for the MX PCI-compliant devices.

3.11.6 PCI Models

Microsemi provides synthesizable VHDL and Verilog-HDL models for a PCI Target interface, a PCI Target and Target+DMA Master interface. Contact the Microsemi sales representative for more details.

Table 32 • Clock Specification for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Time	30	–	4.0	–	4.0	–	ns
t_{HIGH}	CLK High Time	11	–	1.9	–	1.9	–	ns
t_{LOW}	CLK Low Time	11	–	1.9	–	1.9	–	ns

Table 33 • Timing Parameters for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VAL}	CLK to Signal Valid—Bused Signals	2	11	2.0	9.0	2.0	9.0	ns
$t_{\text{VAL(PTP)}}$	CLK to Signal Valid—Point-to-Point	2 ²	12	2.0	9.0	2.0	9.0	ns
t_{ON}	Float to Active	2	–	2.0	4.0	2.0	4.0	ns
t_{OFF}	Active to Float	–	28	–	8.3 ¹	–	8.3 ¹	ns
t_{SU}	Input Set-Up Time to CLK—Bused Signals	7	–	1.5	–	1.5	–	ns

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t _A	Flip-Flop Clock Input Period	4.8		5.6		6.3		7.5		10.4		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		181		167		154		134		80	MHz
Input Module Propagation Delays												
t _{INYH}	Pad-to-Y HIGH		0.7		0.8		0.9		1.1		1.5	ns
t _{INYL}	Pad-to-Y LOW		0.6		0.7		0.8		1.0		1.3	ns
Input Module Predicted Routing Delays¹												
t _{IRD1}	FO = 1 Routing Delay		2.1		2.4		2.2		3.2		4.5	ns
t _{IRD2}	FO = 2 Routing Delay		2.6		3.0		3.4		4.0		5.6	ns
t _{IRD3}	FO = 3 Routing Delay		3.1		3.6		4.1		4.8		6.7	ns
t _{IRD4}	FO = 4 Routing Delay		3.6		4.2		4.8		5.6		7.8	ns
t _{IRD8}	FO = 8 Routing Delay		5.7		6.6		7.5		8.8		12.4	ns
Global Clock Network												
t _{CKH}	Input Low to HIGH	FO = 16	4.6		5.3		6.0		7.0		9.8	ns
		FO = 128	4.6		5.3		6.0		7.0		9.8	
t _{CKL}	Input High to LOW	FO = 16	4.8		5.6		6.3		7.4		10.4	ns
		FO = 128	4.8		5.6		6.3		7.4		10.4	
t _{PWH}	Minimum Pulse Width HIGH	FO = 16	2.2		2.6		2.9		3.4		4.8	ns
		FO = 128	2.4		2.7		3.1		3.6		5.1	
t _{PWL}	Minimum Pulse Width LOW	FO = 16	2.2		2.6		2.9		3.4		4.8	ns
		FO = 128	2.4		2.7		3.01		3.6		5.1	
t _{CKSW}	Maximum Skew	FO = 16	0.4		0.5		0.5		0.6		0.8	ns
		FO = 128	0.5		0.6		0.7		0.8		1.2	
t _P	Minimum Period	FO = 16	4.7		5.4		6.1		7.2		10.0	ns
		FO = 128	4.8		5.6		6.3		7.5		10.4	
f _{MAX}	Maximum Frequency	FO = 16	188		175		160		139		83	MHz
		FO = 128	181		168		154		134		80	
TTL Output Module Timing⁴												
t _{DLH}	Data-to-Pad HIGH		3.3		3.8		4.3		5.1		7.2	ns
t _{DHL}	Data-to-Pad LOW		4.0		4.6		5.2		6.1		8.6	ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.3		4.9		5.8		8.0	ns
t _{ENZL}	Enable Pad Z to LOW		4.7		5.4		6.1		7.2		10.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.1	ns

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{ENLZ} Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH} Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{THL} Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing¹											
t _{DLH}	Data-to-Pad HIGH	3.9	4.5	5.1	6.05	8.5	ns				
t _{DHL}	Data-to-Pad LOW	3.4	3.9	4.4	5.2	7.3	ns				
t _{ENZH}	Enable Pad Z to HIGH	3.4	3.9	4.4	5.2	7.3	ns				
t _{ENZL}	Enable Pad Z to LOW	4.9	5.6	6.4	7.5	10.5	ns				
t _{ENHZ}	Enable Pad HIGH to Z	7.9	9.1	10.4	12.2	17.0	ns				
t _{ENLZ}	Enable Pad LOW to Z	5.9	6.8	7.7	9.0	12.6	ns				
d _{TLH}	Delta LOW to HIGH	0.03	0.04	0.04	0.05	0.07	ns/pF				
d _{THL}	Delta HIGH to LOW	0.02	0.02	0.03	0.03	0.04	ns/pF				

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer utility from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading

Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays											
t _{PD1}	Single Module	1.7	2.0	2.3	2.7	3.7	ns				
t _{PD2}	Dual-Module Macros	3.7	4.3	4.9	5.7	8.0	ns				
t _{CO}	Sequential Clock-to-Q	1.7	2.0	2.3	2.7	3.7	ns				
t _{GO}	Latch G-to-Q	1.7	2.0	2.3	2.7	3.7	ns				
t _{RS}	Flip-Flop (Latch) Reset-to-Q	1.7	2.0	2.3	2.7	3.7	ns				
Logic Module Predicted Routing Delays¹											
t _{RD1}	FO = 1 Routing Delay	1.9	2.2	2.5	3.0	4.2	ns				
t _{RD2}	FO = 2 Routing Delay	2.7	3.1	3.5	4.1	5.7	ns				
t _{RD3}	FO = 3 Routing Delay	3.4	3.9	4.4	5.2	7.3	ns				
t _{RD4}	FO = 4 Routing Delay	4.1	4.8	5.4	6.3	8.9	ns				
t _{RD8}	FO = 8 Routing Delay	7.1	8.1	9.2	10.9	15.2	ns				
Logic Module Sequential Timing²											
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up	4.3	5.0	5.6	6.6	9.2	ns				
t _{HD} ³	Flip-Flop (Latch) Data Input Hold	0.0	0.0	0.0	0.0	0.0	ns				
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	4.3	5.0	5.6	6.6	9.2	ns				
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0	0.0	0.0	0.0	0.0	ns				

Table 41 • A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PWL}	Minimum Pulse Width LOW	FO = 32	5.3	5.9	6.7	7.8	11.0	ns					
		FO = 384	6.2	6.9	7.9	9.2	12.9	ns					
t _{CKSW}	Maximum Skew	FO = 32	0.5	0.5	0.6	0.7	1.0	ns					
		FO = 384	2.2	2.4	2.7	3.2	4.5	ns					
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0	0.0	0.0	0.0	0.0	ns					
		FO = 384	0.0	0.0	0.0	0.0	0.0	ns					
t _{HEXT}	Input Latch External Hold	FO = 32	3.9	4.3	4.9	5.7	8.0	ns					
		FO = 384	4.5	4.9	5.6	6.6	9.2	ns					
t _P	Minimum Period	FO = 32	7.0	7.8	8.4	9.7	16.2	ns					
		FO = 384	7.7	8.6	9.3	10.7	17.8	ns					
f _{MAX}	Maximum Frequency	FO = 32	142	129	119	103	62	MHz					
		FO = 384	129	117	108	94	56	MHz					
TTL Output Module Timing⁵													
t _{DLH}	Data-to-Pad HIGH		3.5	3.9	4.4	5.2	7.3	ns					
t _{DHL}	Data-to-Pad LOW		4.1	4.6	5.2	6.1	8.6	ns					
t _{ENZH}	Enable Pad Z to HIGH		3.8	4.2	4.8	5.6	7.8	ns					
t _{ENZL}	Enable Pad Z to LOW		4.2	4.6	5.3	6.2	8.7	ns					
t _{ENHZ}	Enable Pad HIGH to Z		7.6	8.4	9.5	11.2	15.7	ns					
t _{ENLZ}	Enable Pad LOW to Z		7.0	7.8	8.8	10.4	14.5	ns					
t _{GLH}	G-to-Pad HIGH		4.8	5.3	6.0	7.2	10.0	ns					
t _{GHL}	G-to-Pad LOW		4.8	5.3	6.0	7.2	10.0	ns					
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.0	8.9	10.1	11.9	16.7	ns					
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		11.3	12.5	14.2	16.7	23.3	ns					
d _{TLH}	Capacitive Loading, LOW to HIGH		0.04	0.04	0.05	0.06	0.08	ns/pF					
d _{THL}	Capacitive Loading, HIGH to LOW		0.05	0.05	0.06	0.07	0.10	ns/pF					
CMOS Output Module Timing⁵													
t _{DLH}	Data-to-Pad HIGH		4.5	5.0	5.6	6.6	9.3	ns					
t _{DHL}	Data-to-Pad LOW		3.4	3.8	4.3	5.1	7.1	ns					
t _{ENZH}	Enable Pad Z to HIGH		3.8	4.2	4.8	5.6	7.8	ns					
t _{ENZL}	Enable Pad Z to LOW		4.2	4.6	5.3	6.2	8.7	ns					
t _{ENHZ}	Enable Pad HIGH to Z		7.6	8.4	9.5	11.2	15.7	ns					
t _{ENLZ}	Enable Pad LOW to Z		7.0	7.8	8.8	10.4	14.5	ns					
t _{GLH}	G-to-Pad HIGH		7.1	7.9	8.9	10.5	14.7	ns					
t _{GHL}	G-to-Pad LOW		7.1	7.9	8.9	10.5	14.7	ns					
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.0	8.9	10.1	11.9	16.7	ns					

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Asynchronous SRAM Operations												
t _{RPD}	Asynchronous Access Time		8.1		9.0		10.2		12.0		16.8	ns
t _{RDADV}	Read Address Valid		8.8		9.8		11.1		13.0		18.2	ns
t _{ADSU}	Address/Data Set-Up Time		1.6		1.8		2.0		2.4		3.4	ns
t _{ADH}	Address/Data Hold Time		0.0		0.0		0.0		0.0		0.0	ns
t _{RENSUA}	Read Enable Set-Up to Address Valid		0.6		0.7		0.8		0.9		1.3	ns
t _{RENHA}	Read Enable Hold		3.4		3.8		4.3		5.0		7.0	ns
t _{WENSU}	Write Enable Set-Up		2.7		3.0		3.4		4.0		5.6	ns
t _{WENH}	Write Enable Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{DOH}	Data Out Hold Time		1.2		1.3		1.5		1.8		2.5	ns
Input Module Propagation Delays												
t _{INPY}	Input Data Pad-to-Y		1.0		1.1		1.3		1.5		2.1	ns
t _{INGO}	Input Latch Gate-to-Output		1.4		1.6		1.8		2.1		2.9	ns
t _{INH}	Input Latch Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{INSU}	Input Latch Set-Up		0.5		0.5		0.6		0.7		1.0	ns
t _{ILA}	Latch Active Pulse Width		4.7		5.2		5.9		6.9		9.7	ns
Input Module Predicted Routing Delays²												
t _{IRD1}	FO = 1 Routing Delay		2.0		2.2		2.5		2.9		4.1	ns
t _{IRD2}	FO = 2 Routing Delay		2.3		2.6		2.9		3.4		4.8	ns
t _{IRD3}	FO = 3 Routing Delay		2.6		2.9		3.3		3.9		5.5	ns
t _{IRD4}	FO = 4 Routing Delay		3.0		3.3		3.8		4.4		6.2	ns
t _{IRD8}	FO = 8 Routing Delay		4.3		4.8		5.5		6.4		9.0	ns
Global Clock Network												
t _{CKH}	Input LOW to HIGH	FO = 32	2.7		3.0		3.4		4.0		5.6	ns
		FO = 635	3.0		3.3		3.8		4.4		6.2	ns
t _{CKL}	Input HIGH to LOW	FO = 32	3.8		4.2		4.8		5.6		7.8	ns
		FO = 635	4.9		5.4		6.1		7.2		10.1	ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	1.8		2.0		2.2		2.6		3.6	ns
		FO = 635	2.0		2.2		2.5		2.9		4.1	ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	1.8		2.0		2.2		2.6		3.6	ns
		FO = 635	2.0		2.2		2.5		2.9		4.1	ns
t _{CKSW}	Maximum Skew	FO = 32	0.8		0.8		0.9		1.0		1.4	ns
		FO = 635	0.8		0.8		0.9		1.0		1.4	ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing⁵ (Continued)											
t _{ENLZ}	Enable Pad LOW to Z		4.9	5.5	6.2	7.3	10.2	ns			
t _{GLH}	G-to-Pad HIGH		2.9	3.3	3.7	4.4	6.1	ns			
t _{GHL}	G-to-Pad LOW		2.9	3.3	3.7	4.4	6.1	ns			
t _{LSU}	I/O Latch Output Set-Up		0.5	0.5	0.6	0.7	1.0	ns			
t _{LH}	I/O Latch Output Hold		0.0	0.0	0.0	0.0	0.0	ns			
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7	6.3	7.1	8.4	11.8	ns			
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8	8.6	9.8	11.5	16.1	ns			
d _{TLH}	Capacitive Loading, LOW to HIGH		0.07	0.08	0.09	0.10	0.14	ns/pF			
d _{THL}	Capacitive Loading, HIGH to LOW		0.07	0.08	0.09	0.10	0.14	ns/pF			

Input, output, tristate or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/Os pins are configured by the Designer software as shown in Table 46, page 84.

Table 46 • Configuration of Unused I/Os

Device	Configuration
A40MX02, A40MX04	Pulled LOW
A42MX09, A42MX16	Pulled LOW
A42MX24, A42MX36	Tristated

In all cases, it is recommended to tie all unused MX I/O pins to LOW on the board. This applies to all dual-purpose pins when configured as I/Os as well.

LP, Low Power Mode

Controls the low power mode of all 42MX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation in 200 μ s after the LP pin is driven to a logic LOW.

MODE, Mode

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). The MODE pin is held HIGH to provide verification capability. The MODE pin should be terminated to GND through a 10k Ω resistor so that the MODE pin can be pulled HIGH when required.

NC, No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O

PRB, I/OProbe A/B

The Probe pin is used to output data from any user-defined design node within the device. Each diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. The Probe pin is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

QCLKA/B/C/D, I/O Quadrant Clock

Quadrant clock inputs for A42MX36 devices. When not used as a register control signal, these pins can function as user I/Os.

SDI, I/OSerial Data Input

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDO, I/OSerial Data Output

Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. SDO is available for 42MX devices only.

When Silicon Explorer II is being used, SDO will act as an output while the "checksum" command is run. It will return to user I/O when "checksum" is complete.

TCK, I/O Test Clock

Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
80	GNDI
81	NC
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	I/O
88	VKS
89	VPP
90	VCC
91	VCCI
92	NC
93	VSV
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	GND
101	GNDI
102	NC
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	I/O
109	I/O
110	SDI
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	GNDQ

Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
21	CLKA, I/O	CLKA, I/O	CLKA, I/O
22	I/O	I/O	I/O
23	PRA, I/O	PRA, I/O	PRA, I/O
24	NC	I/O	WD, I/O
25	I/O	I/O	WD, I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	NC	I/O	I/O
29	I/O	I/O	WD, I/O
30	GND	GND	GND
31	NC	I/O	WD, I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	VCCI	VCCI
36	I/O	I/O	WD, I/O
37	I/O	I/O	WD, I/O
38	SDI, I/O	SDI, I/O	SDI, I/O
39	I/O	I/O	I/O
40	GND	GND	GND
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	GND	GND	GND
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	NC	I/O	I/O
53	I/O	I/O	I/O
54	NC	VCCA	VCCA
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	VCCA	VCCA	VCCA

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
21	I/O	I/O	I/O
22	GND	GND	GND
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	GND	GND	GND
28	VCCI	VCCI	VCCI
29	VCCA	VCCA	VCCA
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	VCCA	VCCA	VCCA
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	NC	I/O	I/O
42	NC	I/O	I/O
43	NC	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	NC	I/O	I/O
52	GND	GND	GND
53	GND	GND	GND
54	I/O	TMS, I/O	TMS, I/O
55	I/O	TDI, I/O	TDI, I/O
56	I/O	I/O	I/O
57	I/O	WD, I/O	WD, I/O

Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	NC	VCCA	VCCA
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	GND	GND	GND
19	NC	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	NC	I/O	I/O
23	GND	GND	GND
24	NC	VCCI	VCCI
25	VCCA	VCCA	VCCA
26	NC	I/O	I/O
27	NC	I/O	I/O
28	VCCI	VCCA	VCCA
29	NC	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	NC	NC	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	NC	I/O	I/O
38	NC	NC	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	GND	GND	GND
46	I/O	I/O	TMS, I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
22	I/O
23	I/O
24	I/O
25	I/O
26	VCCA
27	I/O
28	I/O
29	VCCA
30	VCCI
31	GND
32	VCCA
33	LP
34	TCK, I/O
35	I/O
36	GND
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	GND
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
M10	GND
M11	GND
M12	GND
M17	I/O
M18	I/O
M19	I/O
M20	I/O
N1	I/O
N2	I/O
N3	I/O
N4	VCCI
N17	VCCI
N18	I/O
N19	I/O
N20	I/O
P1	I/O
P2	I/O
P3	I/O
P4	VCCA
P17	I/O
P18	I/O
P19	I/O
P20	I/O
R1	I/O
R2	I/O
R3	I/O
R4	VCCI
R17	VCCI
R18	I/O
R19	I/O
R20	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T17	VCCA
T18	I/O