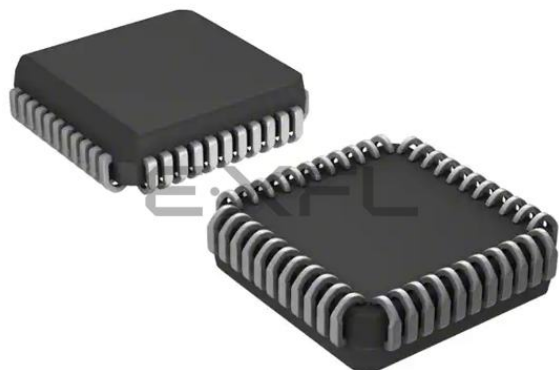




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	34
Number of Gates	6000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-pl44i

2.4 Plastic Device Resources

Table 2 • Plastic Device Resources

Device	User I/Os											
	PLCC 44-Pin	PLCC 68-Pin	PLCC 84-Pin	PQFP 100-Pin	PQFP 144- Pin	PQFP 160-Pin	PQFP 208- Pin	PQFP 240-Pin	VQFP 80-Pin	VQFP 100- Pin	TQFP 176- Pin	PBGA 272- Pin
A40MX02	34	57	–	57	–	–	–	–	57	–	–	–
A40MX04	34	57	69	69	–	–	–	–	69	–	–	–
A42MX09	–	–	72	83	95	101	–	–	–	83	104	–
A42MX16	–	–	72	83	–	125	140	–	–	83	140	–
A42MX24	–	–	72	–	–	125	176	–	–	–	150	–
A42MX36	–	–	–	–	–	–	176	202	–	–	–	202

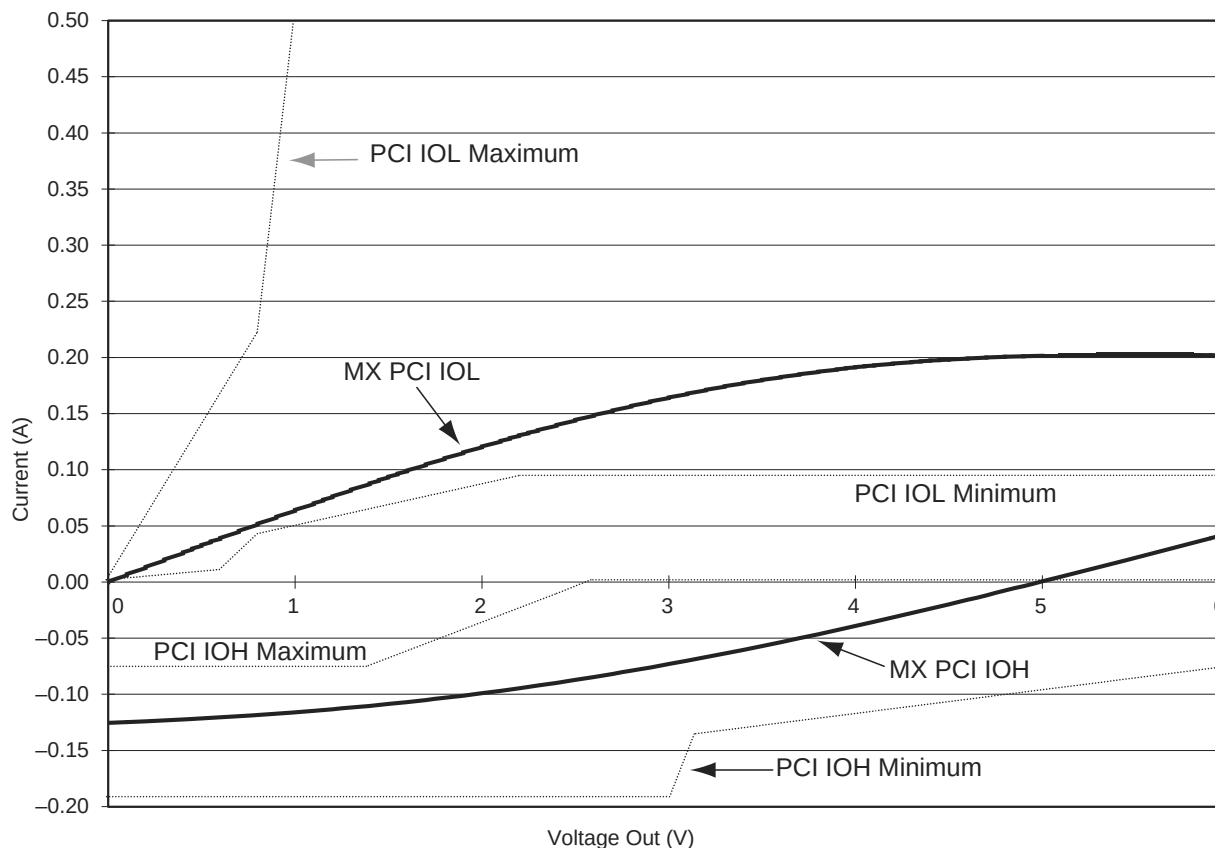
Note: Package Definitions: PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array

2.5 Ceramic Device Resources

Table 3 • Ceramic Device Resources

Device	User I/Os			
	CPGA 132-Pin	CQFP 172-Pin	CQFP 208-Pin	CQFP 256-Pin
A42MX09	95			
A42MX16		131		
A42MX36			176	202

Note: Package Definitions: CQFP = Ceramic Quad Flat Pack

Figure 16 • Typical Output Drive Characteristics (Based Upon Measured Data)

3.9.4 Junction Temperature (T_J)

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a(1)$$

EQ 4

where:

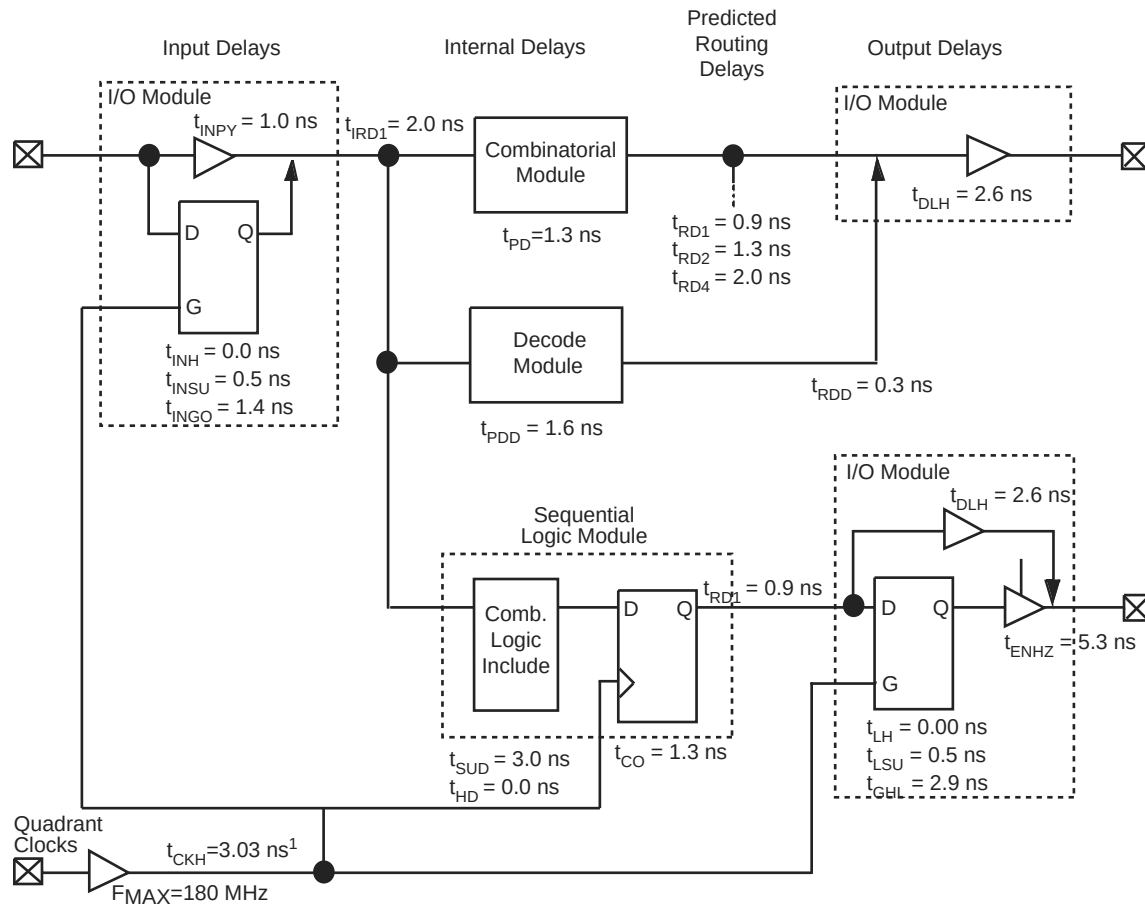
- T_a = Ambient Temperature
- ΔT = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$ (2)
- P = Power
- θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in Table 27, page 29.

3.9.5 Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc} , and the junction-to-ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates.

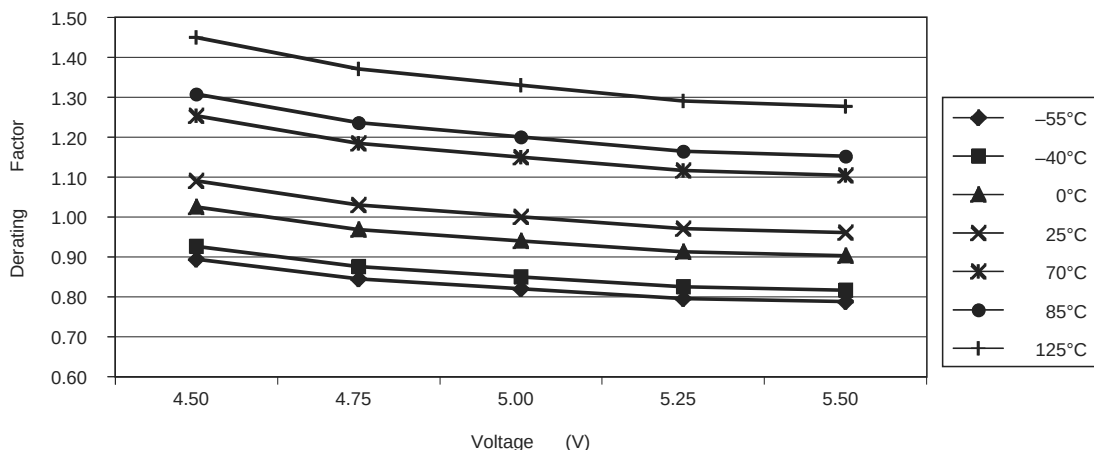
The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of θ_{ja} .

Figure 19 • 42MX Timing Model (Logic Functions Using Quadrant Clocks)

Note: 1. Load-dependent

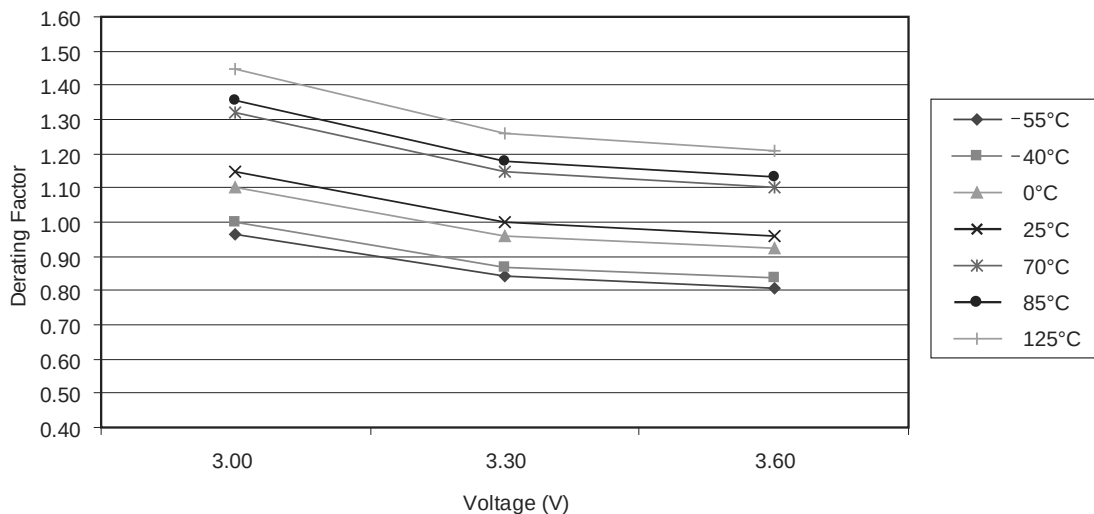
Note: 2. Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions

Figure 35 • 40MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Note: This derating factor applies to all routing and propagation delays

Table 30 • 42MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$)

42MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
3.00	0.97	1.00	1.10	1.15	1.32	1.36	1.45
3.30	0.84	0.87	0.96	1.00	1.15	1.18	1.26
3.60	0.81	0.84	0.92	0.96	1.10	1.13	1.21

Figure 36 • 42MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$)

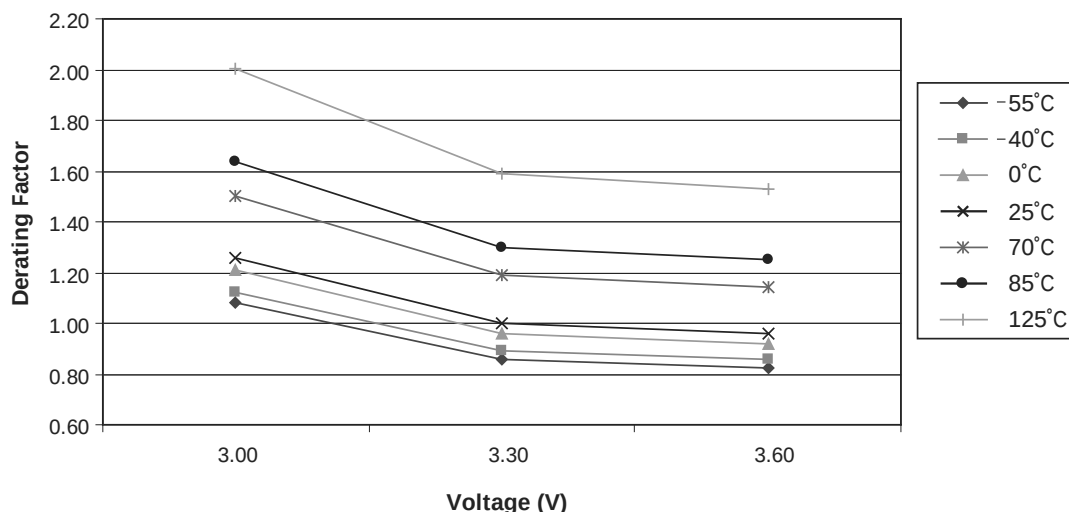
Note: This derating factor applies to all routing and propagation delays

Table 31 • 40MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$)

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
3.00	1.08	1.12	1.21	1.26	1.50	1.64	2.00
3.30	0.86	0.89	0.96	1.00	1.19	1.30	1.59

Table 31 • 40MX Temperature and Voltage Derating Factors (Normalized to T_J = 25°C, V_{CC} = 3.3 V)

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
3.60	0.83	0.85	0.92	0.96	1.14	1.25	1.53

Figure 37 • 40MX Junction Temperature and Voltage Derating Curves (Normalized to T_J = 25°C, V_{CC} = 3.3 V)

Note: This derating factor applies to all routing and propagation delays

3.11.5 PCI System Timing Specification

The following tables list the critical PCI timing parameters and the corresponding timing parameters for the MX PCI-compliant devices.

3.11.6 PCI Models

Microsemi provides synthesizable VHDL and Verilog-HDL models for a PCI Target interface, a PCI Target and Target+DMA Master interface. Contact the Microsemi sales representative for more details.

Table 32 • Clock Specification for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC}	CLK Cycle Time	30	–	4.0	–	4.0	–	ns
t _{HIGH}	CLK High Time	11	–	1.9	–	1.9	–	ns
t _{LOW}	CLK Low Time	11	–	1.9	–	1.9	–	ns

Table 33 • Timing Parameters for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{VAL}	CLK to Signal Valid—Bused Signals	2	11	2.0	9.0	2.0	9.0	ns
t _{VAL(PTP)}	CLK to Signal Valid—Point-to-Point	2 ²	12	2.0	9.0	2.0	9.0	ns
t _{ON}	Float to Active	2	–	2.0	4.0	2.0	4.0	ns
t _{OFF}	Active to Float	–	28	–	8.3 ¹	–	8.3 ¹	ns
t _{SU}	Input Set-Up Time to CLK—Bused Signals	7	–	1.5	–	1.5	–	ns

Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH		3.3		3.8		4.3		5.1		7.2	ns
t _{DHL}	Data-to-Pad LOW		4.0		4.6		5.2		6.1		8.6	ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.3		4.9		5.8		8.0	ns
t _{ENZL}	Enable Pad Z to LOW		4.7		5.4		6.1		7.2		10.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.1	ns
t _{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{THL}	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t _{DHL}	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t _{ENZH}	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t _{ENZL}	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t _{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t _{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d _{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35pF loading

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t _{PD2}	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t _{CO}	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t _{GO}	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays ¹												

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH	5.5		6.4		7.2		8.5		11.9		ns
t _{DHL}	Data-to-Pad LOW	4.8		5.5		6.2		7.3		10.2		ns
t _{ENZH}	Enable Pad Z to HIGH	4.7		5.5		6.2		7.3		10.2		ns
t _{ENZL}	Enable Pad Z to LOW	6.8		7.9		8.9		10.5		14.7		ns
t _{ENHZ}	Enable Pad HIGH to Z	11.1		12.8		14.5		17.1		23.9		ns
t _{ENLZ}	Enable Pad LOW to Z	8.2		9.5		10.7		12.6		17.7		ns
d _{TLH}	Delta LOW to HIGH	0.05		0.05		0.06		0.07		0.10		ns/pF
d _{THL}	Delta HIGH to LOW	0.03		0.03		0.04		0.04		0.06		ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro
4. Delays based on 35 pF loading

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t _{PD2}	Dual-Module Macros		2.3		3.1		3.5		4.1		5.7	ns
t _{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays ¹												
t _{RD1}	FO = 1 Routing Delay		1.2		1.6		1.8		2.1		3.0	ns
t _{RD2}	FO = 2 Routing Delay		1.9		2.2		2.5		2.9		4.1	ns
t _{RD3}	FO = 3 Routing Delay		2.4		2.8		3.2		3.7		5.2	ns
t _{RD4}	FO = 4 Routing Delay		2.9		3.4		3.9		4.5		6.3	ns
t _{RD8}	FO = 8 Routing Delay		5.0		5.8		6.6		7.8		10.9	ns
Logic Module Sequential Timing ²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		3.1		3.5		4.0		4.7		6.6	ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		3.1		3.5		4.0		4.7		6.6	ns

Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		2.4		2.7		3.1		3.6		5.1	ns
t _{DHL}	Data-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t _{ENZH}	Enable Pad Z to HIGH		2.7		2.9		3.3		3.9		5.5	ns
t _{ENZL}	Enable Pad Z to LOW		2.9		3.2		3.7		4.3		6.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		4.9		5.4		6.2		7.3		10.2	ns
t _{ENLZ}	Enable Pad LOW to Z		5.3		5.9		6.7		7.9		11.1	ns
t _{GLH}	G-to-Pad HIGH		4.2		4.6		5.2		6.1		8.6	ns
t _{GHL}	G-to-Pad LOW		4.2		4.6		5.2		6.1		8.6	ns
t _{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.2		5.8		6.6		7.7		10.8	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.4		8.2		9.3		10.9		15.3	ns
d _{TLH}	Capacity Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF
d _{THL}	Capacity Loading, HIGH to LOW		0.04		0.04		0.04		0.05		0.07	ns/pF

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays ¹												
t _{PD1}	Single Module		1.6		1.8		2.1		2.5		3.5	ns
t _{CO}	Sequential Clock-to-Q		1.8		2.0		2.3		2.7		3.8	ns
t _{GO}	Latch G-to-Q		1.7		1.9		2.1		2.5		3.5	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		2.0		2.2		2.5		2.9		4.1	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		1.0		1.1		1.2		1.4		2.0	ns
t _{RD2}	FO = 2 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t _{RD3}	FO = 3 Routing Delay		1.6		1.8		2.0		2.4		3.3	ns

Table 41 • A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		11.3		12.5		14.2		16.7		23.3	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

1. For dual-module macros use tPD1 + tRD1 + taped, to + tRD1 + taped, or tPD1 + tRD1 + tusk, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions ¹												
t _{PD}	Internal Array Module Delay		1.2		1.3		1.5		1.8		2.5	ns
t _{PDD}	Internal Decode Module Delay		1.4		1.6		1.8		2.1		3.0	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		0.8		0.9		1.0		1.2		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.0		1.2		1.3		1.5		2.1	ns
t _{RD3}	FO = 3 Routing Delay		1.3		1.4		1.6		1.9		2.6	ns
t _{RD4}	FO = 4 Routing Delay		1.5		1.7		1.9		2.2		3.1	ns
t _{RD5}	FO = 8 Routing Delay		2.4		2.7		3.0		3.6		5.0	ns
Logic Module Sequential Timing ^{3, 4}												
t _{CO}	Flip-Flop Clock-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t _{GO}	Latch Gate-to-Output		1.2		1.3		1.5		1.8		2.5	ns
t _{SUD}	Flip-Flop (Latch) Set-Up Time	0.3		0.4		0.4		0.5		0.7		ns
t _{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RO}	Flip-Flop (Latch) Reset-to-Output		1.4		1.6		1.8		2.1		2.9	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.4		0.5		0.5		0.6		0.8		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.3		6.5		9.0		ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions ¹												
t _{PD}	Internal Array Module Delay		1.3		1.5		1.7		2.0		2.7	ns
t _{PDD}	Internal Decode Module Delay		1.6		1.8		2.0		2.4		3.3	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.2		1.4		2.0	ns
t _{RD2}	FO = 2 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t _{RD3}	FO =3 Routing Delay		1.6		1.8		2.0		2.4		3.4	ns
t _{RD4}	FO = 4 Routing Delay		2.0		2.2		2.5		2.9		4.1	ns
t _{RD5}	FO = 8 Routing Delay		3.3		3.7		4.2		4.9		6.9	ns
t _{RDD}	Decode-to-Output Routing Delay		0.3		0.4		0.4		0.5		0.7	ns
Logic Module Sequential Timing ^{3, 4}												
t _{CO}	Flip-Flop Clock-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t _{GO}	Latch Gate-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t _{SUD}	Flip-Flop (Latch) Set-Up Time	0.3		0.3		0.4		0.5		0.7		ns
t _{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RO}	Flip-Flop (Latch) Reset-to-Output		1.6		1.7		2.0		2.3		3.2	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.5		6.4		9.0		ns
Synchronous SRAM Operations												
t _{RC}	Read Cycle Time		6.8		7.5		8.5		10.0		14.0	ns
t _{WC}	Write Cycle Time		6.8		7.5		8.5		10.0		14.0	ns
t _{RCKHL}	Clock HIGH/LOW Time		3.4		3.8		4.3		5.0		7.0	ns
t _{RCO}	Data Valid After Clock HIGH/LOW		3.4		3.8		4.3		5.0		7.0	ns
t _{ADSU}	Address/Data Set-Up Time		1.6		1.8		2.0		2.4		3.4	ns
Synchronous SRAM Operations (continued)												
t _{ADH}	Address/Data Hold Time		0.0		0.0		0.0		0.0		0.0	ns
t _{RENSU}	Read Enable Set-Up		0.6		0.7		0.8		0.9		1.3	ns
t _{RENH}	Read Enable Hold		3.4		3.8		4.3		5.0		7.0	ns
t _{WENSU}	Write Enable Set-Up		2.7		3.0		3.4		4.0		5.6	ns
t _{WENH}	Write Enable Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{BENS}	Block Enable Set-Up		2.8		3.1		3.5		4.1		5.7	ns
t _{BENH}	Block Enable Hold		0.0		0.0		0.0		0.0		0.0	ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵ (Continued)												
t _{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t _{GLH}	G-to-Pad HIGH		2.9		3.3		3.7		4.4		6.1	ns
t _{GHL}	G-to-Pad LOW		2.9		3.3		3.7		4.4		6.1	ns
t _{LSU}	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
10	I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O
11	I/O	I/O	I/O	I/O
12	NC	MODE	MODE	MODE
13	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	I/O	I/O	I/O	I/O
18	GND	I/O	I/O	I/O
19	GND	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	VCCA	VCCI	VCCI
23	I/O	VCCI	VCCA	VCCA
24	I/O	I/O	I/O	I/O
25	VCC	I/O	I/O	I/O
26	VCC	I/O	I/O	I/O
27	I/O	I/O	I/O	I/O
28	I/O	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	I/O	I/O	I/O	I/O
31	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	VCC	I/O	I/O	I/O
34	I/O	I/O	I/O	TMS, I/O
35	I/O	I/O	I/O	TDI, I/O
36	I/O	I/O	I/O	WD, I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	WD, I/O
39	I/O	I/O	I/O	WD, I/O
40	GND	I/O	I/O	I/O
41	I/O	I/O	I/O	I/O
42	I/O	I/O	I/O	I/O
43	I/O	VCCA	VCCA	VCCA
44	I/O	I/O	I/O	WD, I/O
45	I/O	I/O	I/O	WD, I/O
46	VCC	I/O	I/O	WD, I/O

Figure 42 • PQ144

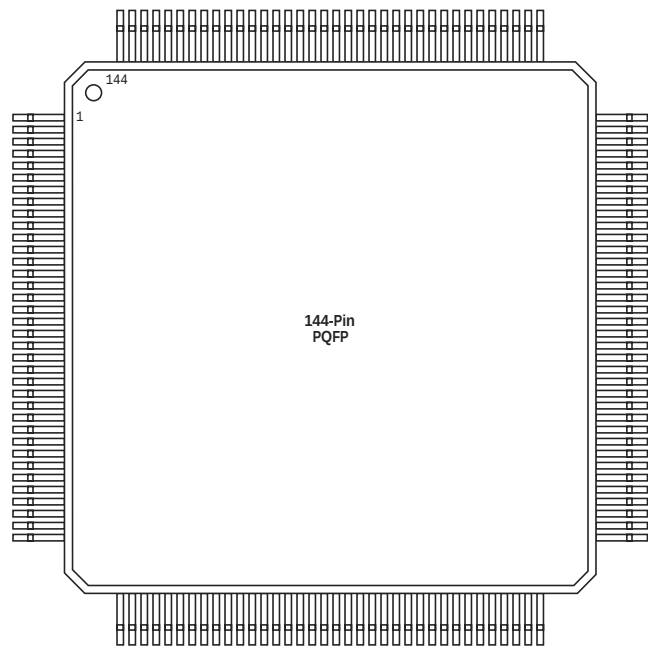


Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
1	I/O
2	MODE
3	I/O
4	I/O
5	I/O

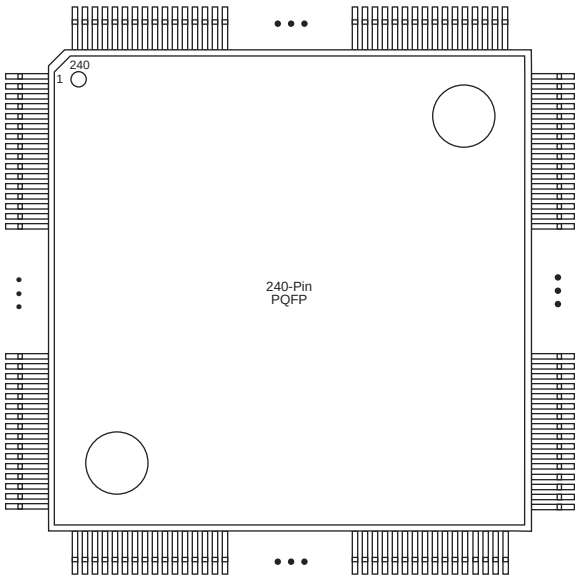
Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
58	I/O	WD, I/O	WD, I/O
59	I/O	I/O	I/O
60	VCCI	VCCI	VCCI
61	NC	I/O	I/O
62	NC	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	QCLKA, I/O
66	I/O	WD, I/O	WD, I/O
67	NC	WD, I/O	WD, I/O
68	NC	I/O	I/O
69	I/O	I/O	I/O
70	I/O	WD, I/O	WD, I/O
71	I/O	WD, I/O	WD, I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	GND	GND	GND
79	VCCA	VCCA	VCCA
80	NC	VCCI	VCCI
81	I/O	I/O	I/O
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	WD, I/O	WD, I/O
86	I/O	WD, I/O	WD, I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	NC	I/O	I/O
90	NC	I/O	I/O
91	I/O	I/O	QCLKB, I/O
92	I/O	I/O	I/O
93	I/O	WD, I/O	WD, I/O
94	I/O	WD, I/O	WD, I/O

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
206	I/O	I/O	I/O
207	DCLK, I/O	DCLK, I/O	DCLK, I/O
208	I/O	I/O	I/O

Figure 45 • PQ240



Note: This figure shows the 240-Pin PQFP Package top view.

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
1	I/O
2	DCLK, I/O
3	I/O
4	I/O
5	I/O
6	WD, I/O
7	WD, I/O
8	VCCI
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O

Table 56 • VQ100

VQ100		
Pin Number	A42MX09 Function	A42MX16 Function
93	I/O	I/O
94	GND	GND
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	DCLK, I/O	DCLK, I/O

Figure 48 • TQ176

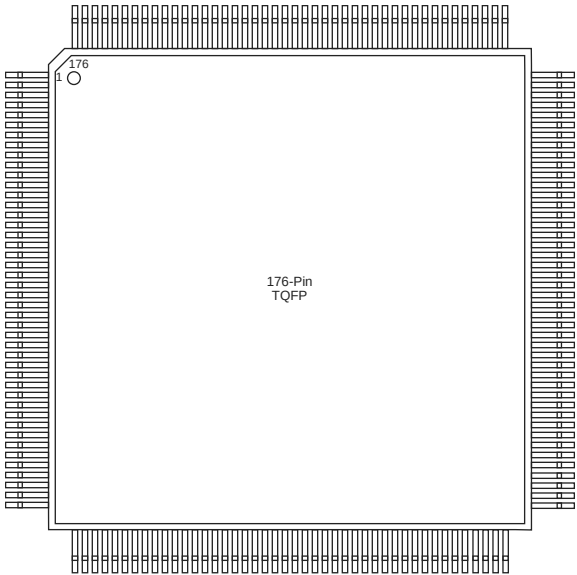


Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	GND	GND	GND
2	MODE	MODE	MODE
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	NC	NC	I/O
9	I/O	I/O	I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	I/O
125	I/O
126	GND
127	I/O
128	TCK, I/O
129	LP
130	VCCA
131	GND
132	VCCI
133	VCCA
134	I/O
135	I/O
136	VCCA
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
22	I/O
23	I/O
24	I/O
25	I/O
26	VCCA
27	I/O
28	I/O
29	VCCA
30	VCCI
31	GND
32	VCCA
33	LP
34	TCK, I/O
35	I/O
36	GND
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	GND
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
133	I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	GND
140	I/O
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	I/O
153	I/O
154	I/O
155	VCCA
156	I/O
157	I/O
158	VCCA
159	VCCI
160	GND
161	I/O
162	I/O
163	I/O
164	I/O
165	GND
166	I/O
167	I/O
168	I/O
169	I/O

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
T19	I/O
T20	I/O
U1	I/O
U2	I/O
U3	I/O
U4	I/O
U5	VCCI
U6	WD, I/O
U7	I/O
U8	I/O
U9	WD, I/O
U10	VCCA
U11	VCCI
U12	I/O
U13	I/O
U14	QCLKB, I/O
U15	I/O
U16	VCCI
U17	I/O
U18	GND
U19	I/O
U20	I/O
V1	I/O
V2	I/O
V3	GND
V4	GND
V5	I/O
V6	I/O
V7	I/O
V8	WD, I/O
V9	I/O
V10	I/O
V11	I/O
V12	I/O
V13	WD, I/O
V14	I/O
V15	WD, I/O