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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	6000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-pl84i">https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-pl84i</a>



**Microsemi Corporate Headquarters**  
One Enterprise, Aliso Viejo,  
CA 92656 USA  
Within the USA: +1 (800) 713-4113  
Outside the USA: +1 (949) 380-6100  
Fax: +1 (949) 215-4996  
Email: [sales.support@microsemi.com](mailto:sales.support@microsemi.com)  
[www.microsemi.com](http://www.microsemi.com)

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Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at [www.microsemi.com](http://www.microsemi.com).

# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- [Table 15](#), page 21 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- [Table 22](#), page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- [Table 23](#), page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

## 1.2 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Added CQFP package information for A42MX16 device in [Product Profile](#), page 1 and [Ceramic Device Resources](#), page 4 (SAR 79522).
- Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in [Temperature Grade Offerings](#), page 5 (SAR 79519)
- Changed Silicon Sculptor II to Silicon Sculptor in [Programming](#), page 12 (SAR 38754)
- Added [Figure 53](#), page 158 CQ172 package (SAR 79522).

## 1.3 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Added [Figure 42](#), page 97 PQ144 Package for A42MX09 device (SAR 69776)
- Added [Figure 52](#), page 153 PQ132 Package for A42MX09 device (SAR 69776)

## 1.4 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Added information on power-up behavior for A42MX24 and A42MX36 devices to the [Power Supply](#), page 13 (SAR 42096)
- Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793)

## 1.5 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- The FuseLock logo and accompanying text was removed from the [User Security](#), page 12. This marking is no longer used on Microsemi devices ([PCN 0915](#))
- The [Development Tool Support](#), page 19 was updated (SAR 38512)

## 1.6 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- [Ordering Information](#), page 3 was updated to include lead-free package ordering codes (SAR 21968)
- The [User Security](#), page 12 was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673)

## 2.4 Plastic Device Resources

**Table 2 • Plastic Device Resources**

Device	User I/Os											
	PLCC 44-Pin	PLCC 68-Pin	PLCC 84-Pin	PQFP 100-Pin	PQFP 144- Pin	PQFP 160-Pin	PQFP 208- Pin	PQFP 240-Pin	VQFP 80-Pin	VQFP 100- Pin	TQFP 176- Pin	PBGA 272- Pin
A40MX02	34	57	—	57	—	—	—	—	57	—	—	—
A40MX04	34	57	69	69	—	—	—	—	69	—	—	—
A42MX09	—	—	72	83	95	101	—	—	—	83	104	—
A42MX16	—	—	72	83	—	125	140	—	—	83	140	—
A42MX24	—	—	72	—	—	125	176	—	—	—	150	—
A42MX36	—	—	—	—	—	—	176	202	—	—	—	202

**Note: Package Definitions:** PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array

## 2.5 Ceramic Device Resources

**Table 3 • Ceramic Device Resources**

Device	User I/Os			
	CPGA 132-Pin	CQFP 172-Pin	CQFP 208-Pin	CQFP 256-Pin
A42MX09	95			
A42MX16		131		
A42MX36			176	202

**Note: Package Definitions:** CQFP = Ceramic Quad Flat Pack

## 2.6 Temperature Grade Offerings

**Table 4 • Temperature Grade Offerings**

Package	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PLCC 44	C, I, M	C, I, M				
PLCC 68	C, I, A, M	C, I, M				
PLCC 84		C, I, A, M	C, I, A, M	C, I, M	C, I, M	
PQFP 100	C, I, A, M	C, I, A, M	C, I, A, M	C, I, M		
PQFP 144			C			
PQFP 160			C, I, A, M	C, I, M	C, I, A, M	
PQFP 208				C, I, A, M	C, I, A, M	C, I, A, M
PQFP 240						C, I, A, M
VQFP 80	C, I, A, M	C, I, A, M				
VQFP 100			C, I, A, M	C, I, A, M		
TQFP 176			C, I, A, M	C, I, A, M	C, I, A, M	
PBGA 272						C, I, M
CQFP 172				C, M, B		
CQFP 208						C, M, B
CQFP 256						C, M, B
CPGA 132			C, M, B			

**Note:** C = Commercial  
 I = Industrial  
 A = Automotive  
 M = Military  
 B = MIL-STD-883 Class B

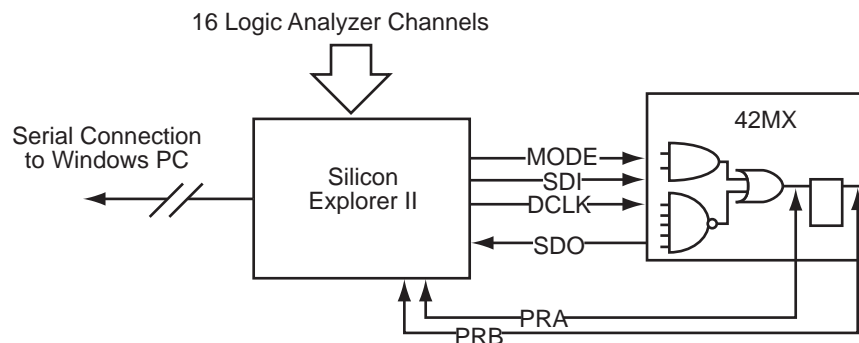
## 2.7 Speed Grade Offerings

**Table 5 • Speed Grade Offerings**

	– F	Std	–1	–2	–3
C	P	P	P	P	P
I		P	P	P	P
A		P			
M		P	P		
B		P	P		

**Note:** See the [40MX and 42MX Automotive Family FPGAs](#) datasheet for details on automotive-grade MX offerings.

Contact your local [Microsemi Sales representative](#) for device availability.

**Figure 13 • Silicon Explorer II Setup with 42MX****Table 8 • Device Configuration Options for Probe Capability**

Security Fuse(s) Programmed	Mode	PRA, PRB <sup>1</sup>	SDI, SDO, DCLK <sup>1</sup>
No	LOW	User I/Os <sup>2</sup>	User I/Os <sup>2</sup>
No	HIGH	Probe Circuit Outputs	Probe Circuit Inputs
Yes	—	Probe Circuit Secured	Probe Circuit Secured

1. Avoid using SDI, SDO, DCLK, PRA and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.
2. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. See the [Pin Descriptions](#), page 83 for information on unused I/O pins

### 3.4.7 Design Consideration

It is recommended to use a series 70Ω termination resistor on every probe connector (SDI, SDO, MODE, DCLK, PRA and PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

### 3.4.8 IEEE Standard 1149.1 Boundary Scan Test (BST) Circuitry

42MX24 and 42MX36 devices are compatible with IEEE Standard 1149.1 (informally known as Joint Testing Action Group Standard or JTAG), which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic MX boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers and instruction register ([Figure 14](#), page 18). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and some optional instructions. [Table 9](#), page 18 describes the ports that control JTAG testing, while [Table 10](#), page 18 describes the test instructions supported by these MX devices.

Each test section is accessed through the TAP, which has four associated pins: TCK (test clock input), TDI and TDO (test data input and output), and TMS (test mode selector).

The TAP controller is a four-bit state machine. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles.

42MX24 and 42MX36 devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi's integrated verification and logic analysis tool. Another tool included in the Libero software is the SmartGen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Microsemi's Libero software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synopsys, and Cadence design systems.

See the Libero IDE web content at [www.microsemi.com/soc/products/software/libero/default.aspx](http://www.microsemi.com/soc/products/software/libero/default.aspx) for further information on licensing and current operating system support.

## 3.6 Related Documents

The following sections give the list of related documents which can be referred for this datasheet.

### 3.6.1 Application Notes

- *AC278: BSDL Files Format Description*
- *AC225: Programming Antifuse Devices*
- *AC168: Implementation of Security in Microsemi Antifuse FPGAs*

### 3.6.2 User Guides and Manuals

- *Antifuse Macro Library Guide*
- *Silicon Sculptor Programmers User Guide*

### 3.6.3 Miscellaneous

*Libero IDE Flow Diagram*

## 3.7 5.0 V Operating Conditions

The following tables show 5.0 V operating conditions.

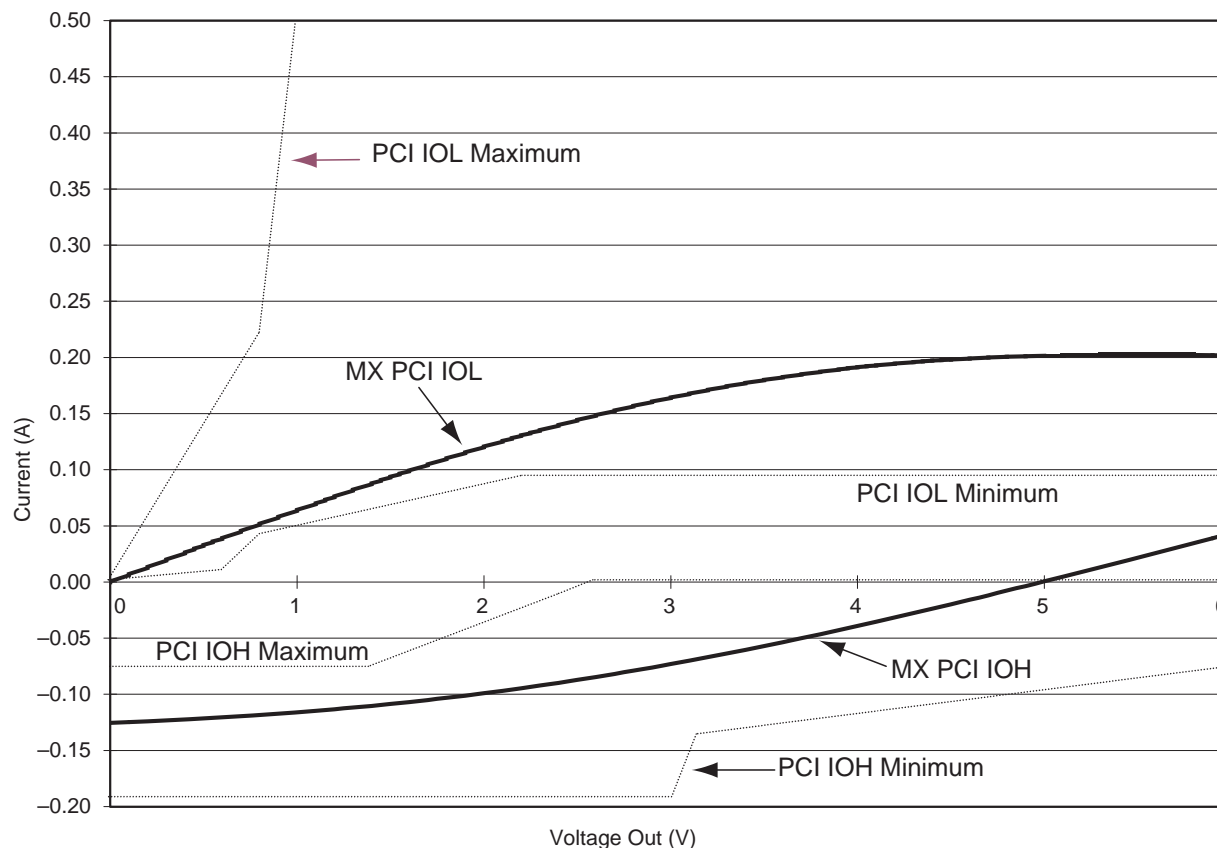
**Table 12 • Absolute Maximum Ratings for 40MX Devices\***

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	−0.5 to +7.0	V
VI	Input Voltage	−0.5 to VCC+0.5	V
VO	Output Voltage	−0.5 to VCC+0.5	V
t <sub>STG</sub>	Storage Temperature	−65 to +150	°C

**Note:** \*Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

**Table 13 • Absolute Maximum Ratings for 42MX Devices\***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	−0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	−0.5 to +7.0	V
VI	Input Voltage	−0.5 to VCCI+0.5	V
VO	Output Voltage	−0.5 to VCCI+0.5	V
t <sub>STG</sub>	Storage Temperature	−65 to +150	°C

**Figure 16 • Typical Output Drive Characteristics (Based Upon Measured Data)**

### 3.9.4 Junction Temperature ( $T_J$ )

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a(1)$$

**EQ 4**

where:

- $T_a$  = Ambient Temperature
- $\Delta T$  = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$  (2)
- $P$  = Power
- $\theta_{ja}$  = Junction to ambient of package.  $\theta_{ja}$  numbers are located in [Table 27](#), page 29.

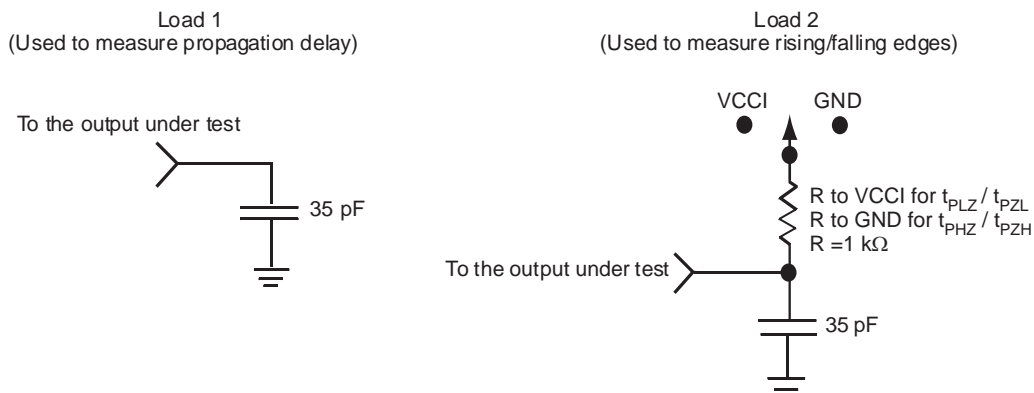
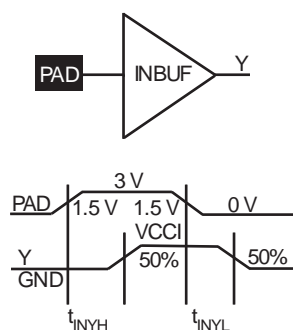
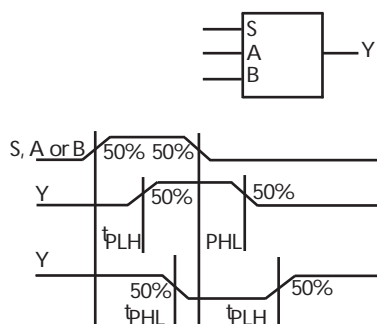
### 3.9.5 Package Thermal Characteristics

The device junction-to-case thermal characteristic is  $\theta_{jc}$ , and the junction-to-ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates.

The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of  $\theta_{ja}$ .



**Figure 22 • AC Test Loads****Figure 23 • Input Buffer Delays****Figure 24 • Module Delays**

**Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>HENA</sub>	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t <sub>WCLKA</sub>	Flip-Flop (Latch) Clock Active Pulse Width		3.3		3.8		4.3		5.0		7.0		ns
t <sub>WASYN</sub>	Flip-Flop (Latch) Asynchronous Pulse Width		3.3		3.8		4.3		5.0		7.0		ns
t <sub>A</sub>	Flip-Flop Clock Input Period		4.8		5.6		6.3		7.5		10.4		ns
f <sub>MAX</sub>	Flip-Flop (Latch) Clock Frequency (FO = 128)			181		167		154		134		80	MHz
Input Module Propagation Delays													
t <sub>INYH</sub>	Pad-to-Y HIGH			0.7		0.8		0.9		1.1		1.5	ns
t <sub>INYL</sub>	Pad-to-Y LOW			0.6		0.7		0.8		1.0		1.3	ns
Input Module Predicted Routing Delays <sup>1</sup>													
t <sub>IRD1</sub>	FO = 1 Routing Delay			2.1		2.4		2.2		3.2		4.5	ns
t <sub>IRD2</sub>	FO = 2 Routing Delay			2.6		3.0		3.4		4.0		5.6	ns
t <sub>IRD3</sub>	FO = 3 Routing Delay			3.1		3.6		4.1		4.8		6.7	ns
t <sub>IRD4</sub>	FO = 4 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t <sub>IRD8</sub>	FO = 8 Routing Delay			5.7		6.6		7.5		8.8		12.4	ns
Global Clock Network													
t <sub>CKH</sub>	Input Low to HIGH	FO = 16		4.6		5.3		6.0		7.0		9.8	ns
		FO = 128		4.6		5.3		6.0		7.0		9.8	
t <sub>CKL</sub>	Input High to LOW	FO = 16		4.8		5.6		6.3		7.4		10.4	ns
		FO = 128		4.8		5.6		6.3		7.4		10.4	
t <sub>PWH</sub>	Minimum Pulse Width HIGH	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.1		3.6		5.1		
t <sub>PWL</sub>	Minimum Pulse Width LOW	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.01		3.6		5.1		
t <sub>CKSW</sub>	Maximum Skew	FO = 16		0.4		0.5		0.5		0.6		0.8	ns
		FO = 128		0.5		0.6		0.7		0.8		1.2	
t <sub>P</sub>	Minimum Period	FO = 16	4.7		5.4		6.1		7.2		10.0		ns
		FO = 128	4.8		5.6		6.3		7.5		10.4		
f <sub>MAX</sub>	Maximum Frequency	FO = 16		188		175		160		139		83	MHz
		FO = 128		181		168		154		134		80	
TTL Output Module Timing <sup>4</sup>													
t <sub>DLH</sub>	Data-to-Pad HIGH			3.3		3.8		4.3		5.1		7.2	ns
t <sub>DHL</sub>	Data-to-Pad LOW			4.0		4.6		5.2		6.1		8.6	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH			3.7		4.3		4.9		5.8		8.0	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW			4.7		5.4		6.1		7.2		10.1	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z			7.9		9.1		10.4		12.2		17.1	ns

**Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T<sub>J</sub> = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t <sub>INYH</sub>	Pad-to-Y HIGH			1.0		1.2		1.3		1.6		2.2	ns
t <sub>INYL</sub>	Pad-to-Y LOW			0.8		0.9		1.0		1.2		1.7	ns
t <sub>INGH</sub>	G to Y HIGH			1.3		1.4		1.6		1.9		2.7	ns
t <sub>INGL</sub>	G to Y LOW			1.3		1.4		1.6		1.9		2.7	ns
Input Module Predicted Routing Delays <sup>2</sup>													
t <sub>IRD1</sub>	FO = 1 Routing Delay			2.0		2.2		2.5		3.0		4.2	ns
t <sub>IRD2</sub>	FO = 2 Routing Delay			2.3		2.5		2.9		3.4		4.7	ns
t <sub>IRD3</sub>	FO = 3 Routing Delay			2.5		2.8		3.2		3.7		5.2	ns
t <sub>IRD4</sub>	FO = 4 Routing Delay			2.8		3.1		3.5		4.1		5.7	ns
t <sub>IRD8</sub>	FO = 8 Routing Delay			3.7		4.1		4.7		5.5		7.7	ns
Global Clock Network													
t <sub>CKH</sub>	Input LOW to HIGH	FO = 32		2.4		2.7		3.0		3.6		5.0	ns
		FO = 256		2.7		3.0		3.4		4.0		5.5	ns
t <sub>CKL</sub>	Input HIGH to LOW	FO = 32		3.5		3.9		4.4		5.2		7.3	ns
		FO = 256		3.9		4.3		4.9		5.7		8.0	ns
t <sub>PWH</sub>	Minimum Pulse Width HIGH	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t <sub>PWL</sub>	Minimum Pulse Width LOW	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t <sub>CKSW</sub>	Maximum Skew	FO = 32		0.3		0.3		0.4		0.5		0.6	ns
		FO = 256		0.3		0.3		0.4		0.5		0.6	ns
t <sub>SUEXT</sub>	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		0.0		0.0		ns
t <sub>HEXT</sub>	Input Latch External Hold	FO = 32	2.3		2.6		3.0		3.5		4.9		ns
		FO = 256	2.2		2.4		3.3		3.9		5.5		ns
t <sub>P</sub>	Minimum Period	FO = 32	3.4		3.7		4.0		4.7		7.8		ns
		FO = 256	3.7		4.1		4.5		5.2		8.6		ns
f <sub>MAX</sub>	Maximum Frequency	FO = 32		296		269		247		215		129	MHz
		FO = 256		268		244		224		195		117	MHz

**Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T<sub>J</sub> = 70°C)**

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Sequential Timing <sup>3, 4</sup>												
t <sub>CO</sub>	Flip-Flop Clock-to-Output	2.1		2.0		2.3		2.7		3.7		ns
t <sub>GO</sub>	Latch Gate-to-Output	3.4		1.9		2.1		2.5		3.4		ns
t <sub>SUD</sub>	Flip-Flop (Latch) Set-Up Time	0.4		0.5		0.6		0.7		0.9		ns
t <sub>HD</sub>	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t <sub>RO</sub>	Flip-Flop (Latch) Reset-to-Output	2.0		2.2		2.5		2.9		4.1		ns
t <sub>SUENA</sub>	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t <sub>HENA</sub>	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>WCLKA</sub>	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.2		5.8		6.9		9.6		ns
t <sub>WASYN</sub>	Flip-Flop (Latch) Asynchronous Pulse Width	6.1		6.8		7.7		9.0		12.6		ns
Input Module Propagation Delays												
t <sub>INPY</sub>	Input Data Pad-to-Y	1.4		1.6		1.8		2.2		3.0		ns
t <sub>INGO</sub>	Input Latch Gate-to-Output	1.8		1.9		2.2		2.6		3.6		ns
t <sub>INH</sub>	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>INSU</sub>	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t <sub>ILA</sub>	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

**Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)** (Worst-Case Commercial Conditions, VCCA = 3.0 V, T<sub>J</sub> = 70°C)

Parameter / Description	–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>ACO</sub> Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.9		12.1		13.7		16.1		22.5	ns
d <sub>TLH</sub> Capacitive Loading, LOW to HIGH		0.10		0.11		0.12		0.14		0.20	ns/pF
d <sub>THL</sub> Capacitive Loading, HIGH to LOW		0.10		0.11		0.12		0.14		0.20	ns/pF
<b>CMOS Output Module Timing<sup>5</sup></b>											
t <sub>DLH</sub> Data-to-Pad HIGH		4.9		5.5		6.2		7.3		10.3	ns
t <sub>DHL</sub> Data-to-Pad LOW		3.4		3.8		4.3		5.1		7.1	ns
t <sub>ENZH</sub> Enable Pad Z to HIGH		3.7		4.1		4.7		5.5		7.7	ns
t <sub>ENZL</sub> Enable Pad Z to LOW		4.1		4.6		5.2		6.1		8.5	ns
t <sub>ENHZ</sub> Enable Pad HIGH to Z		7.4		8.2		9.3		10.9		15.3	ns
t <sub>ENLZ</sub> Enable Pad LOW to Z		6.9		7.6		8.7		10.2		14.3	ns
t <sub>GLH</sub> G-to-Pad HIGH		7.0		7.8		8.9		10.4		14.6	ns
t <sub>GHL</sub> G-to-Pad LOW		7.0		7.8		8.9		10.4		14.6	ns
t <sub>LSU</sub> I/O Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t <sub>LH</sub> I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>LCO</sub> I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.9		8.8		10.0		11.8		16.5	ns

1. For dual-module macros, use t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

## 3.12 Pin Descriptions

This section lists the pin descriptions for 40MX and 42MX series FPGAs.

### CLK/A/B, I/O Global Clock

Clock inputs for clock distribution networks. CLK is for 40MX while CLKA and CLKB are for 42MX devices. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

### DCLK, I/O Diagnostic Clock

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### GND, Ground

Input LOW supply voltage.

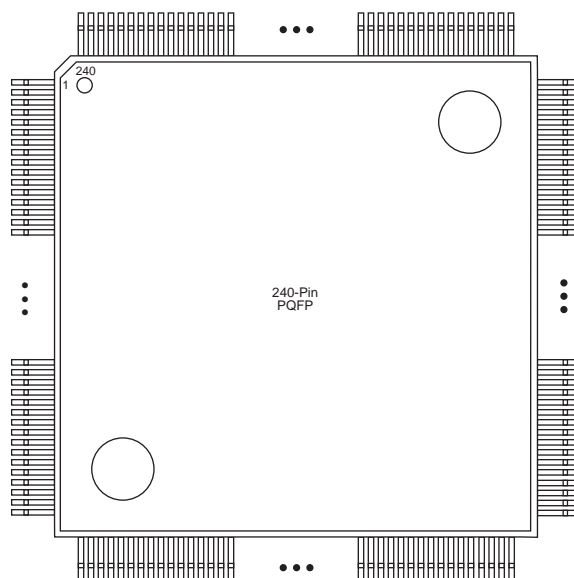
### I/O, Input/Output

**Table 53 • PQ208**

<b>PQ208</b>			
<b>Pin Number</b>	<b>A42MX16 Function</b>	<b>A42MX24 Function</b>	<b>A42MX36 Function</b>
21	I/O	I/O	I/O
22	GND	GND	GND
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	GND	GND	GND
28	VCCI	VCCI	VCCI
29	VCCA	VCCA	VCCA
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	VCCA	VCCA	VCCA
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	NC	I/O	I/O
42	NC	I/O	I/O
43	NC	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	NC	I/O	I/O
52	GND	GND	GND
53	GND	GND	GND
54	I/O	TMS, I/O	TMS, I/O
55	I/O	TDI, I/O	TDI, I/O
56	I/O	I/O	I/O
57	I/O	WD, I/O	WD, I/O

**Table 53 • PQ208**

<b>PQ208</b>			
<b>Pin Number</b>	<b>A42MX16 Function</b>	<b>A42MX24 Function</b>	<b>A42MX36 Function</b>
206	I/O	I/O	I/O
207	DCLK, I/O	DCLK, I/O	DCLK, I/O
208	I/O	I/O	I/O

**Figure 45 • PQ240**

**Note:** This figure shows the 240-Pin PQFP Package top view.

**Table 54 • PQ240**

<b>PQ240</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
1	I/O
2	DCLK, I/O
3	I/O
4	I/O
5	I/O
6	WD, I/O
7	WD, I/O
8	VCCI
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O

**Table 54 • PQ240**

<b>PQ240</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
89	VCCI
90	VCCA
91	LP
92	TCK, I/O
93	I/O
94	GND
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	VCCI
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	VCCA
119	GND
120	GND
121	GND
122	I/O
123	SDO, TDO, I/O
124	I/O
125	WD, I/O



**Table 54 • PQ240**

<b>PQ240</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
200	I/O
201	I/O
202	I/O
203	I/O
204	I/O
205	I/O
206	VCCA
207	I/O
208	I/O
209	VCCA
210	VCCI
211	I/O
212	I/O
213	I/O
214	I/O
215	I/O
216	I/O
217	I/O
218	I/O
219	VCCA
220	I/O
221	I/O
222	I/O
223	I/O
224	I/O
225	I/O
226	I/O
227	VCCI
228	I/O
229	I/O
230	I/O
231	I/O
232	I/O
233	I/O
234	I/O
235	I/O
236	I/O

**Table 55 • VQ80**

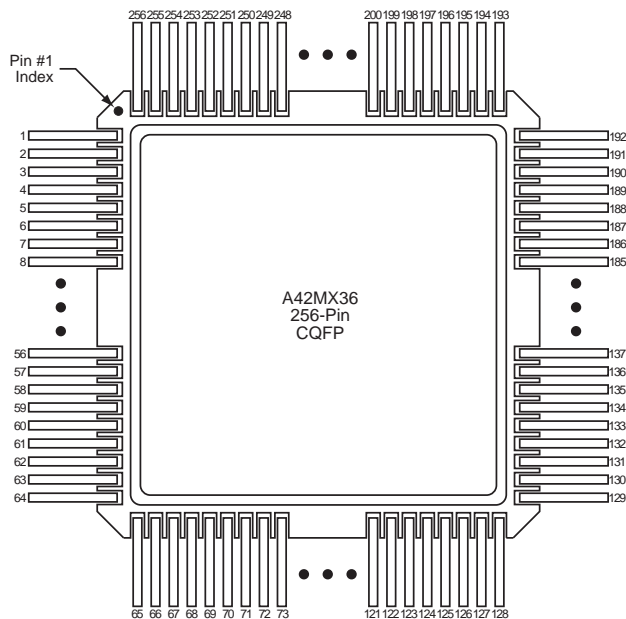
<b>VQ80</b>		
<b>Pin Number</b>	<b>A40MX02 Function</b>	<b>A40MX04 Function</b>
49	I/O	I/O
50	CLK, I/O	CLK, I/O
51	I/O	I/O
52	MODE	MODE
53	VCC	VCC
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	GND	GND
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	VCC	<b>VCC</b>
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O

**Table 57 • TQ176**

<b>TQ176</b>			
<b>Pin Number</b>	<b>A42MX09 Function</b>	<b>A42MX16 Function</b>	<b>A42MX24 Function</b>
84	I/O	I/O	WD, I/O
85	I/O	I/O	WD, I/O
86	NC	I/O	I/O
87	SDO, I/O	SDO, I/O	SDO, TDO, I/O
88	I/O	I/O	I/O
89	GND	GND	GND
90	I/O	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	NC	NC	I/O
102	I/O	I/O	I/O
103	NC	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	GND	GND	GND
107	NC	I/O	I/O
108	NC	I/O	TCK, I/O
109	LP	LP	LP
110	VCCA	VCCA	VCCA
111	GND	GND	GND
112	VCCI	VCCI	VCCI
113	VCCA	VCCA	VCCA
114	NC	I/O	I/O
115	NC	I/O	I/O
116	NC	VCCA	VCCA
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O

**Table 58 • CQ208**

<b>CQ208</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
1	GND
2	VCCA
3	MODE
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	VCCA
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	VCCI
29	VCCA
30	I/O
31	I/O
32	VCCA
33	I/O
34	I/O
35	I/O
36	I/O

**Figure 50 • CQ256****Table 59 • CQ256**

<b>CQ256</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
1	NC
2	GND
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	GND
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O