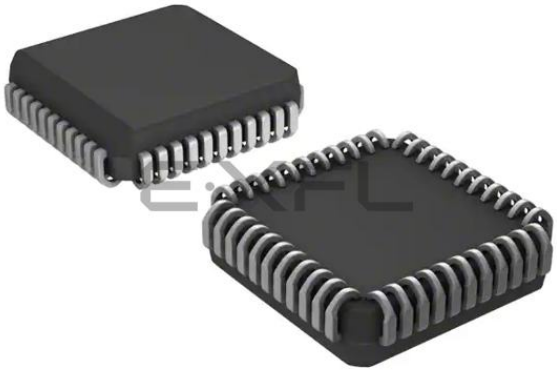

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Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	34
Number of Gates	6000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-plg44i

3.4.9 JTAG Mode Activation

The JTAG test logic circuit is activated in the Designer software by selecting **Tools > Device Selection**. This brings up the Device Selection dialog box as shown in the following figure. The JTAG test logic circuit can be enabled by clicking the “Reserve JTAG Pins” check box. The following table explains the pins' behavior in either mode.

Figure 15 • **Device Selection Wizard**

Table 11 • **Boundary Scan Pin Configuration and Functionality**

Reserve JTAG	Checked	Unchecked
TCK	BST input; must be terminated to logical HIGH or LOW to avoid floating	User I/O
TDI, TMS	BST input; may float or be tied to HIGH	User I/O
TDO	BST output; may float or be connected to TDI of another device	User I/O

3.4.10 TRST Pin and TAP Controller Reset

An active reset (TRST) pin is not supported; however, MX devices contain power-on circuitry that resets the boundary scan circuitry upon power-up. Also, the TMS pin is equipped with an internal pull-up resistor. This allows the TAP controller to remain in or return to the Test-Logic-Reset state when there is no input or when a logical 1 is on the TMS pin. To reset the controller, TMS must be HIGH for at least five TCK cycles.

3.4.11 Boundary Scan Description Language (BSDL) File

Conforming to the IEEE Standard 1149.1 requires that the operation of the various JTAG components be documented. The BSDL file provides the standard format to describe the JTAG components that can be used by automatic test equipment software. The file includes the instructions that are supported, instruction bit pattern, and the boundary-scan chain order. For an in-depth discussion on BSDL files, see the *BSDL Files Format Description* application note.

BSDL files are grouped into two categories - generic and device-specific. The generic files assign all user I/Os as inouts. Device-specific files assign user I/Os as inputs, outputs or inouts.

Generic files for MX devices are available on the Microsemi SoC Product Group's website:

http://www.microsemi.com/soc/techdocs/models/bsdl.html.

3.5 Development Tool Support

The MX family of FPGAs is fully supported by Libero® Integrated Design Environment (IDE). Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes SynplifyPro from Synopsys, ModelSim® HDL Simulator from Mentor Graphics® and Viewdraw.

Libero IDE includes place-and-route and provides a comprehensive suite of backend support tools for FPGA development, including timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor.

3. All outputs unloaded. All inputs = VCC/VCCI or GND

3.8 3.3 V Operating Conditions

The following table shows 3.3 V operating conditions.

Table 16 • **Absolute Maximum Ratings for 40MX Devices***

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCC + 0.5	V
VO	Output Voltage	–0.5 to VCC + 0.5	V
t_{STG}	Storage Temperature	–65 to + 150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 17 • **Absolute Maximum Ratings for 42MX Devices***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCCI+0.5	V
VO	Output Voltage	–0.5 to VCCI+0.5	V
t_{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 18 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCA (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCI (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

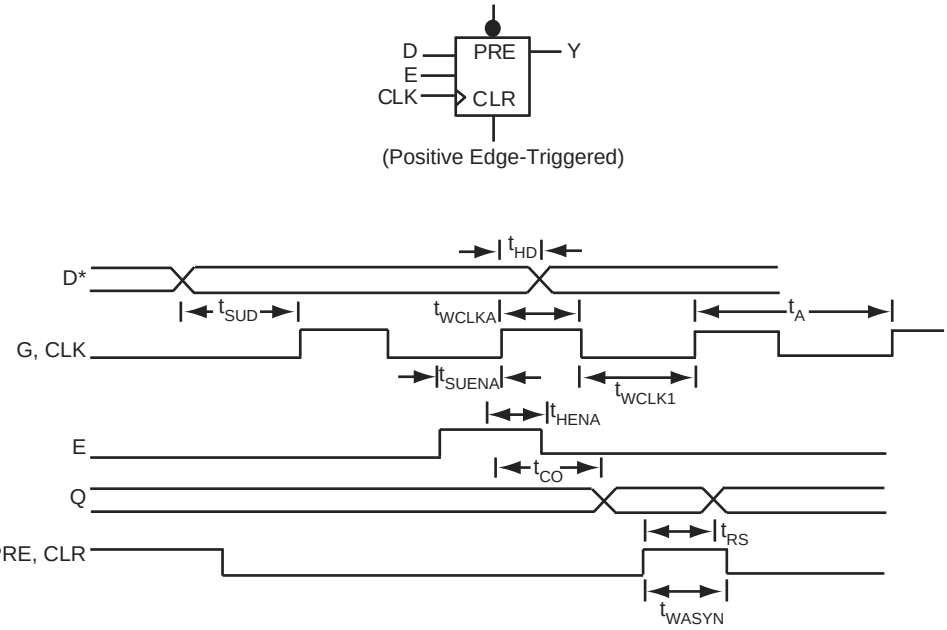
Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

All the following tables show various specifications and operating conditions of 40MX and 42MX FPGAs.

3.10.2 Sequential Module Timing Characteristics

The following figure shows sequential module timing characteristics.

Figure 25 • **Flip-Flops and Latches**

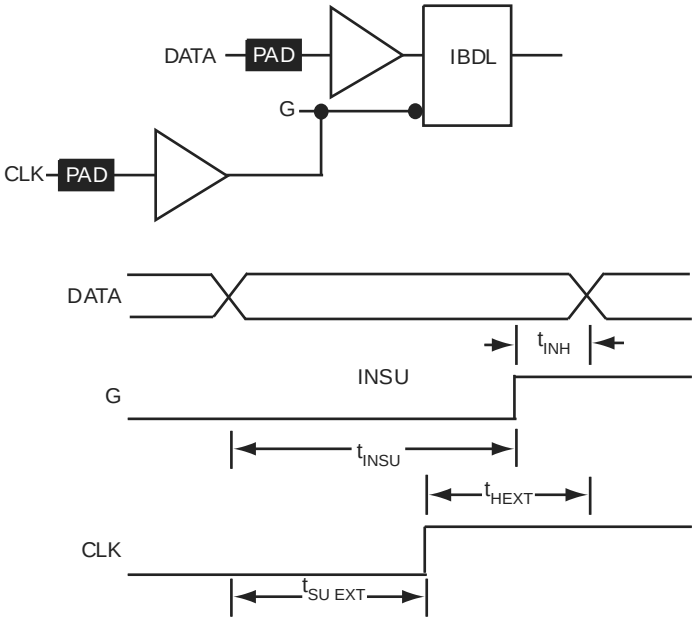


Note: *D represents all data functions involving A, B, and S for multiplexed flip-flops.

3.10.3 Sequential Timing Characteristics

The following figures show sequential timing characteristics.

Figure 26 • **Input Buffer Latches**



approximately a 3 ns to a 6 ns delay, which is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section, shown in Table 34, page 41.

3.11.3 Timing Derating

MX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature and worst-case processing.

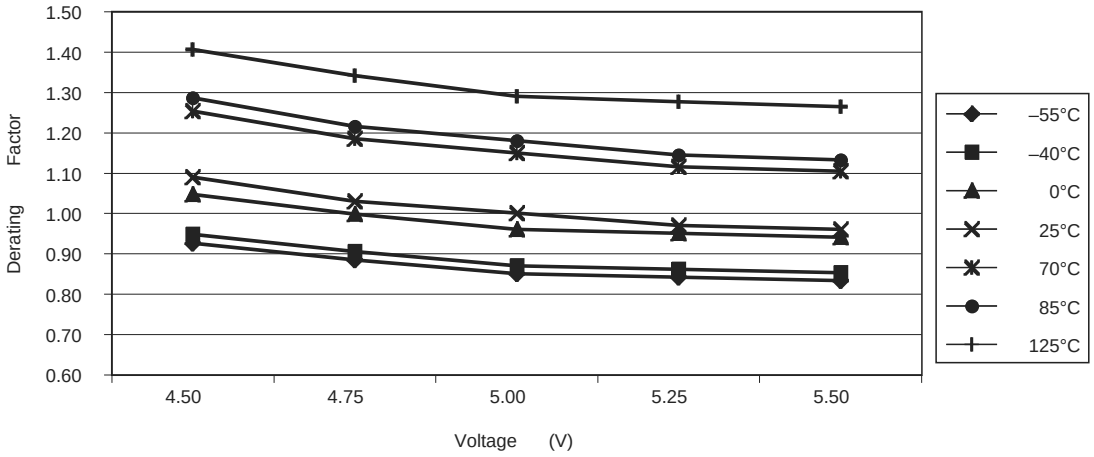
3.11.4 Temperature and Voltage Derating Factors

The following tables and figures show temperature and voltage derating factors for 40MX and 42MX FPGAs.

Table 28 • **42MX Temperature and Voltage Derating Factors (Normalized to T_J = 25°C, VCCA = 5.0 V)**

	Temperature						
42MX Voltage	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
4.50	0.93	0.95	1.05	1.09	1.25	1.29	1.41
4.75	0.88	0.90	1.00	1.03	1.18	1.22	1.34
5.00	0.85	0.87	0.96	1.00	1.15	1.18	1.29
5.25	0.84	0.86	0.95	0.97	1.12	1.14	1.28
5.50	0.83	0.85	0.94	0.96	1.10	1.13	1.26

Figure 34 • **42MX Junction Temperature and Voltage Derating Curves (Normalized to TJ = 25°C, VCCA = 5.0 V)**



Note: This derating factor applies to all routing and propagation delays

Table 29 • **40MX Temperature and Voltage Derating Factors(Normalized to TJ = 25°C, VCC = 5.0 V)**

	Temperature						
40MX Voltage	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
4.50	0.89	0.93	1.02	1.09	1.25	1.31	1.45
4.75	0.84	0.88	0.97	1.03	1.18	1.24	1.37
5.00	0.82	0.85	0.94	1.00	1.15	1.20	1.33
5.25	0.80	0.82	0.91	0.97	1.12	1.16	1.29
5.50	0.79	0.82	0.90	0.96	1.10	1.15	1.28

Table 40 • **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RD3}	FO = 3 Routing Delay			1.3		1.4		1.6		1.9		2.7	ns
t_{RD4}	FO = 4 Routing Delay			1.6		1.7		2.0		2.3		3.2	ns
t_{RD8}	FO = 8 Routing Delay			2.6		2.9		3.2		3.8		5.3	ns
Logic Module Sequential Timing[3,4]													
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up		0.3		0.4		0.4		0.5		0.7		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up		0.7		0.8		0.9		1.0		1.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		3.4		3.8		4.3		5.0		7.1		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		4.5		5.0		5.6		6.6		9.2		ns
t_A	Flip-Flop Clock Input Period		6.8		7.6		8.6		10.1		14.1		ns
t_{INH}	Input Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Set-Up		0.5		0.5		0.6		0.7		1.0		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up		0.5		0.5		0.6		0.7		1.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency			215		195		179		156		94	MHz
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			1.1		1.2		1.3		1.6		2.2	ns
t_{INYL}	Pad-to-Y LOW			0.8		0.9		1.0		1.2		1.7	ns
t_{INGH}	G to Y HIGH			1.4		1.6		1.8		2.1		2.9	ns
t_{INGL}	G to Y LOW			1.4		1.6		1.8		2.1		2.9	ns
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			1.8		2.0		2.3		2.7		4.0	ns
t_{IRD2}	FO = 2 Routing Delay			2.1		2.3		2.6		3.1		4.3	ns
t_{IRD3}	FO = 3 Routing Delay			2.3		2.6		3.0		3.5		4.9	ns
t_{IRD4}	FO = 4 Routing Delay			2.6		3.0		3.3		3.9		5.4	ns
t_{IRD8}	FO = 8 Routing Delay			3.6		4.0		4.6		5.4		7.5	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		2.6		2.9		3.3		3.9		5.4	ns
		FO = 384		2.9		3.2		3.6		4.3		6.0	ns
t_{CKL}	Input HIGH to LOW	FO = 32		3.8		4.2		4.8		5.6		7.8	ns
		FO = 384		4.5		5.0		5.6		6.6		9.2	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	3.2		3.5		4.0		4.7		6.6		ns
		FO = 384	3.7		4.1		4.6		5.4		7.6		ns

Table 41 • **A42MX16 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PWL}	Minimum Pulse Width LOW	FO = 32	5.3		5.9		6.7		7.8		11.0		ns
		FO = 384	6.2		6.9		7.9		9.2		12.9		ns
t_{CKSW}	Maximum Skew	FO = 32		0.5		0.5		0.6		0.7		1.0	ns
		FO = 384		2.2		2.4		2.7		3.2		4.5	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 384	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	3.9		4.3		4.9		5.7		8.0		ns
		FO = 384	4.5		4.9		5.6		6.6		9.2		ns
t_P	Minimum Period	FO = 32	7.0		7.8		8.4		9.7		16.2		ns
		FO = 384	7.7		8.6		9.3		10.7		17.8		ns
f_{MAX}	Maximum Frequency	FO = 32		142		129		119		103		62	MHz
		FO = 384		129		117		108		94		56	MHz
TTL Output Module Timing[5]													
t_{DLH}	Data-to-Pad HIGH			3.5		3.9		4.4		5.2		7.3	ns
t_{DHL}	Data-to-Pad LOW			4.1		4.6		5.2		6.1		8.6	ns
t_{ENZH}	Enable Pad Z to HIGH			3.8		4.2		4.8		5.6		7.8	ns
t_{ENZL}	Enable Pad Z to LOW			4.2		4.6		5.3		6.2		8.7	ns
t_{ENHZ}	Enable Pad HIGH to Z			7.6		8.4		9.5		11.2		15.7	ns
t_{ENLZ}	Enable Pad LOW to Z			7.0		7.8		8.8		10.4		14.5	ns
t_{GLH}	G-to-Pad HIGH			4.8		5.3		6.0		7.2		10.0	ns
t_{GHL}	G-to-Pad LOW			4.8		5.3		6.0		7.2		10.0	ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading			8.0		8.9		10.1		11.9		16.7	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading			11.3		12.5		14.2		16.7		23.3	ns
d_{TLH}	Capacitive Loading, LOW to HIGH			0.04		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW			0.05		0.05		0.06		0.07		0.10	ns/pF
CMOS Output Module Timing[5]													
t_{DLH}	Data-to-Pad HIGH			4.5		5.0		5.6		6.6		9.3	ns
t_{DHL}	Data-to-Pad LOW			3.4		3.8		4.3		5.1		7.1	ns
t_{ENZH}	Enable Pad Z to HIGH			3.8		4.2		4.8		5.6		7.8	ns
t_{ENZL}	Enable Pad Z to LOW			4.2		4.6		5.3		6.2		8.7	ns
t_{ENHZ}	Enable Pad HIGH to Z			7.6		8.4		9.5		11.2		15.7	ns
t_{ENLZ}	Enable Pad LOW to Z			7.0		7.8		8.8		10.4		14.5	ns
t_{GLH}	G-to-Pad HIGH			7.1		7.9		8.9		10.5		14.7	ns
t_{GHL}	G-to-Pad LOW			7.1		7.9		8.9		10.5		14.7	ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading			8.0		8.9		10.1		11.9		16.7	ns

Table 44 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions[1]												
t_{PD}	Internal Array Module Delay		1.3		1.5		1.7		2.0		2.7	ns
t_{PDD}	Internal Decode Module Delay		1.6		1.8		2.0		2.4		3.3	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.2		1.4		2.0	ns
t_{RD2}	FO = 2 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t_{RD3}	FO =3 Routing Delay		1.6		1.8		2.0		2.4		3.4	ns
t_{RD4}	FO = 4 Routing Delay		2.0		2.2		2.5		2.9		4.1	ns
t_{RD5}	FO = 8 Routing Delay		3.3		3.7		4.2		4.9		6.9	ns
t_{RDD}	Decode-to-Output Routing Delay		0.3		0.4		0.4		0.5		0.7	ns
Logic Module Sequential Timing[3, 4]												
t_{CO}	Flip-Flop Clock-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch Gate-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t_{SUD}	Flip-Flop (Latch) Set-Up Time	0.3		0.3		0.4		0.5		0.7		ns
t_{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		1.6		1.7		2.0		2.3		3.2	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.5		6.4		9.0		ns
Synchronous SRAM Operations												
t_{RC}	Read Cycle Time	6.8		7.5		8.5		10.0		14.0		ns
t_{WC}	Write Cycle Time	6.8		7.5		8.5		10.0		14.0		ns
t_{RCKHL}	Clock HIGH/LOW Time	3.4		3.8		4.3		5.0		7.0		ns
t_{RCO}	Data Valid After Clock HIGH/LOW		3.4		3.8		4.3		5.0		7.0	ns
t_{ADSU}	Address/Data Set-Up Time	1.6		1.8		2.0		2.4		3.4		ns
Synchronous SRAM Operations (continued)												
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Set-Up	0.6		0.7		0.8		0.9		1.3		ns
t_{RENH}	Read Enable Hold	3.4		3.8		4.3		5.0		7.0		ns
t_{WENSU}	Write Enable Set-Up	2.7		3.0		3.4		4.0		5.6		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Set-Up	2.8		3.1		3.5		4.1		5.7		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		ns

Table 44 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 635	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	2.8		3.2		3.6		4.2		5.9		ns
		FO = 635	3.3		3.7		4.2		4.9		6.9		ns
t_P	Minimum Period ($1/f_{MAX}$)	FO = 32	5.5		6.1		6.6		7.6		12.7		ns
		FO = 635	6.0		6.6		7.2		8.3		13.8		ns
f_{MAX}	Maximum Datapath Frequency	FO = 32		180		164		151		131		79	MHz
		FO = 635		166		151		139		121		73	MHz
TTL Output Module Timing[5]													
t_{DLH}	Data-to-Pad HIGH			2.6		2.8		3.2		3.8		5.3	ns
t_{DHL}	Data-to-Pad LOW			3.0		3.3		3.7		4.4		6.2	ns
t_{ENZH}	Enable Pad Z to HIGH			2.7		3.0		3.3		3.9		5.5	ns
t_{ENZL}	Enable Pad Z to LOW			3.0		3.3		3.7		4.3		6.1	ns
t_{ENHZ}	Enable Pad HIGH to Z			5.3		5.8		6.6		7.8		10.9	ns

Table 45 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.9		12.1		13.7		16.1		22.5	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.10		0.11		0.12		0.14		0.20	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.10		0.11		0.12		0.14		0.20	ns/pF
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		4.9		5.5		6.2		7.3		10.3	ns
t_{DHL}	Data-to-Pad LOW		3.4		3.8		4.3		5.1		7.1	ns
t_{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.7		5.5		7.7	ns
t_{ENZL}	Enable Pad Z to LOW		4.1		4.6		5.2		6.1		8.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.4		8.2		9.3		10.9		15.3	ns
t_{ENLZ}	Enable Pad LOW to Z		6.9		7.6		8.7		10.2		14.3	ns
t_{GLH}	G-to-Pad HIGH		7.0		7.8		8.9		10.4		14.6	ns
t_{GHL}	G-to-Pad LOW		7.0		7.8		8.9		10.4		14.6	ns
t_{LSU}	I/O Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.9		8.8		10.0		11.8		16.5	ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. Delays based on 35 pF loading.

3.12 Pin Descriptions

This section lists the pin descriptions for 40MX and 42MX series FPGAs.

CLK/A/B, I/O Global Clock

Clock inputs for clock distribution networks. CLK is for 40MX while CLKA and CLKB are for 42MX devices. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK, I/ODiagnostic Clock

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND, Ground

Input LOW supply voltage.

I/O, Input/Output

Figure 42 • **PQ144**

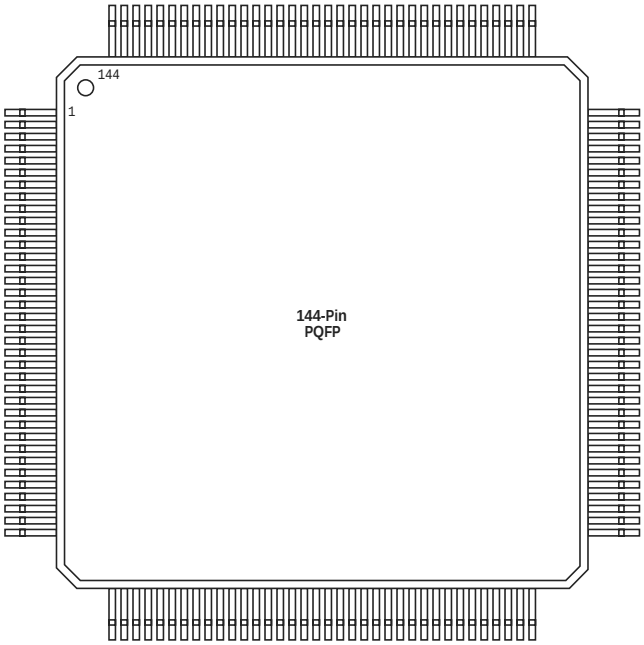


Table 51 • **PQ144**

PQ144	
Pin Number	**A42MX09 Function**
1	I/O
2	MODE
3	I/O
4	I/O
5	I/O

Table 51 • **PQ144**

PQ144	
Pin Number	**A42MX09 Function**
117	GNDI
118	NC
119	I/O
120	I/O
121	I/O
122	I/O
123	PROBA
124	I/O
125	CLKA
126	VCC
127	VCCI
128	NC
129	I/O
130	CLKB
131	I/O
132	PROBB
133	I/O
134	I/O
135	I/O
136	GND
137	GNDI
138	NC
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	DCLK

Table 52 • **PQ160**

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
95	I/O	I/O	I/O
96	I/O	I/O	WD, I/O
97	I/O	I/O	I/O
98	VCCA	VCCA	VCCA
99	GND	GND	GND
100	NC	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	NC	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	WD, I/O
107	I/O	I/O	WD, I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	NC	I/O	I/O
111	I/O	I/O	WD, I/O
112	I/O	I/O	WD, I/O
113	I/O	I/O	I/O
114	NC	VCCI	VCCI
115	I/O	I/O	WD, I/O
116	NC	I/O	WD, I/O
117	I/O	I/O	I/O
118	I/O	I/O	TDI, I/O
119	I/O	I/O	TMS, I/O
120	GND	GND	GND
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	NC	I/O	I/O
125	GND	GND	GND
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	NC	I/O	I/O
130	GND	GND	GND
131	I/O	I/O	I/O

Table 54 • **PQ240**

PQ240	
Pin Number	**A42MX36 Function**
163	WD, I/O
164	WD, I/O
165	I/O
166	QCLKA, I/O
167	I/O
168	I/O
169	I/O
170	I/O
171	I/O
172	VCCI
173	I/O
174	WD, I/O
175	WD, I/O
176	I/O
177	I/O
178	TDI, I/O
179	TMS, I/O
180	GND
181	VCCA
182	GND
183	I/O
184	I/O
185	I/O
186	I/O
187	I/O
188	I/O
189	I/O
190	I/O
191	I/O
192	VCCI
193	I/O
194	I/O
195	I/O
196	I/O
197	I/O
198	I/O
199	I/O

Table 58 • **CQ208**

CQ208	
Pin Number	**A42MX36 Function**
185	I/O
186	CLKB, I/O
187	I/O
188	PRB, I/O
189	I/O
190	WD, I/O
191	WD, I/O
192	I/O
193	I/O
194	WD, I/O
195	WD, I/O
196	QCLKC, I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	I/O
202	VCCI
203	WD, I/O
204	WD, I/O
205	I/O
206	I/O
207	DCLK, I/O
208	I/O

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
207	I/O
208	I/O
209	QCLKC, I/O
210	I/O
211	WD, I/O
212	WD, I/O
213	I/O
214	I/O
215	WD, I/O
216	WD, I/O
217	I/O
218	PRB, I/O
219	I/O
220	CLKB, I/O
221	I/O
222	GND
223	GND
224	VCCA
225	VCCI
226	I/O
227	CLKA, I/O
228	I/O
229	PRA, I/O
230	I/O
231	I/O
232	WD, I/O
233	WD, I/O
234	I/O
235	I/O
236	I/O
237	I/O
238	I/O
239	I/O
240	QCLKD, I/O
241	I/O
242	WD, I/O
243	GND

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
244	WD, I/O
245	I/O
246	I/O
247	I/O
248	VCCI
249	I/O
250	WD, I/O
251	WD, I/O
252	I/O
253	SDI, I/O
254	I/O
255	GND
256	NC

Figure 51 • **BG272**

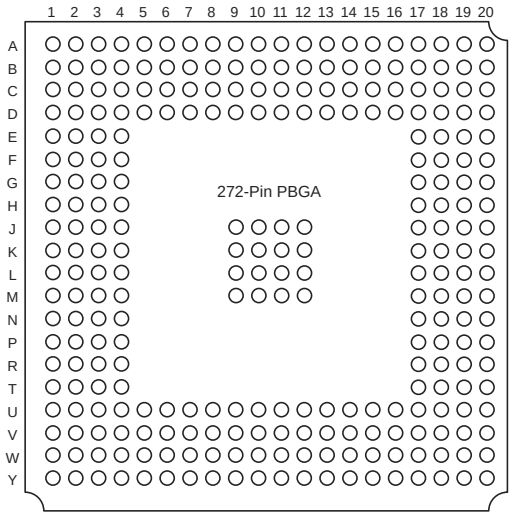


Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
A1	GND
A2	GND
A3	I/O
A4	WD, I/O
A5	I/O

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
A6	I/O
A7	WD, I/O
A8	WD, I/O
A9	I/O
A10	I/O
A11	CLKA
A12	I/O
A13	I/O
A14	I/O
A15	I/O
A16	WD, I/O
A17	I/O
A18	I/O
A19	GND
A20	GND
B1	GND
B2	GND
B3	DCLK, I/O
B4	I/O
B5	I/O
B6	I/O
B7	WD, I/O
B8	I/O
B9	PRB, I/O
B10	I/O
B11	I/O
B12	WD, I/O
B13	I/O
B14	I/O
B15	WD, I/O
B16	I/O
B17	WD, I/O
B18	I/O
B19	GND
B20	GND
C1	I/O
C2	MODE

Table 61 • **PG132**

PG132	
Pin Number	**A42MX09 Function**
F2	I/O
F1	I/O
G1	I/O
G4	VSV
H1	I/O
H2	I/O
H3	I/O
H4	I/O
J1	I/O
K1	I/O
L1	I/O
K2	I/O
M1	I/O
K3	I/O
L2	I/O
N1	I/O
L3	BININ
M2	BINOUT
N2	I/O
M3	I/O
L4	I/O
N3	I/O
M4	I/O
N4	I/O
M5	I/O
K6	I/O
N5	I/O
N6	I/O
L6	I/O
M6	I/O
M7	I/O
N7	I/O
N8	I/O
M8	I/O
L8	I/O
K8	I/O
N9	I/O

Table 61 • **PG132**

PG132	
Pin Number	**A42MX09 Function**
B3	I/O
A2	I/O
C3	DCLK
B5	GNDA
E12	GNDA
J2	GNDA
M9	GNDA
B9	GNDI
C5	GNDI
E11	GNDI
F4	GNDI
J3	GNDI
J11	GNDI
L5	GNDI
L9	GNDI
C9	GNDQ
E3	GNDQ
K12	GNDQ
D7	VCCA
G3	VCCA
G10	VCCA
L7	VCCA
C7	VCCI
G2	VCCI
G11	VCCI
K7	VCCI

Figure 53 • **CQ172**

Table 62 • **CQ172**

CQ172	
Pin Number	**A42MX16 Function**
1	MODE
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	GND
8	I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	I/O
17	GND
18	I/O
19	I/O
20	I/O