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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	57
Number of Gates	6000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-plg68

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- VCCA = Power supply in volts (V)
- F = Switching frequency in megahertz (MHz)

3.4.4 Equivalent Capacitance

Equivalent capacitance is calculated by measuring ICC_{active} at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

3.4.5 C_{EQ} Values for Microsemi MX FPGAs

Modules (C_{EQM}) 3.5

Input Buffers (C_{EQI}) 6.9

Output Buffers (C_{EQO}) 18.2

Routed Array Clock Buffer Loads (C_{EQCR}) 1.4

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. The equation below shows a piece-wise linear summation over all components.

$$\text{Power} = VCCA^2 * [(m \times C_{EQM} * f_m)_{\text{modules}} + (n * C_{EQI} * f_n)_{\text{inputs}} + (p * (C_{EQO} + C_L) * f_p)_{\text{outputs}} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{\text{routed_clk1}} + (r_1 * f_{q1})_{\text{routed_clk1}} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{\text{routed_clk2}} + (r_2 * f_{q2})_{\text{routed_clk2}}] \quad (2)$$

EQ 3

where:

m = Number of logic modules switching at frequency f_m

n = Number of input buffers switching at frequency f_n

p = Number of output buffers switching at frequency f_p

q₁ = Number of clock loads on the first routed array clock

q₂ = Number of clock loads on the second routed array clock

r₁ = Fixed capacitance due to first routed array clock

r₂ = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output load capacitance in pF

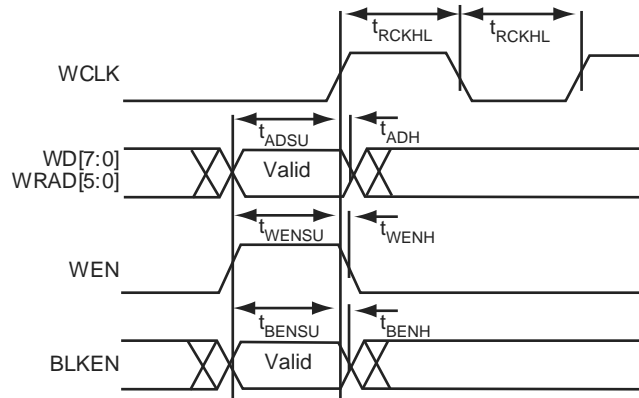
f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

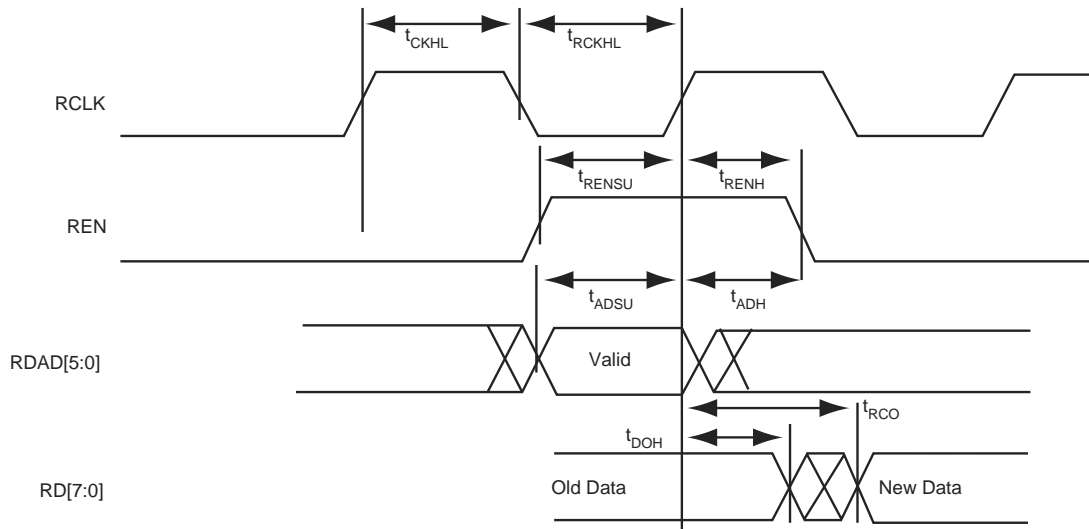
f_{q1} = Average first routed array clock rate in MHz

Figure 30 • 42MX SRAM Write Operation



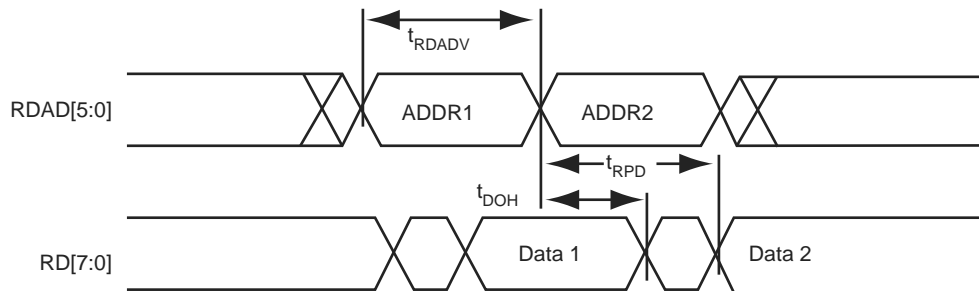
Note: Identical timing for falling edge clock

Figure 31 • 42MX SRAM Synchronous Read Operation



Note: Identical timing for falling edge clock

Figure 32 • 42MX SRAM Asynchronous Read Operation—Type 1 (Read Address Controlled)



approximately a 3 ns to a 6 ns delay, which is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section, shown in Table 34, page 41.

3.11.3 Timing Derating

MX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature and worst-case processing.

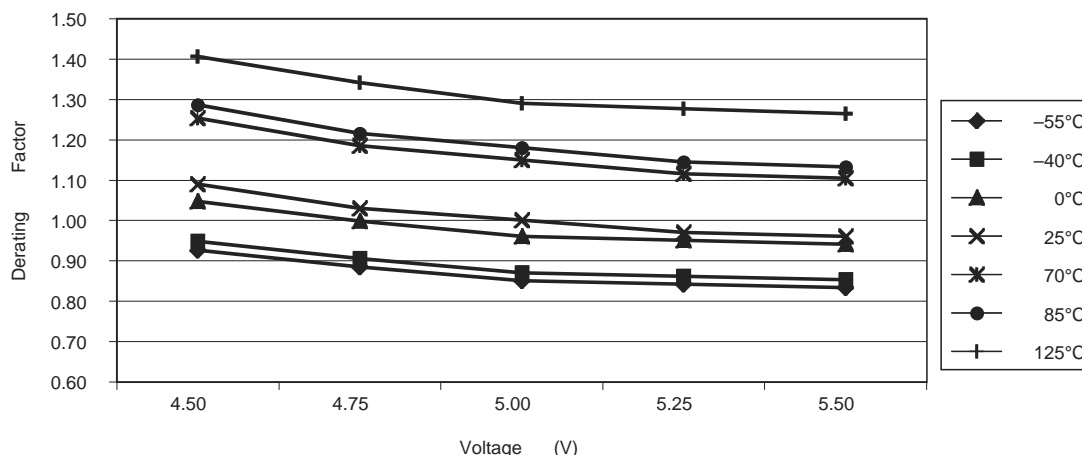
3.11.4 Temperature and Voltage Derating Factors

The following tables and figures show temperature and voltage derating factors for 40MX and 42MX FPGAs.

Table 28 • 42MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 5.0\text{ V}$)

42MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.93	0.95	1.05	1.09	1.25	1.29	1.41
4.75	0.88	0.90	1.00	1.03	1.18	1.22	1.34
5.00	0.85	0.87	0.96	1.00	1.15	1.18	1.29
5.25	0.84	0.86	0.95	0.97	1.12	1.14	1.28
5.50	0.83	0.85	0.94	0.96	1.10	1.13	1.26

Figure 34 • 42MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 5.0\text{ V}$)



Note: This derating factor applies to all routing and propagation delays

Table 29 • 40MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.89	0.93	1.02	1.09	1.25	1.31	1.45
4.75	0.84	0.88	0.97	1.03	1.18	1.24	1.37
5.00	0.82	0.85	0.94	1.00	1.15	1.20	1.33
5.25	0.80	0.82	0.91	0.97	1.12	1.16	1.29
5.50	0.79	0.82	0.90	0.96	1.10	1.15	1.28

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PWL}	Minimum Pulse Width LOW	FO = 32	3.2	3.5	4.0	4.7	6.6	ns					
		FO = 384	3.7	4.1	4.6	5.4	7.6	ns					
t _{CKSW}	Maximum Skew	FO = 32	0.3	0.4	0.4	0.5	0.7	ns					
		FO = 384	0.3	0.4	0.4	0.5	0.7	ns					
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0	0.0	0.0	0.0	0.0	ns					
		FO = 384	0.0	0.0	0.0	0.0	0.0	ns					
t _{HEXT}	Input Latch External Hold	FO = 32	2.8	3.1	5.5	4.1	5.7	ns					
		FO = 384	3.2	3.5	4.0	4.7	6.6	ns					
t _P	Minimum Period	FO = 32	4.2	4.67	5.1	5.8	9.7	ns					
		FO = 384	4.6	5.1	5.6	6.4	10.7	ns					
f _{MAX}	Maximum Frequency	FO = 32	237	215	198	172	103	MHz					
		FO = 384	215	195	179	156	94	MHz					

Table 41 • A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PWL}	Minimum Pulse Width LOW	FO = 32	5.3	5.9	6.7	7.8	11.0	ns					
		FO = 384	6.2	6.9	7.9	9.2	12.9	ns					
t _{CKSW}	Maximum Skew	FO = 32	0.5	0.5	0.6	0.7	1.0	ns					
		FO = 384	2.2	2.4	2.7	3.2	4.5	ns					
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0	0.0	0.0	0.0	0.0	ns					
		FO = 384	0.0	0.0	0.0	0.0	0.0	ns					
t _{HEXT}	Input Latch External Hold	FO = 32	3.9	4.3	4.9	5.7	8.0	ns					
		FO = 384	4.5	4.9	5.6	6.6	9.2	ns					
t _P	Minimum Period	FO = 32	7.0	7.8	8.4	9.7	16.2	ns					
		FO = 384	7.7	8.6	9.3	10.7	17.8	ns					
f _{MAX}	Maximum Frequency	FO = 32	142	129	119	103	62	MHz					
		FO = 384	129	117	108	94	56	MHz					
TTL Output Module Timing⁵													
t _{DLH}	Data-to-Pad HIGH		3.5	3.9	4.4	5.2	7.3	ns					
t _{DHL}	Data-to-Pad LOW		4.1	4.6	5.2	6.1	8.6	ns					
t _{ENZH}	Enable Pad Z to HIGH		3.8	4.2	4.8	5.6	7.8	ns					
t _{ENZL}	Enable Pad Z to LOW		4.2	4.6	5.3	6.2	8.7	ns					
t _{ENHZ}	Enable Pad HIGH to Z		7.6	8.4	9.5	11.2	15.7	ns					
t _{ENLZ}	Enable Pad LOW to Z		7.0	7.8	8.8	10.4	14.5	ns					
t _{GLH}	G-to-Pad HIGH		4.8	5.3	6.0	7.2	10.0	ns					
t _{GHL}	G-to-Pad LOW		4.8	5.3	6.0	7.2	10.0	ns					
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.0	8.9	10.1	11.9	16.7	ns					
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		11.3	12.5	14.2	16.7	23.3	ns					
d _{TLH}	Capacitive Loading, LOW to HIGH		0.04	0.04	0.05	0.06	0.08	ns/pF					
d _{THL}	Capacitive Loading, HIGH to LOW		0.05	0.05	0.06	0.07	0.10	ns/pF					
CMOS Output Module Timing⁵													
t _{DLH}	Data-to-Pad HIGH		4.5	5.0	5.6	6.6	9.3	ns					
t _{DHL}	Data-to-Pad LOW		3.4	3.8	4.3	5.1	7.1	ns					
t _{ENZH}	Enable Pad Z to HIGH		3.8	4.2	4.8	5.6	7.8	ns					
t _{ENZL}	Enable Pad Z to LOW		4.2	4.6	5.3	6.2	8.7	ns					
t _{ENHZ}	Enable Pad HIGH to Z		7.6	8.4	9.5	11.2	15.7	ns					
t _{ENLZ}	Enable Pad LOW to Z		7.0	7.8	8.8	10.4	14.5	ns					
t _{GLH}	G-to-Pad HIGH		7.1	7.9	8.9	10.5	14.7	ns					
t _{GHL}	G-to-Pad LOW		7.1	7.9	8.9	10.5	14.7	ns					
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.0	8.9	10.1	11.9	16.7	ns					

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays²												
t _{IRD1}	FO = 1 Routing Delay		2.6		2.9		3.2		3.8		5.3	ns
t _{IRD2}	FO = 2 Routing Delay		2.9		3.2		3.6		4.3		6.0	ns
t _{IRD3}	FO = 3 Routing Delay		3.2		3.6		4.0		4.8		6.6	ns
t _{IRD4}	FO = 4 Routing Delay		3.5		3.9		4.4		5.2		7.3	ns
t _{IRD8}	FO = 8 Routing Delay		4.8		5.3		6.1		7.1		10.0	ns
Global Clock Network												
t _{CKH}	Input LOW to HIGH	FO = 32	4.4		4.8		5.5		6.5		9.1	ns
		FO = 486	4.8		5.3		6.0		7.1		10.0	ns
t _{CKL}	Input HIGH to LOW	FO = 32	5.1		5.7		6.4		7.6		10.6	ns
		FO = 486	6.0		6.6		7.5		8.8		12.4	ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	3.0		3.3		3.8		4.5		6.3	ns
		FO = 486	3.3		3.7		4.2		4.9		6.9	ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	3.0		3.4		3.8		4.5		6.3	ns
		FO = 486	3.3		3.7		4.2		4.9		6.9	ns
t _{CKSW}	Maximum Skew	FO = 32	0.8		0.8		1.0		1.1		1.6	ns
		FO = 486	0.8		0.8		1.0		1.1		1.6	ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0	ns
		FO = 486	0.0		0.0		0.0		0.0		0.0	ns
TTL Output Module Timing⁵												
t _{DLH}	Data-to-Pad HIGH		3.4		3.8		4.3		5.0		7.1	ns
t _{DHL}	Data-to-Pad LOW		4.0		4.4		5.0		5.9		8.3	ns
t _{ENZH}	Enable Pad Z to HIGH		3.6		4.0		4.5		5.3		7.4	ns
t _{ENZL}	Enable Pad Z to LOW		3.9		4.4		5.0		5.8		8.2	ns
t _{ENHZ}	Enable Pad HIGH to Z		7.2		8.0		9.1		10.7		14.9	ns
t _{ENLZ}	Enable Pad LOW to Z		6.7		7.5		8.5		9.9		13.9	ns
t _{GLH}	G-to-Pad HIGH		4.8		5.3		6.0		7.2		10.0	ns
t _{GHL}	G-to-Pad LOW		4.8		5.3		6.0		7.2		10.0	ns
t _{LSU}	I/O Latch Output Set-Up		0.7		0.7		0.8		1.0		1.4	ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Asynchronous SRAM Operations												
t _{RPD}	Asynchronous Access Time		8.1		9.0		10.2		12.0		16.8	ns
t _{RDADV}	Read Address Valid		8.8		9.8		11.1		13.0		18.2	ns
t _{ADSU}	Address/Data Set-Up Time		1.6		1.8		2.0		2.4		3.4	ns
t _{ADH}	Address/Data Hold Time		0.0		0.0		0.0		0.0		0.0	ns
t _{RENSUA}	Read Enable Set-Up to Address Valid		0.6		0.7		0.8		0.9		1.3	ns
t _{RENHA}	Read Enable Hold		3.4		3.8		4.3		5.0		7.0	ns
t _{WENSU}	Write Enable Set-Up		2.7		3.0		3.4		4.0		5.6	ns
t _{WENH}	Write Enable Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{DOH}	Data Out Hold Time		1.2		1.3		1.5		1.8		2.5	ns
Input Module Propagation Delays												
t _{INPY}	Input Data Pad-to-Y		1.0		1.1		1.3		1.5		2.1	ns
t _{INGO}	Input Latch Gate-to-Output		1.4		1.6		1.8		2.1		2.9	ns
t _{INH}	Input Latch Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{INSU}	Input Latch Set-Up		0.5		0.5		0.6		0.7		1.0	ns
t _{ILA}	Latch Active Pulse Width		4.7		5.2		5.9		6.9		9.7	ns
Input Module Predicted Routing Delays²												
t _{IRD1}	FO = 1 Routing Delay		2.0		2.2		2.5		2.9		4.1	ns
t _{IRD2}	FO = 2 Routing Delay		2.3		2.6		2.9		3.4		4.8	ns
t _{IRD3}	FO = 3 Routing Delay		2.6		2.9		3.3		3.9		5.5	ns
t _{IRD4}	FO = 4 Routing Delay		3.0		3.3		3.8		4.4		6.2	ns
t _{IRD8}	FO = 8 Routing Delay		4.3		4.8		5.5		6.4		9.0	ns
Global Clock Network												
t _{CKH}	Input LOW to HIGH	FO = 32	2.7		3.0		3.4		4.0		5.6	ns
		FO = 635	3.0		3.3		3.8		4.4		6.2	ns
t _{CKL}	Input HIGH to LOW	FO = 32	3.8		4.2		4.8		5.6		7.8	ns
		FO = 635	4.9		5.4		6.1		7.2		10.1	ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	1.8		2.0		2.2		2.6		3.6	ns
		FO = 635	2.0		2.2		2.5		2.9		4.1	ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	1.8		2.0		2.2		2.6		3.6	ns
		FO = 635	2.0		2.2		2.5		2.9		4.1	ns
t _{CKSW}	Maximum Skew	FO = 32	0.8		0.8		0.9		1.0		1.4	ns
		FO = 635	0.8		0.8		0.9		1.0		1.4	ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing⁵											
t _{DLH}	Data-to-Pad HIGH	3.5	3.9	4.5	5.2	7.3	ns				
t _{DHL}	Data-to-Pad LOW	2.5	2.7	3.1	3.6	5.1	ns				
t _{ENZH}	Enable Pad Z to HIGH	2.7	3.0	3.3	3.9	5.5	ns				
t _{ENZL}	Enable Pad Z to LOW	2.9	3.3	3.7	4.3	6.1	ns				
t _{ENHZ}	Enable Pad HIGH to Z	5.3	5.8	6.6	7.8	10.9	ns				
t _{ENLZ}	Enable Pad LOW to Z	4.9	5.5	6.2	7.3	10.2	ns				
t _{GLH}	G-to-Pad HIGH	5.0	5.6	6.3	7.5	10.4	ns				
t _{GHL}	G-to-Pad LOW	5.0	5.6	6.3	7.5	10.4	ns				
t _{LSU}	I/O Latch Set-Up	0.5	0.5	0.6	0.7	1.0	ns				
t _{LH}	I/O Latch Hold	0.0	0.0	0.0	0.0	0.0	ns				
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O	5.7	6.3	7.1	8.4	11.8	ns				
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O	7.8	8.6	9.8	11.5	16.1	ns				
d _{TLH}	Capacitive Loading, LOW to HIGH	0.07	0.08	0.09	0.10	0.14	ns/pF				
d _{THL}	Capacitive Loading, HIGH to LOW	0.07	0.08	0.09	0.10	0.14	ns/pF				

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions¹											
t _{PD}	Internal Array Module Delay	1.9	2.1	2.3	2.7	3.8	ns				
t _{PDD}	Internal Decode Module Delay	2.2	2.5	2.8	3.3	4.7	ns				
Logic Module Predicted Routing Delays²											
t _{RD1}	FO = 1 Routing Delay	1.3	1.5	1.7	2.0	2.7	ns				
t _{RD2}	FO = 2 Routing Delay	1.8	2.0	2.3	2.7	3.7	ns				
t _{RD3}	FO = 3 Routing Delay	2.3	2.5	2.8	3.4	4.7	ns				
t _{RD4}	FO = 4 Routing Delay	2.8	3.1	3.5	4.1	5.7	ns				

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RD5} FO = 8 Routing Delay		4.6		5.2		5.8		6.9		9.6	ns
t _{RDD} Decode-to-Output Routing Delay		0.5		0.5		0.6		0.7		1.0	ns
Logic Module Sequential Timing^{3, 4}											
t _{CO} Flip-Flop Clock-to-Output		1.8		2.0		2.3		2.7		3.7	ns
t _{GO} Latch Gate-to-Output		1.8		2.0		2.3		2.7		3.7	ns
t _{SUD} Flip-Flop (Latch) Set-Up Time	0.4		0.5		0.6		0.7		0.9		ns
t _{HD} Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RO} Flip-Flop (Latch) Reset-to-Output		2.2		2.4		2.7		3.2		4.5	ns
t _{SUENA} Flip-Flop (Latch) Enable Set-Up	1.0		1.1		1.2		1.4		2.0		ns
t _{HENA} Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA} Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.2		5.8		6.9		9.6		ns
t _{WASYN} Flip-Flop (Latch) Asynchronous Pulse Width	6.1		6.8		7.7		9.0		12.6		ns
Synchronous SRAM Operations											
t _{RC} Read Cycle Time		9.5		10.5		11.9		14.0		19.6	ns
t _{WC} Write Cycle Time		9.5		10.5		11.9		14.0		19.6	ns
t _{RCKHL} Clock HIGH/LOW Time		4.8		5.3		6.0		7.0		9.8	ns
t _{RCO} Data Valid After Clock HIGH/LOW		4.8		5.3		6.0		7.0		9.8	ns
t _{ADSU} Address/Data Set-Up Time		2.3		2.5		2.8		3.4		4.8	ns

4 Package Pin Assignments

The following figures and tables give the details of the package pin assignments.

Figure 38 • PL44

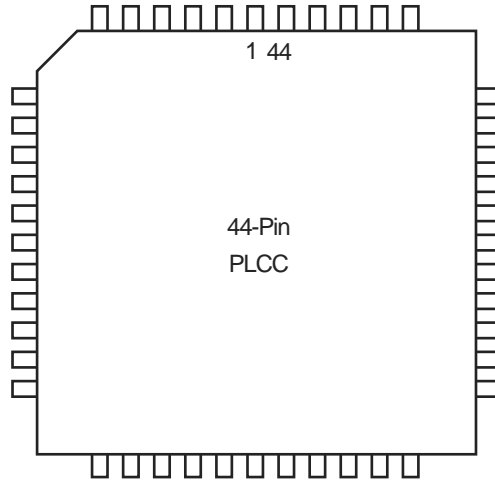


Table 47 • PL44

PL44		
Pin Number	A40MX02 Function	A40MX04 Function
1	I/O	I/O
2	I/O	I/O
3	VCC	VCC
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	GND	GND
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	VCC	VCC
15	I/O	I/O
16	VCC	VCC
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O

Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
47	I/O	I/O	I/O	WD, I/O
48	I/O	I/O	I/O	I/O
49	I/O	GND	GND	GND
50	I/O	I/O	I/O	WD, I/O
51	I/O	I/O	I/O	WD, I/O
52	I/O	SDO, I/O	SDO, I/O	SDO, TDO, I/O
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	GND	I/O	I/O	I/O
61	GND	I/O	I/O	I/O
62	I/O	I/O	I/O	TCK, I/O
63	I/O	LP	LP	LP
64	CLK, I/O	VCCA	VCCA	VCCA
65	I/O	VCCI	VCCI	VCCI
66	MODE	I/O	I/O	I/O
67	VCC	I/O	I/O	I/O
68	VCC	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	GND	GND	GND
71	I/O	I/O	I/O	I/O
72	SDI, I/O	I/O	I/O	I/O
73	DCLK, I/O	I/O	I/O	I/O
74	PRA, I/O	I/O	I/O	I/O
75	PRB, I/O	I/O	I/O	I/O
76	I/O	SDI, I/O	SDI, I/O	SDI, I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	WD, I/O
79	I/O	I/O	I/O	WD, I/O
80	I/O	I/O	I/O	WD, I/O
81	I/O	PRA, I/O	PRA, I/O	PRA, I/O
82	GND	I/O	I/O	I/O
83	I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O

Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	VCCA	VCCA
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	VCCA	VCCA
139	VCCI	VCCI	VCCI
140	GND	GND	GND
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	GND	GND	GND
146	NC	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	NC	VCCA	VCCA
151	NC	I/O	I/O
152	NC	I/O	I/O
153	NC	I/O	I/O
154	NC	I/O	I/O
155	GND	GND	GND
156	I/O	I/O	I/O
157	I/O	I/O	I/O
158	I/O	I/O	I/O
159	MODE	MODE	MODE
160	GND	GND	GND

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
15	QCLKC, I/O
16	I/O
17	WD, I/O
18	WD, I/O
19	I/O
20	I/O
21	WD, I/O
22	WD, I/O
23	I/O
24	PRB, I/O
25	I/O
26	CLKB, I/O
27	I/O
28	GND
29	VCCA
30	VCCI
31	I/O
32	CLKA, I/O
33	I/O
34	PRA, I/O
35	I/O
36	I/O
37	WD, I/O
38	WD, I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	QCLKD, I/O
46	I/O
47	WD, I/O
48	WD, I/O
49	I/O
50	I/O
51	I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
52	VCCI
53	I/O
54	WD, I/O
55	WD, I/O
56	I/O
57	SDI, I/O
58	I/O
59	VCCA
60	GND
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	VCCI
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	VCCA
86	I/O
87	I/O
88	VCCA

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
74	I/O
75	I/O
76	I/O
77	I/O
78	GND
79	VCCA
80	VCCI
81	I/O
82	I/O
83	I/O
84	I/O
85	WD, I/O
86	WD, I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	QCLKB, I/O
92	I/O
93	WD, I/O
94	WD, I/O
95	I/O
96	I/O
97	I/O
98	VCCI
99	I/O
100	WD, I/O
101	WD, I/O
102	I/O
103	TDO, I/O
104	I/O
105	GND
106	VCCA
107	I/O
108	I/O
109	I/O
110	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
22	I/O
23	I/O
24	I/O
25	I/O
26	VCCA
27	I/O
28	I/O
29	VCCA
30	VCCI
31	GND
32	VCCA
33	LP
34	TCK, I/O
35	I/O
36	GND
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	GND
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
207	I/O
208	I/O
209	QCLKC, I/O
210	I/O
211	WD, I/O
212	WD, I/O
213	I/O
214	I/O
215	WD, I/O
216	WD, I/O
217	I/O
218	PRB, I/O
219	I/O
220	CLKB, I/O
221	I/O
222	GND
223	GND
224	VCCA
225	VCCI
226	I/O
227	CLKA, I/O
228	I/O
229	PRA, I/O
230	I/O
231	I/O
232	WD, I/O
233	WD, I/O
234	I/O
235	I/O
236	I/O
237	I/O
238	I/O
239	I/O
240	QCLKD, I/O
241	I/O
242	WD, I/O
243	GND

Table 61 • PG132

PG132	
Pin Number	A42MX09 Function
F2	I/O
F1	I/O
G1	I/O
G4	VSV
H1	I/O
H2	I/O
H3	I/O
H4	I/O
J1	I/O
K1	I/O
L1	I/O
K2	I/O
M1	I/O
K3	I/O
L2	I/O
N1	I/O
L3	BININ
M2	BINOUT
N2	I/O
M3	I/O
L4	I/O
N3	I/O
M4	I/O
N4	I/O
M5	I/O
K6	I/O
N5	I/O
N6	I/O
L6	I/O
M6	I/O
M7	I/O
N7	I/O
N8	I/O
M8	I/O
L8	I/O
K8	I/O
N9	I/O

Table 62 • CQ172

138	I/O
139	I/O
140	I/O
141	GND
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	PROBA
149	I/O
150	CLKA
151	VCC
152	GND
153	I/O
154	CLKB
155	I/O
156	PROBB
157	I/O
158	I/O
159	I/O
160	I/O
161	GND
162	I/O
163	I/O
164	I/O
165	I/O
166	VCCI
167	I/O
168	I/O
169	I/O
170	I/O
171	DCLK