# Microchip Technology - A40MX04-VQ80 Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 69 |
| Number of Gates | 6000 |
| Voltage - Supply | 3V ~ 3.6V, 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 80-TQFP |
| Supplier Device Package | 80-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-vq80 |

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**Figure 8 •** **Clock Networks of 42MX Devices**

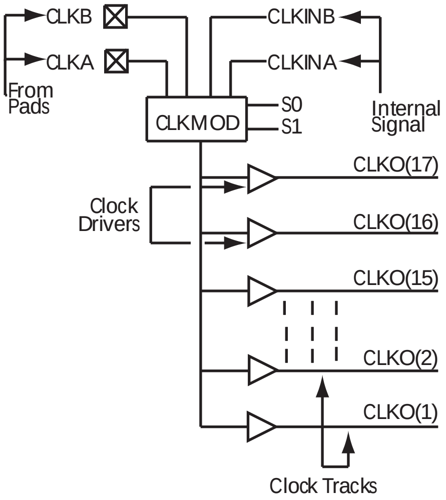
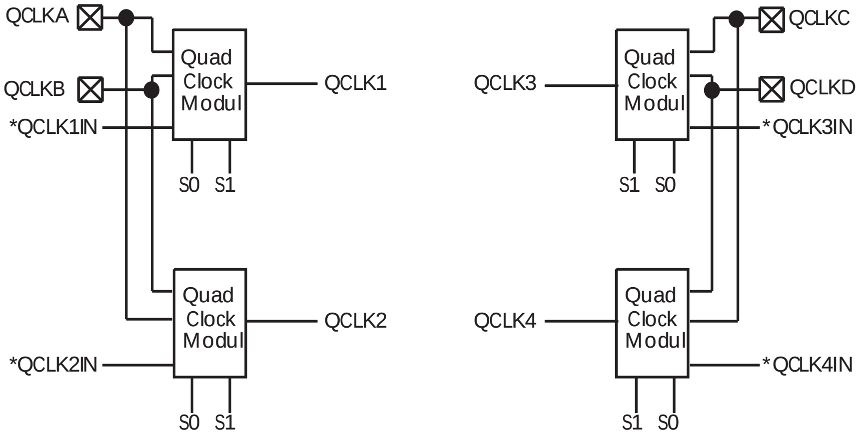


**Figure 9 •** **Quadrant Clock Network of A42MX36 Devices**



**Note:** *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

## 3.2.5 MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 10, page 12 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (See the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 10, page 12). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. See the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 µA.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 11, page 12). When the PCI fuse is not programmed, the output drive is standard.

$f_{q2}$ = Average second routed array clock rate in MHz)

***Table 7 •*** **Fixed Capacitance Values for MX FPGAs (pF)**

| Device Type | r1 routed_Clk1 | r2 routed_Clk2 |
|---|---|---|
| A40MX02 | 41.4 | N/A |
| A40MX04 | 68.6 | N/A |
| A42MX09 | 118 | 118 |
| A42MX16 | 165 | 165 |
| A42MX24 | 185 | 185 |
| A42MX36 | 220 | 220 |

### 3.4.6 Test Circuitry and Silicon Explorer II Probe

MX devices contain probing circuitry that provides built-in access to every node in a design, via the use of Silicon Explorer II. Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer software, allow users to examine any of the internal nets of the device while it is operating in a prototyping or a production system. The user can probe into an MX device without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle and providing a true representation of the device under actual functional situations.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

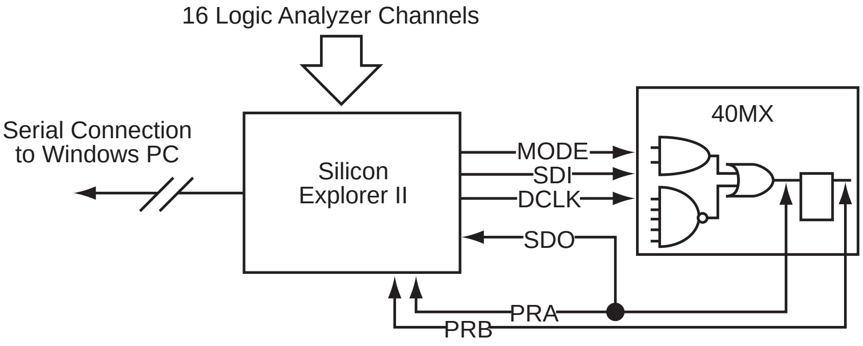
Silicon Explorer II is used to control the MODE, DCLK, SDI and SDO pins in MX devices to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the MODE pin is held HIGH.

Figure 12, page 16 illustrates the interconnection between Silicon Explorer II and 40MX devices, while Figure 13, page 17 illustrates the interconnection between Silicon Explorer II and 42MX devices

To allow for probing capabilities, the security fuses must not be programmed. (See User Security, page 12 for the security fuses of 40MX and 42MX devices). Table 8, page 17 summarizes the possible device configurations for probing.

PRA and PRB pins are dual-purpose pins. When the “Reserve Probe Pin” is checked in the Designer software, PRA and PRB pins are reserved as dedicated outputs for probing. If PRA and PRB pins are required as user I/Os to achieve successful layout and “Reserve Probe Pin” is checked, the layout tool will override the option and place user I/Os on PRA and PRB pins.

***Figure 12 •*** **Silicon Explorer II Setup with 40MX**



## 3.9.1 Mixed 5.0V/3.3V Electrical Specifications

***Table 22 •*** **Mixed 5.0V/3.3V Electrical Specifications**

| | | Commercial | | Commercial –F | | Industrial | | Military | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| VOH[1] | IOH = –10 mA | 2.4 | | 2.4 | | | | | | V |
| | IOH = –4 mA | | | | | 2.4 | | 2.4 | | V |
| VOL[1] | IOL = 10 mA | | 0.5 | | 0.5 | | | | | V |
| | IOL = 6 mA | | | | | | 0.4 | | 0.4 | V |
| VIL | | –0.3 | 0.8 | –0.3 | 0.8 | –0.3 | 0.8 | –0.3 | 0.8 | V |
| VIH[2] | | 2.0 | VCCA + 0.3 | 2.0 | VCCA + 0.3 | 2.0 | VCCA + 0.3 | 2.0 | VCCA + 0.3 | V |
| IL | VIN = 0.5 V | | –10 | | –10 | | –10 | | –10 | µA |
| IH | VIN = 2.7 V | | –10 | | –10 | | –10 | | –10 | µA |
| Input Transition Time, $T_R$ and $T_F$ | | | 500 | | 500 | | 500 | | 500 | ns |
| $C_{IO}$ I/O Capacitance | | | 10 | | 10 | | 10 | | 10 | pF |
| Standby Current, ICC[3] | A42MX09 | | 5 | | 25 | | 25 | | 25 | mA |
| | A42MX16 | | 6 | | 25 | | 25 | | 25 | mA |
| | A42MX24, A42MX36 | | 20 | | 25 | | 25 | | 25 | mA |
| Low Power Mode Standby Current | | | 0.5 | | ICC – 5.0 | | ICC – 5.0 | | ICC – 5.0 | mA |
| IIO I/O source sink current | Can be derived from the *IBIS model* (http://www.microsemi.com/soc/techdocs/models/ibis.html) | | | | | | | | | |

1. Only one output tested at a time. VCCI = min.
2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
3. All outputs unloaded. All inputs = VCCI or GND

## 3.9.2 Output Drive Characteristics for 5.0 V PCI Signaling

MX PCI device I/O drivers were designed specifically for high-performance PCI systems. Figure 16, page 28 shows the typical output drive characteristics of the MX devices. MX output drivers are compliant with the PCI Local Bus Specification.

***Table 23 •*** **DC Specification (5.0 V PCI Signaling)[1]**

| | | | PCI | | MX | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Condition** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| VCCI | Supply Voltage for I/Os | | 4.75 | 5.25 | 4.75 | 5.25[2] | V |
| VIH[3] | Input High Voltage | | 2.0 | VCC + 0.5 | 2.0 | VCCI + 0.3 | V |
| VIL | Input Low Voltage | | –0.5 | 0.8 | –0.3 | 0.8 | V |
| IIH | Input High Leakage Current | VIN = 2.7 V | | 70 | — | 10 | µA |
| IIL | Input Low Leakage Current | VIN=0.5 V | | –70 | — | –10 | µA |
| VOH | Output High Voltage | IOUT = –2 mA | 2.4 | | | | V |
| | | IOUT = –6 mA | | | 3.84 | | |
| VOL | Output Low Voltage | IOUT = 3 mA, 6 mA | | 0.55 | — | 0.33 | V |

**Table 34 •** **A40MX02 Timing Characteristics (Nominal 5.0 V Operation) *(continued)***
**(Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C)**

| | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **TTL Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 3.3 | | 3.8 | | 4.3 | | 5.1 | | 7.2 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 4.0 | | 4.6 | | 5.2 | | 6.1 | | 8.6 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 3.7 | | 4.3 | | 4.9 | | 5.8 | | 8.0 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 4.7 | | 5.4 | | 6.1 | | 7.2 | | 10.1 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 7.9 | | 9.1 | | 10.4 | | 12.2 | | 17.1 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.9 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | ns |
| $d_{TLH}$ | Delta LOW to HIGH | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |
| $d_{THL}$ | Delta HIGH to LOW | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.06 | ns/pF |
| **CMOS Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 3.9 | | 4.5 | | 5.1 | | 6.05 | | 8.5 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 4.9 | | 5.6 | | 6.4 | | 7.5 | | 10.5 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 7.9 | | 9.1 | | 10.4 | | 12.2 | | 17.0 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.9 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | ns |
| $d_{TLH}$ | Delta LOW to HIGH | | 0.03 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| $d_{THL}$ | Delta HIGH to LOW | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35pF loading

**Table 35 •** **A40MX02 Timing Characteristics (Nominal 3.3 V Operation)**
**(Worst-Case Commercial Conditions, VCC = 3.0 V, $T_J$ = 70°C)**

| | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Logic Module Propagation Delays** | | | | | | | | | | | | |
| $t_{PD1}$ | Single Module | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{PD2}$ | Dual-Module Macros | | 3.7 | | 4.3 | | 4.9 | | 5.7 | | 8.0 | ns |
| $t_{CO}$ | Sequential Clock-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{GO}$ | Latch G-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| **Logic Module Predicted Routing Delays[1]** | | | | | | | | | | | | |

***Table 39 •*** **A42MX09 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| **Input Module Propagation Delays** | | | | | | | | | | | | | |
| $t_{INYH}$ | Pad-to-Y HIGH | | | 1.5 | | 1.6 | | 1.8 | | 2.17 | | 3.0 | ns |
| $t_{INYL}$ | Pad-to-Y LOW | | | 1.2 | | 1.3 | | 1.4 | | 1.7 | | 2.4 | ns |
| $t_{INGH}$ | G to Y HIGH | | | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{INGL}$ | G to Y LOW | | | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| **Input Module Predicted Routing Delays**[2] | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 3.2 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 3.5 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 3.9 | | 4.3 | | 4.9 | | 5.7 | | 8.0 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 5.2 | | 5.8 | | 6.6 | | 7.7 | | 10.8 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 32 | | 4.1 | | 4.5 | | 5.1 | | 6.0 | | 8.4 | ns |
| | | FO = 256 | | 4.5 | | 5.0 | | 5.6 | | 6.7 | | 9.3 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 32 | | 5.0 | | 5.5 | | 6.2 | | 7.3 | | 10.2 | ns |
| | | FO = 256 | | 5.4 | | 6.0 | | 6.8 | | 8.0 | | 11.2 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 32 | 1.7 | | 1.9 | | 2.1 | | 2.5 | | 3.5 | | ns |
| | | FO = 256 | 1.9 | | 2.1 | | 2.3 | | 2.7 | | 3.8 | | ns |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 1.7 | | 1.9 | | 2.1 | | 2.5 | | 3.5 | | ns |
| | | FO = 256 | 1.9 | | 2.1 | | 2.3 | | 2.7 | | 3.8 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.9 | ns |
| | | FO = 256 | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.9 | ns |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 256 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | | ns |
| | | FO = 256 | 3.7 | | 4.1 | | 4.6 | | 5.5 | | 7.6 | | ns |
| $t_P$ | Minimum Period | FO = 32 | 5.6 | | 6.2 | | 6.7 | | 7.8 | | 12.9 | | ns |
| | | FO = 256 | 6.1 | | 6.8 | | 7.4 | | 8.5 | | 14.2 | | ns |
| $f_{MAX}$ | Maximum Frequency | FO = 32 | | 177 | | 161 | | 148 | | 129 | | 77 | MHz |
| | | FO = 256 | | 161 | | 146 | | 135 | | 117 | | 70 | MHz |

**Table 40 •** **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 3.2 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | | ns |
| | | FO = 384 | 3.7 | | 4.1 | | 4.6 | | 5.4 | | 7.6 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| | | FO = 384 | | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 384 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 2.8 | | 3.1 | | 5.5 | | 4.1 | | 5.7 | | ns |
| | | FO = 384 | 3.2 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | | ns |
| $t_P$ | Minimum Period | FO = 32 | 4.2 | | 4.67 | | 5.1 | | 5.8 | | 9.7 | | ns |
| | | FO = 384 | 4.6 | | 5.1 | | 5.6 | | 6.4 | | 10.7 | | ns |
| $f_{MAX}$ | Maximum Frequency | FO = 32 | | 237 | | 215 | | 198 | | 172 | | 103 | MHz |
| | | FO = 384 | | 215 | | 195 | | 179 | | 156 | | 94 | MHz |

***Table 41 •*** **A42MX16 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 5.3 | | 5.9 | | 6.7 | | 7.8 | | 11.0 | | ns |
| | | FO = 384 | 6.2 | | 6.9 | | 7.9 | | 9.2 | | 12.9 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | ns |
| | | FO = 384 | | 2.2 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 384 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 3.9 | | 4.3 | | 4.9 | | 5.7 | | 8.0 | | ns |
| | | FO = 384 | 4.5 | | 4.9 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_P$ | Minimum Period | FO = 32 | 7.0 | | 7.8 | | 8.4 | | 9.7 | | 16.2 | | ns |
| | | FO = 384 | 7.7 | | 8.6 | | 9.3 | | 10.7 | | 17.8 | | ns |
| $f_{MAX}$ | Maximum Frequency | FO = 32 | | 142 | | 129 | | 119 | | 103 | | 62 | MHz |
| | | FO = 384 | | 129 | | 117 | | 108 | | 94 | | 56 | MHz |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 3.5 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 4.1 | | 4.6 | | 5.2 | | 6.1 | | 8.6 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.8 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 4.2 | | 4.6 | | 5.3 | | 6.2 | | 8.7 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.6 | | 8.4 | | 9.5 | | 11.2 | | 15.7 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 7.0 | | 7.8 | | 8.8 | | 10.4 | | 14.5 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | | 8.0 | | 8.9 | | 10.1 | | 11.9 | | 16.7 | ns |
| $t_{ACO}$ | Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | | 11.3 | | 12.5 | | 14.2 | | 16.7 | | 23.3 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| $d_{THL}$ | Capacitive Loading, HIGH to LOW | | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.10 | ns/pF |
| **CMOS Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 4.5 | | 5.0 | | 5.6 | | 6.6 | | 9.3 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 3.4 | | 3.8 | | 4.3 | | 5.1 | | 7.1 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.8 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 4.2 | | 4.6 | | 5.3 | | 6.2 | | 8.7 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.6 | | 8.4 | | 9.5 | | 11.2 | | 15.7 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 7.0 | | 7.8 | | 8.8 | | 10.4 | | 14.5 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 7.1 | | 7.9 | | 8.9 | | 10.5 | | 14.7 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 7.1 | | 7.9 | | 8.9 | | 10.5 | | 14.7 | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | | 8.0 | | 8.9 | | 10.1 | | 11.9 | | 16.7 | ns |

***Table 43 •*** **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Input Module Predicted Routing Delays[2]** | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.6 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 2.9 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 3.2 | | 3.6 | | 4.0 | | 4.8 | | 6.6 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 3.5 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 4.8 | | 5.3 | | 6.1 | | 7.1 | | 10.0 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 32 | | 4.4 | | 4.8 | | 5.5 | | 6.5 | | 9.1 | ns |
| | | FO = 486 | | 4.8 | | 5.3 | | 6.0 | | 7.1 | | 10.0 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 32 | | 5.1 | | 5.7 | | 6.4 | | 7.6 | | 10.6 | ns |
| | | FO = 486 | | 6.0 | | 6.6 | | 7.5 | | 8.8 | | 12.4 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 32 | 3.0 | | 3.3 | | 3.8 | | 4.5 | | 6.3 | | ns |
| | | FO = 486 | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | | ns |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 3.0 | | 3.4 | | 3.8 | | 4.5 | | 6.3 | | ns |
| | | FO = 486 | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 0.8 | | 0.8 | | 1.0 | | 1.1 | | 1.6 | ns |
| | | FO = 486 | | 0.8 | | 0.8 | | 1.0 | | 1.1 | | 1.6 | ns |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 486 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.1 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 4.0 | | 4.4 | | 5.0 | | 5.9 | | 8.3 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.4 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 3.9 | | 4.4 | | 5.0 | | 5.8 | | 8.2 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.2 | | 8.0 | | 9.1 | | 10.7 | | 14.9 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 6.7 | | 7.5 | | 8.5 | | 9.9 | | 13.9 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| $t_{LSU}$ | I/O Latch Output Set-Up | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |

***Table 45 •*** **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| | | | **–3 Speed** | | **–2 Speed** | | **–1 Speed** | | **Std Speed** | | **–F Speed** | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Input Module Predicted Routing Delays**[2] | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 3.2 | | 3.5 | | 4.1 | | 4.8 | | 6.7 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 7.7 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 4.2 | | 4.6 | | 5.3 | | 6.2 | | 8.7 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 6.1 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 32 | | 4.6 | | 5.1 | | 5.7 | | 6.7 | | 9.3 | ns |
| | | FO = 635 | | 5.0 | | 5.6 | | 6.3 | | 7.4 | | 10.3 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 32 | | 5.3 | | 5.9 | | 6.7 | | 7.8 | | 11.0 | ns |
| | | FO = 635 | | 6.8 | | 7.6 | | 8.6 | | 10.1 | | 14.1 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 32 | 2.5 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | | ns |
| | | FO = 635 | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | | ns |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 2.5 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | | ns |
| | | FO = 635 | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.2 | ns |
| | | FO = 635 | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.2 | ns |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 635 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 4.0 | | 4.4 | | 5.0 | | 5.9 | | 8.2 | | ns |
| | | FO = 635 | 4.6 | | 5.2 | | 5.9 | | 6.9 | | 9.6 | | ns |
| $t_P$ | Minimum Period ($1/f_{MAX}$) | FO = 32 | 9.2 | | 10.2 | | 11.1 | | 12.7 | | 21.2 | | ns |
| | | FO = 635 | 9.9 | | 11.0 | | 12.0 | | 13.8 | | 23.0 | | ns |
| $f_{MAX}$ | Maximum Datapath Frequency | FO = 32 | | 108 | | 98 | | 90 | | 79 | | 47 | MHz |
| | | FO = 635 | | 100 | | 91 | | 83 | | 73 | | 44 | MHz |
| **TTL Output Module Timing**[5] | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.4 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 4.2 | | 4.6 | | 5.2 | | 6.2 | | 8.6 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.7 | | 4.2 | | 4.7 | | 5.5 | | 7.7 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 4.1 | | 4.6 | | 5.2 | | 6.1 | | 8.5 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.34 | | 8.2 | | 9.3 | | 10.9 | | 15.3 | ns |
| **TTL Output Module Timing**[5] | | | | | | | | | | | | | |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 6.9 | | 7.6 | | 8.7 | | 10.2 | | 14.3 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 4.9 | | 5.5 | | 6.2 | | 7.3 | | 10.2 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 4.9 | | 5.5 | | 6.2 | | 7.3 | | 10.2 | ns |
| $t_{LSU}$ | I/O Latch Output Set-Up | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{LH}$ | I/O Latch Output Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | | 7.9 | | 8.8 | | 10.0 | | 11.8 | | 16.5 | ns |

# 4 Package Pin Assignments

The following figures and tables give the details of the package pin assignments.

*Figure 38 •* **PL44**

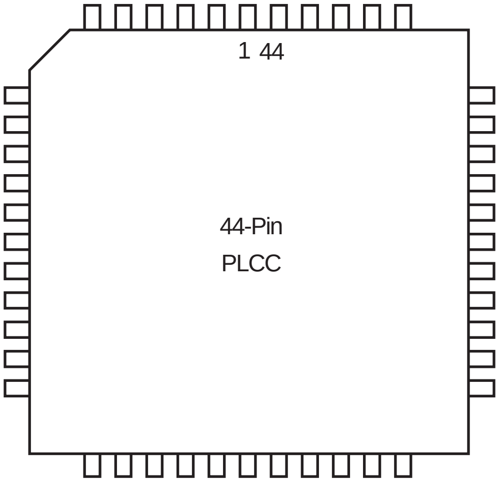


*Table 47 •* **PL44**

| **PL44** | | |
|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** |
| 1 | I/O | I/O |
| 2 | I/O | I/O |
| 3 | VCC | VCC |
| 4 | I/O | I/O |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | I/O | I/O |
| 8 | I/O | I/O |
| 9 | I/O | I/O |
| 10 | GND | GND |
| 11 | I/O | I/O |
| 12 | I/O | I/O |
| 13 | I/O | I/O |
| 14 | VCC | VCC |
| 15 | I/O | I/O |
| 16 | VCC | VCC |
| 17 | I/O | I/O |
| 18 | I/O | I/O |
| 19 | I/O | I/O |
| 20 | I/O | I/O |

**Table 52 •** **PQ160**

| **PQ160** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 58 | VCCI | VCCI | VCCI |
| 59 | GND | GND | GND |
| 60 | VCCA | VCCA | VCCA |
| 61 | LP | LP | LP |
| 62 | I/O | I/O | TCK, I/O |
| 63 | I/O | I/O | I/O |
| 64 | GND | GND | GND |
| 65 | I/O | I/O | I/O |
| 66 | I/O | I/O | I/O |
| 67 | I/O | I/O | I/O |
| 68 | I/O | I/O | I/O |
| 69 | GND | GND | GND |
| 70 | NC | I/O | I/O |
| 71 | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O |
| 75 | NC | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | NC | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | NC | I/O | I/O |
| 80 | GND | GND | GND |
| 81 | I/O | I/O | I/O |
| 82 | SDO, I/O | SDO, I/O | SDO, TDO, I/O |
| 83 | I/O | I/O | WD, I/O |
| 84 | I/O | I/O | WD, I/O |
| 85 | I/O | I/O | I/O |
| 86 | NC | VCCI | VCCI |
| 87 | I/O | I/O | I/O |
| 88 | I/O | I/O | WD, I/O |
| 89 | GND | GND | GND |
| 90 | NC | I/O | I/O |
| 91 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |

***Table 52 •*** **PQ160**

| **PQ160** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 132 | I/O | I/O | I/O |
| 133 | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O |
| 135 | NC | VCCA | VCCA |
| 136 | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O |
| 138 | NC | VCCA | VCCA |
| 139 | VCCI | VCCI | VCCI |
| 140 | GND | GND | GND |
| 141 | NC | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | I/O | I/O | I/O |
| 144 | I/O | I/O | I/O |
| 145 | GND | GND | GND |
| 146 | NC | I/O | I/O |
| 147 | I/O | I/O | I/O |
| 148 | I/O | I/O | I/O |
| 149 | I/O | I/O | I/O |
| 150 | NC | VCCA | VCCA |
| 151 | NC | I/O | I/O |
| 152 | NC | I/O | I/O |
| 153 | NC | I/O | I/O |
| 154 | NC | I/O | I/O |
| 155 | GND | GND | GND |
| 156 | I/O | I/O | I/O |
| 157 | I/O | I/O | I/O |
| 158 | I/O | I/O | I/O |
| 159 | MODE | MODE | MODE |
| 160 | GND | GND | GND |

*Table 54 •* **PQ240**

| **PQ240** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 15 | QCLKC, I/O |
| 16 | I/O |
| 17 | WD, I/O |
| 18 | WD, I/O |
| 19 | I/O |
| 20 | I/O |
| 21 | WD, I/O |
| 22 | WD, I/O |
| 23 | I/O |
| 24 | PRB, I/O |
| 25 | I/O |
| 26 | CLKB, I/O |
| 27 | I/O |
| 28 | GND |
| 29 | VCCA |
| 30 | VCCI |
| 31 | I/O |
| 32 | CLKA, I/O |
| 33 | I/O |
| 34 | PRA, I/O |
| 35 | I/O |
| 36 | I/O |
| 37 | WD, I/O |
| 38 | WD, I/O |
| 39 | I/O |
| 40 | I/O |
| 41 | I/O |
| 42 | I/O |
| 43 | I/O |
| 44 | I/O |
| 45 | QCLKD, I/O |
| 46 | I/O |
| 47 | WD, I/O |
| 48 | WD, I/O |
| 49 | I/O |
| 50 | I/O |
| 51 | I/O |

*Table 54 •* **PQ240**

| **PQ240** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 200 | I/O |
| 201 | I/O |
| 202 | I/O |
| 203 | I/O |
| 204 | I/O |
| 205 | I/O |
| 206 | VCCA |
| 207 | I/O |
| 208 | I/O |
| 209 | VCCA |
| 210 | VCCI |
| 211 | I/O |
| 212 | I/O |
| 213 | I/O |
| 214 | I/O |
| 215 | I/O |
| 216 | I/O |
| 217 | I/O |
| 218 | I/O |
| 219 | VCCA |
| 220 | I/O |
| 221 | I/O |
| 222 | I/O |
| 223 | I/O |
| 224 | I/O |
| 225 | I/O |
| 226 | I/O |
| 227 | VCCI |
| 228 | I/O |
| 229 | I/O |
| 230 | I/O |
| 231 | I/O |
| 232 | I/O |
| 233 | I/O |
| 234 | I/O |
| 235 | I/O |
| 236 | I/O |

**Table 57 •** **TQ176**

| **TQ176** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 121 | NC | NC | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | NC | I/O | I/O |
| 125 | NC | I/O | I/O |
| 126 | NC | NC | I/O |
| 127 | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O |
| 129 | I/O | I/O | I/O |
| 130 | I/O | I/O | I/O |
| 131 | I/O | I/O | I/O |
| 132 | I/O | I/O | I/O |
| 133 | GND | GND | GND |
| 134 | I/O | I/O | I/O |
| 135 | SDI, I/O | SDI, I/O | SDI, I/O |
| 136 | NC | I/O | I/O |
| 137 | I/O | I/O | WD, I/O |
| 138 | I/O | I/O | WD, I/O |
| 139 | I/O | I/O | I/O |
| 140 | NC | VCCI | VCCI |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | NC | I/O | I/O |
| 144 | NC | I/O | WD, I/O |
| 145 | NC | NC | WD, I/O |
| 146 | I/O | I/O | I/O |
| 147 | NC | I/O | I/O |
| 148 | I/O | I/O | I/O |
| 149 | I/O | I/O | I/O |
| 150 | I/O | I/O | WD, I/O |
| 151 | NC | I/O | WD, I/O |
| 152 | PRA, I/O | PRA, I/O | PRA, I/O |
| 153 | I/O | I/O | I/O |
| 154 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 155 | VCCA | VCCA | VCCA |
| 156 | GND | GND | GND |
| 157 | I/O | I/O | I/O |

*Table 58 •* **CQ208**

| **CQ208** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 74 | I/O |
| 75 | I/O |
| 76 | I/O |
| 77 | I/O |
| 78 | GND |
| 79 | VCCA |
| 80 | VCCI |
| 81 | I/O |
| 82 | I/O |
| 83 | I/O |
| 84 | I/O |
| 85 | WD, I/O |
| 86 | WD, I/O |
| 87 | I/O |
| 88 | I/O |
| 89 | I/O |
| 90 | I/O |
| 91 | QCLKB, I/O |
| 92 | I/O |
| 93 | WD, I/O |
| 94 | WD, I/O |
| 95 | I/O |
| 96 | I/O |
| 97 | I/O |
| 98 | VCCI |
| 99 | I/O |
| 100 | WD, I/O |
| 101 | WD, I/O |
| 102 | I/O |
| 103 | TDO, I/O |
| 104 | I/O |
| 105 | GND |
| 106 | VCCA |
| 107 | I/O |
| 108 | I/O |
| 109 | I/O |
| 110 | I/O |

*Table 59 •* **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 96 | VCCA |
| 97 | GND |
| 98 | GND |
| 99 | I/O |
| 100 | I/O |
| 101 | I/O |
| 102 | I/O |
| 103 | I/O |
| 104 | I/O |
| 105 | WD, I/O |
| 106 | WD, I/O |
| 107 | I/O |
| 108 | I/O |
| 109 | WD, I/O |
| 110 | WD, I/O |
| 111 | I/O |
| 112 | QCLKA, I/O |
| 113 | I/O |
| 114 | GND |
| 115 | I/O |
| 116 | I/O |
| 117 | I/O |
| 118 | I/O |
| 119 | VCCI |
| 120 | I/O |
| 121 | WD, I/O |
| 122 | WD, I/O |
| 123 | I/O |
| 124 | I/O |
| 125 | I/O |
| 126 | I/O |
| 127 | GND |
| 128 | NC |
| 129 | NC |
| 130 | NC |
| 131 | GND |
| 132 | I/O |

*Table 60 •* **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| D20 | I/O |
| E1 | I/O |
| E2 | I/O |
| E3 | I/O |
| E4 | VCCA |
| E17 | VCCI |
| E18 | I/O |
| E19 | I/O |
| E20 | I/O |
| F1 | I/O |
| F2 | I/O |
| F3 | I/O |
| F4 | VCCI |
| F17 | I/O |
| F18 | I/O |
| F19 | I/O |
| F20 | I/O |
| G1 | I/O |
| G2 | I/O |
| G3 | I/O |
| G4 | VCCI |
| G17 | VCCI |
| G18 | I/O |
| G19 | I/O |
| G20 | I/O |
| H1 | I/O |
| H2 | I/O |
| H3 | I/O |
| H4 | VCCA |
| H17 | I/O |
| H18 | I/O |
| H19 | I/O |
| H20 | I/O |
| J1 | I/O |
| J2 | I/O |
| J3 | I/O |
| J4 | VCCI |

**Table 60 •** **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| J9 | GND |
| J10 | GND |
| J11 | GND |
| J12 | GND |
| J17 | VCCA |
| J18 | I/O |
| J19 | I/O |
| J20 | I/O |
| K1 | I/O |
| K2 | I/O |
| K3 | I/O |
| K4 | VCCI |
| K9 | GND |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K17 | I/O |
| K18 | VCCA |
| K19 | VCCA |
| K20 | LP |
| L1 | I/O |
| L2 | I/O |
| L3 | VCCA |
| L4 | VCCA |
| L9 | GND |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L17 | VCCI |
| L18 | I/O |
| L19 | I/O |
| L20 | TCK, I/O |
| M1 | I/O |
| M2 | I/O |
| M3 | I/O |
| M4 | VCCI |
| M9 | GND |