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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                                               |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                                                      |
| Number of LABs/CLBs            | -                                                                                                                                                             |
| Number of Logic Elements/Cells | -                                                                                                                                                             |
| Total RAM Bits                 | -                                                                                                                                                             |
| Number of I/O                  | 69                                                                                                                                                            |
| Number of Gates                | 6000                                                                                                                                                          |
| Voltage - Supply               | 3V ~ 3.6V, 4.5V ~ 5.5V                                                                                                                                        |
| Mounting Type                  | Surface Mount                                                                                                                                                 |
| Operating Temperature          | -40°C ~ 85°C (TA)                                                                                                                                             |
| Package / Case                 | 80-TQFP                                                                                                                                                       |
| Supplier Device Package        | 80-VQFP (14x14)                                                                                                                                               |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-vq80i">https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-vq80i</a> |

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**Table 33 • Timing Parameters for 33 MHz PCI**

| Symbol        | Parameter                               | PCI                 |      | A42MX24 |      | A42MX36 |      | Units |
|---------------|-----------------------------------------|---------------------|------|---------|------|---------|------|-------|
|               |                                         | Min.                | Max. | Min.    | Max. | Min.    | Max. |       |
| $t_{SU(PTP)}$ | Input Set-Up Time to CLK—Point-to-Point | 10, 12 <sup>2</sup> | —    | 1.5     | —    | 1.5     | —    | ns    |
| $t_H$         | Input Hold to CLK                       | 0                   | —    | 0       | —    | 0       | —    | ns    |

1. TOFF is system dependent. MX PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.
2. REQ# and GNT# are point-to-point signals and have different output valid delay and input setup times than do bussed signals. GNT# has a setup of 10; REW# has a setup of 12.

### 3.11.6.1 Timing Characteristics

The following tables list the timing characteristics.

**Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation)**  
**(Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C)**

| Parameter / Description                            |                                                 | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|----------------------------------------------------|-------------------------------------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                                    |                                                 | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| Logic Module Propagation Delays                    |                                                 |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>PD1</sub>                                   | Single Module                                   |          | 1.2  |          | 1.4  |          | 1.6  |           | 1.9  |          | 2.7  | ns    |
| t <sub>PD2</sub>                                   | Dual-Module Macros                              |          | 2.7  |          | 3.1  |          | 3.5  |           | 4.1  |          | 5.7  | ns    |
| t <sub>CO</sub>                                    | Sequential Clock-to-Q                           |          | 1.2  |          | 1.4  |          | 1.6  |           | 1.9  |          | 2.7  | ns    |
| t <sub>GO</sub>                                    | Latch G-to-Q                                    |          | 1.2  |          | 1.4  |          | 1.6  |           | 1.9  |          | 2.7  | ns    |
| t <sub>RS</sub>                                    | Flip-Flop (Latch) Reset-to-Q                    |          | 1.2  |          | 1.4  |          | 1.6  |           | 1.9  |          | 2.7  | ns    |
| Logic Module Predicted Routing Delays <sup>1</sup> |                                                 |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>RD1</sub>                                   | FO = 1 Routing Delay                            |          | 1.3  |          | 1.5  |          | 1.7  |           | 2.0  |          | 2.8  | ns    |
| t <sub>RD2</sub>                                   | FO = 2 Routing Delay                            |          | 1.8  |          | 2.1  |          | 2.4  |           | 2.8  |          | 3.9  | ns    |
| t <sub>RD3</sub>                                   | FO = 3 Routing Delay                            |          | 2.3  |          | 2.7  |          | 3.0  |           | 3.6  |          | 5.0  | ns    |
| t <sub>RD4</sub>                                   | FO = 4 Routing Delay                            |          | 2.9  |          | 3.3  |          | 3.7  |           | 4.4  |          | 6.1  | ns    |
| t <sub>RD8</sub>                                   | FO = 8 Routing Delay                            |          | 4.9  |          | 5.7  |          | 6.5  |           | 7.6  |          | 10.6 | ns    |
| Logic Module Sequential Timing <sup>2</sup>        |                                                 |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>SUD</sub>                                   | Flip-Flop (Latch)<br>Data Input Set-Up          | 3.1      |      | 3.5      |      | 4.0      |      | 4.7       |      | 6.6      |      | ns    |
| t <sub>HD</sub> <sup>3</sup>                       | Flip-Flop (Latch)<br>Data Input Hold            | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>SUENA</sub>                                 | Flip-Flop (Latch)<br>Enable Set-Up              | 3.1      |      | 3.5      |      | 4.0      |      | 4.7       |      | 6.6      |      | ns    |
| t <sub>HENA</sub>                                  | Flip-Flop (Latch) Enable Hold                   | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>WCLKA</sub>                                 | Flip-Flop (Latch)<br>Clock Active Pulse Width   | 3.3      |      | 3.8      |      | 4.3      |      | 5.0       |      | 7.0      |      | ns    |
| t <sub>WASYN</sub>                                 | Flip-Flop (Latch)<br>Asynchronous Pulse Width   | 3.3      |      | 3.8      |      | 4.3      |      | 5.0       |      | 7.0      |      | ns    |
| t <sub>A</sub>                                     | Flip-Flop Clock Input Period                    | 4.8      |      | 5.6      |      | 6.3      |      | 7.5       |      | 10.4     |      | ns    |
| f <sub>MAX</sub>                                   | Flip-Flop (Latch) Clock<br>Frequency (FO = 128) |          | 181  |          | 168  |          | 154  |           | 134  |          | 80   | MHz   |



**Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation) (continued)**  
**(Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C)**

| Parameter / Description                            |                          |                     | –3 Speed   |            | –2 Speed   |             | –1 Speed   |            | Std Speed  |              | –F Speed     |      | Units |
|----------------------------------------------------|--------------------------|---------------------|------------|------------|------------|-------------|------------|------------|------------|--------------|--------------|------|-------|
|                                                    |                          |                     | Min.       | Max.       | Min.       | Max.        | Min.       | Max.       | Min.       | Max.         | Min.         | Max. |       |
| Input Module Propagation Delays                    |                          |                     |            |            |            |             |            |            |            |              |              |      |       |
| t <sub>INYH</sub>                                  | Pad-to-Y HIGH            |                     | 0.7        |            | 0.8        |             | 0.9        |            | 1.1        |              | 1.5          |      | ns    |
| t <sub>INYL</sub>                                  | Pad-to-Y LOW             |                     | 0.6        |            | 0.7        |             | 0.8        |            | 1.0        |              | 1.3          |      | ns    |
| Input Module Predicted Routing Delays <sup>1</sup> |                          |                     |            |            |            |             |            |            |            |              |              |      |       |
| t <sub>IRD1</sub>                                  | FO = 1 Routing Delay     |                     | 2.1        |            | 2.4        |             | 2.2        |            | 3.2        |              | 4.5          |      | ns    |
| t <sub>IRD2</sub>                                  | FO = 2 Routing Delay     |                     | 2.6        |            | 3.0        |             | 3.4        |            | 4.0        |              | 5.6          |      | ns    |
| t <sub>IRD3</sub>                                  | FO = 3 Routing Delay     |                     | 3.1        |            | 3.6        |             | 4.1        |            | 4.8        |              | 6.7          |      | ns    |
| t <sub>IRD4</sub>                                  | FO = 4 Routing Delay     |                     | 3.6        |            | 4.2        |             | 4.8        |            | 5.6        |              | 7.8          |      | ns    |
| t <sub>IRD8</sub>                                  | FO = 8 Routing Delay     |                     | 5.7        |            | 6.6        |             | 7.5        |            | 8.8        |              | 12.4         |      | ns    |
| Global Clock Network                               |                          |                     |            |            |            |             |            |            |            |              |              |      |       |
| t <sub>CKH</sub>                                   | Input Low to HIGH        | FO = 16<br>FO = 128 | 4.6<br>4.6 |            | 5.3<br>5.3 |             | 6.0<br>6.0 |            | 7.0<br>7.0 |              | 9.8<br>9.8   |      | ns    |
| t <sub>CKL</sub>                                   | Input High to LOW        | FO = 16<br>FO = 128 | 4.8<br>4.8 |            | 5.6<br>5.6 |             | 6.3<br>6.3 |            | 7.4<br>7.4 |              | 10.4<br>10.4 |      | ns    |
| t <sub>PWH</sub>                                   | Minimum Pulse Width HIGH | FO = 16<br>FO = 128 | 2.2<br>2.4 | 2.6<br>2.7 |            | 2.9<br>3.1  |            | 3.4<br>3.6 |            | 4.8<br>5.1   |              | ns   |       |
| t <sub>PWL</sub>                                   | Minimum Pulse Width LOW  | FO = 16<br>FO = 128 | 2.2<br>2.4 | 2.6<br>2.7 |            | 2.9<br>3.01 |            | 3.4<br>3.6 |            | 4.8<br>5.1   |              | ns   |       |
| t <sub>CKSW</sub>                                  | Maximum Skew             | FO = 16<br>FO = 128 | 0.4<br>0.5 |            | 0.5<br>0.6 |             | 0.5<br>0.7 |            | 0.6<br>0.8 |              | 0.8<br>1.2   |      | ns    |
| t <sub>P</sub>                                     | Minimum Period           | FO = 16<br>FO = 128 | 4.7<br>4.8 | 5.4<br>5.6 |            | 6.1<br>6.3  |            | 7.2<br>7.5 |            | 10.0<br>10.4 |              | ns   |       |
| f <sub>MAX</sub>                                   | Maximum Frequency        | FO = 16<br>FO = 128 | 188<br>181 |            | 175<br>168 |             | 160<br>154 |            | 139<br>134 |              | 83<br>80     |      | MHz   |

**Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C)**

| Parameter / Description                |                      | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|----------------------------------------|----------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                        |                      | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| CMOS Output Module Timing <sup>1</sup> |                      |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>DLH</sub>                       | Data-to-Pad HIGH     |          | 3.9  |          | 4.5  |          | 5.1  |           | 6.05 |          | 8.5  | ns    |
| t <sub>DHL</sub>                       | Data-to-Pad LOW      |          | 3.4  |          | 3.9  |          | 4.4  |           | 5.2  |          | 7.3  | ns    |
| t <sub>ENZH</sub>                      | Enable Pad Z to HIGH |          | 3.4  |          | 3.9  |          | 4.4  |           | 5.2  |          | 7.3  | ns    |
| t <sub>ENZL</sub>                      | Enable Pad Z to LOW  |          | 4.9  |          | 5.6  |          | 6.4  |           | 7.5  |          | 10.5 | ns    |
| t <sub>ENHZ</sub>                      | Enable Pad HIGH to Z |          | 7.9  |          | 9.1  |          | 10.4 |           | 12.2 |          | 17.0 | ns    |
| t <sub>ENLZ</sub>                      | Enable Pad LOW to Z  |          | 5.9  |          | 6.8  |          | 7.7  |           | 9.0  |          | 12.6 | ns    |
| d <sub>TLH</sub>                       | Delta LOW to HIGH    |          | 0.03 |          | 0.04 |          | 0.04 |           | 0.05 |          | 0.07 | ns/pF |
| d <sub>THL</sub>                       | Delta HIGH to LOW    |          | 0.02 |          | 0.02 |          | 0.03 |           | 0.03 |          | 0.04 | ns/pF |

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer utility from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading

**Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCC = 3.0 V, T<sub>J</sub> = 70°C)**

| Parameter / Description                            |                                     | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|----------------------------------------------------|-------------------------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                                    |                                     | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| Logic Module Propagation Delays                    |                                     |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>PD1</sub>                                   | Single Module                       |          | 1.7  |          | 2.0  |          | 2.3  |           | 2.7  |          | 3.7  | ns    |
| t <sub>PD2</sub>                                   | Dual-Module Macros                  |          | 3.7  |          | 4.3  |          | 4.9  |           | 5.7  |          | 8.0  | ns    |
| t <sub>CO</sub>                                    | Sequential Clock-to-Q               |          | 1.7  |          | 2.0  |          | 2.3  |           | 2.7  |          | 3.7  | ns    |
| t <sub>GO</sub>                                    | Latch G-to-Q                        |          | 1.7  |          | 2.0  |          | 2.3  |           | 2.7  |          | 3.7  | ns    |
| t <sub>RS</sub>                                    | Flip-Flop (Latch) Reset-to-Q        |          | 1.7  |          | 2.0  |          | 2.3  |           | 2.7  |          | 3.7  | ns    |
| Logic Module Predicted Routing Delays <sup>1</sup> |                                     |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>RD1</sub>                                   | FO = 1 Routing Delay                |          | 1.9  |          | 2.2  |          | 2.5  |           | 3.0  |          | 4.2  | ns    |
| t <sub>RD2</sub>                                   | FO = 2 Routing Delay                |          | 2.7  |          | 3.1  |          | 3.5  |           | 4.1  |          | 5.7  | ns    |
| t <sub>RD3</sub>                                   | FO = 3 Routing Delay                |          | 3.4  |          | 3.9  |          | 4.4  |           | 5.2  |          | 7.3  | ns    |
| t <sub>RD4</sub>                                   | FO = 4 Routing Delay                |          | 4.1  |          | 4.8  |          | 5.4  |           | 6.3  |          | 8.9  | ns    |
| t <sub>RD8</sub>                                   | FO = 8 Routing Delay                |          | 7.1  |          | 8.1  |          | 9.2  |           | 10.9 |          | 15.2 | ns    |
| Logic Module Sequential Timing <sup>2</sup>        |                                     |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>SUD</sub>                                   | Flip-Flop (Latch) Data Input Set-Up |          | 4.3  |          | 5.0  |          | 5.6  |           | 6.6  |          | 9.2  | ns    |
| t <sub>HD</sub> <sup>3</sup>                       | Flip-Flop (Latch) Data Input Hold   | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>SUENA</sub>                                 | Flip-Flop (Latch) Enable Set-Up     |          | 4.3  |          | 5.0  |          | 5.6  |           | 6.6  |          | 9.2  | ns    |
| t <sub>HENA</sub>                                  | Flip-Flop (Latch) Enable Hold       | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |























**Table 60 • BG272**

| <b>BG272</b>      |                         |
|-------------------|-------------------------|
| <b>Pin Number</b> | <b>A42MX36 Function</b> |
| V16               | I/O                     |
| V17               | I/O                     |
| V18               | SDO, TDO, I/O           |
| V19               | I/O                     |
| V20               | I/O                     |
| W1                | GND                     |
| W2                | GND                     |
| W3                | I/O                     |
| W4                | TMS, I/O                |
| W5                | I/O                     |
| W6                | I/O                     |
| W7                | I/O                     |
| W8                | WD, I/O                 |
| W9                | WD, I/O                 |
| W10               | I/O                     |
| W11               | I/O                     |
| W12               | I/O                     |
| W13               | WD, I/O                 |
| W14               | I/O                     |
| W15               | I/O                     |
| W16               | WD, I/O                 |
| W17               | I/O                     |
| W18               | WD, I/O                 |
| W19               | GND                     |
| W20               | GND                     |
| Y1                | GND                     |
| Y2                | GND                     |
| Y3                | I/O                     |
| Y4                | TDI, I/O                |
| Y5                | WD, I/O                 |
| Y6                | I/O                     |
| Y7                | QCLKA, I/O              |
| Y8                | I/O                     |
| Y9                | I/O                     |
| Y10               | I/O                     |
| Y11               | I/O                     |
| Y12               | I/O                     |