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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

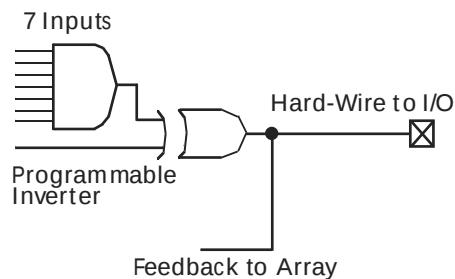
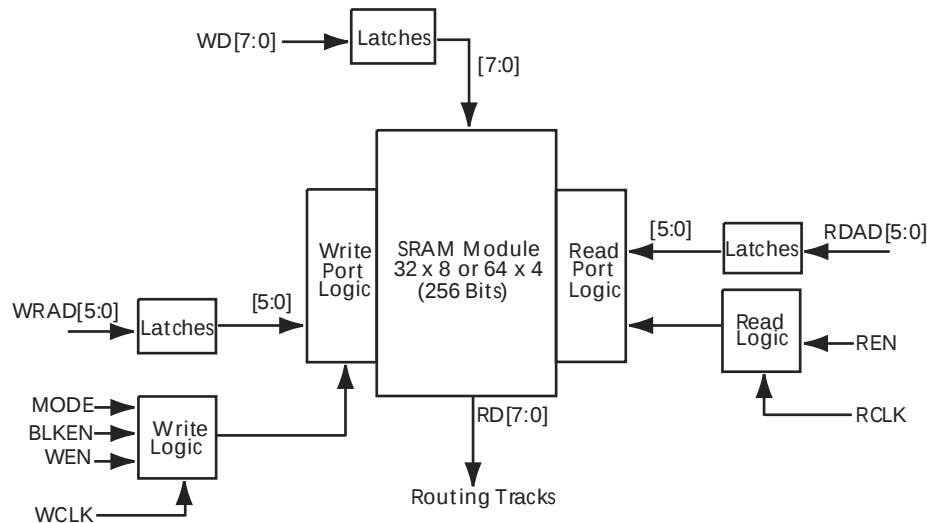
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	6000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	80-TQFP
Supplier Device Package	80-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx04-vqg80i

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Figure 5 • A42MX24 and A42MX36 D-Module Implementation**Figure 6 • A42MX36 Dual-Port SRAM Block**

3.2.3 Routing Structure

The MX architecture uses vertical and horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may be continuous or split into segments. Varying segment lengths allow the interconnect of over 90% of design tracks to occur with only two antifuse connections. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

3.2.3.1 Horizontal Routing

Horizontal routing tracks span the whole row length or are divided into multiple segments and are located in between the rows of modules. Any segment that spans more than one-third of the row length is considered a long horizontal segment. A typical channel is shown in Figure 7, page 10. Within horizontal routing, dedicated routing tracks are used for global clock networks and for power and ground tie-off tracks. Non-dedicated tracks are used for signal nets.

3.2.3.2 Vertical Routing

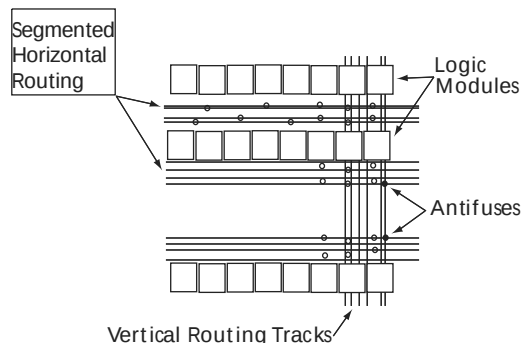
Another set of routing tracks run vertically through the module. There are three types of vertical tracks: input, output, and long. Long tracks span the column length of the module, and can be divided into multiple segments. Each segment in an input track is dedicated to the input of a particular module; each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing.

Each output segment spans four channels (two above and two below), except near the top and bottom of the array, where edge effects occur. Long vertical tracks contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 7, page 10.

3.2.3.3 Antifuse Structures

An antifuse is a “normally open” structure. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient programming algorithms. There are no pre-existing connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For instance, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Figure 7 • MX Routing Structure



3.2.4 Clock Networks

The 40MX devices have one global clock distribution network (CLK). A signal can be put on the CLK network by being routed through the CLKBUF buffer.

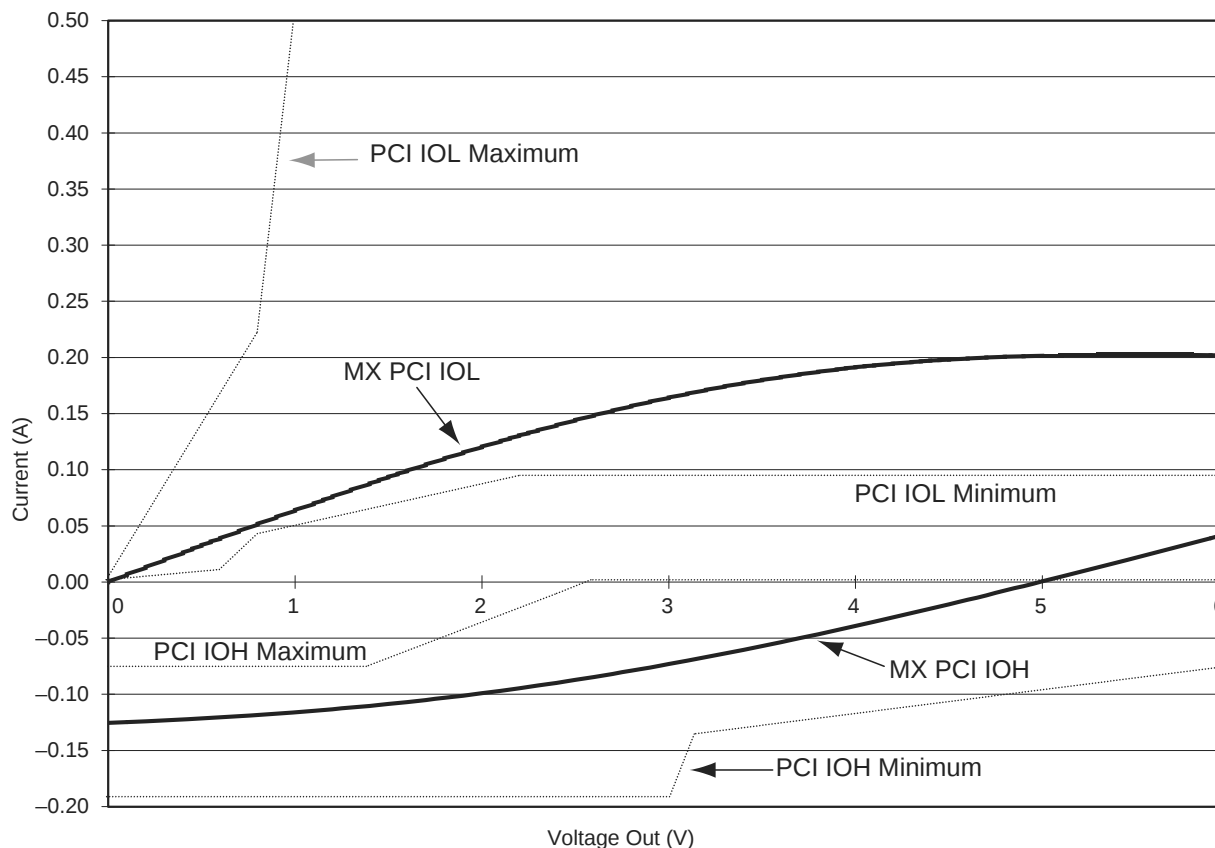
In 42MX devices, there are two low-skew, high-fanout clock distribution networks, referred to as CLKA and CLKB. Each network has a clock module (CLKMOD) that can select the source of the clock signal from any of the following (Figure 8, page 11):

- Externally from the CLKA pad, using CLKBUF buffer
- Externally from the CLKB pad, using CLKBUF buffer
- Internally from the CLKINTA input, using CLKINT buffer
- Internally from the CLKINTB input, using CLKINT buffer

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

Clock input pads in both 40MX and 42MX devices can also be used as normal I/Os, bypassing the clock networks.

The A42MX36 device has four additional register control resources, called quadrant clock networks (Figure 9, page 11). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

Figure 16 • Typical Output Drive Characteristics (Based Upon Measured Data)

3.9.4 Junction Temperature (T_J)

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a(1)$$

EQ 4

where:

- T_a = Ambient Temperature
- ΔT = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$ (2)
- P = Power
- θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in Table 27, page 29.

3.9.5 Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc} , and the junction-to-ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates.

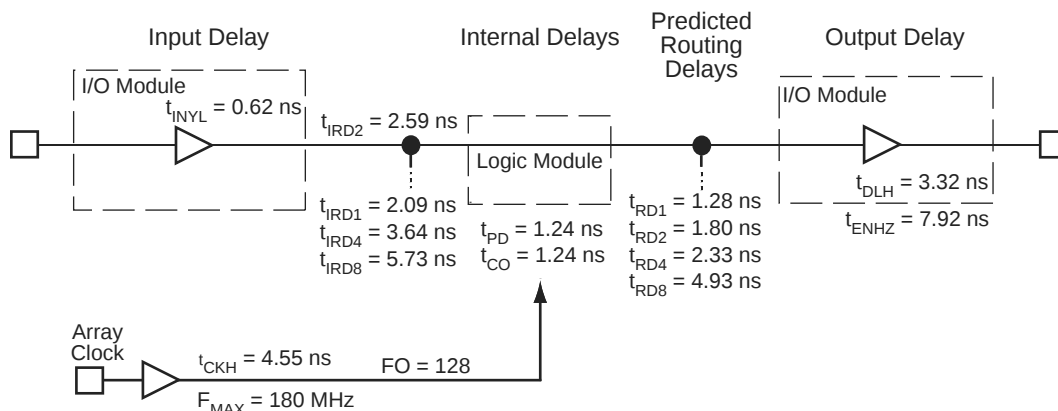
The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of θ_{ja} .

3.10 Timing Models

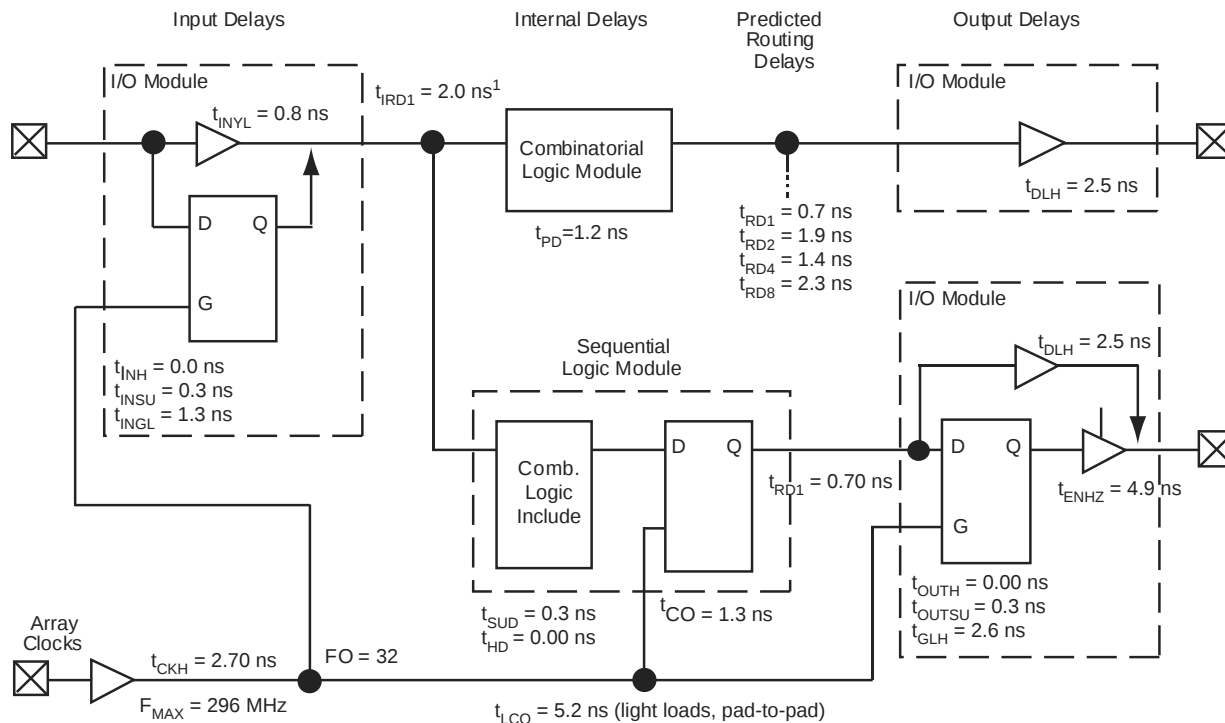
The following figures show various timing models.

Figure 17 • 40MX Timing Model*



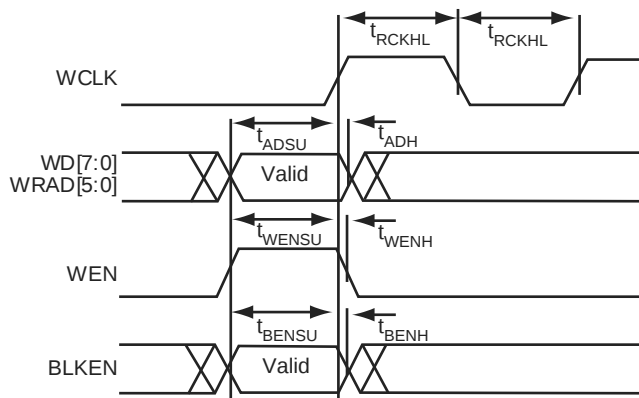
Note: Values are shown for 40MX –3 speed devices at 5.0 V worst-case commercial conditions.

Figure 18 • 42MX Timing Model

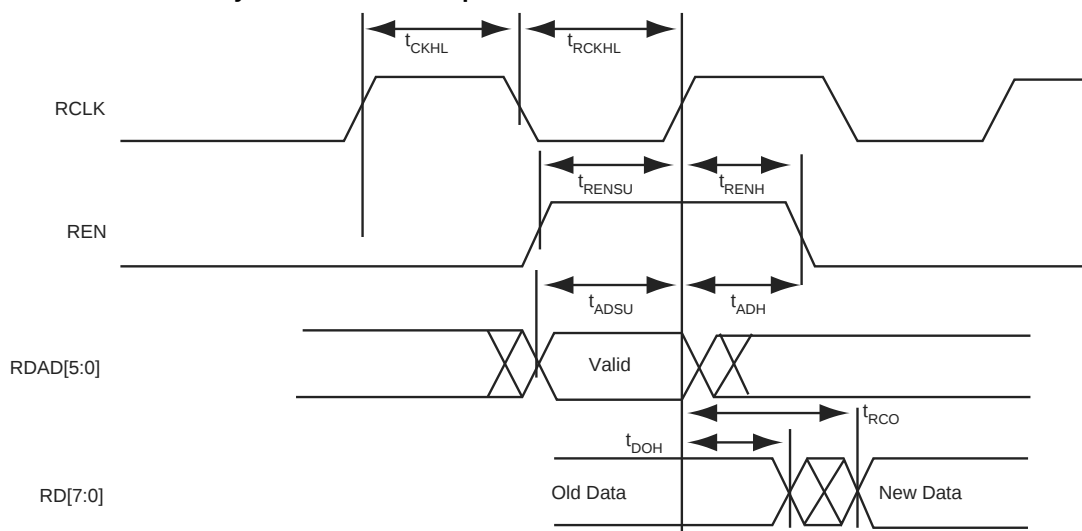


Note: 1. Input module predicted routing delay

Note: 2. Values are shown for A42MX09 –3 at 5.0 V worst-case commercial conditions.

Figure 30 • 42MX SRAM Write Operation

Note: Identical timing for falling edge clock

Figure 31 • 42MX SRAM Synchronous Read Operation

Note: Identical timing for falling edge clock

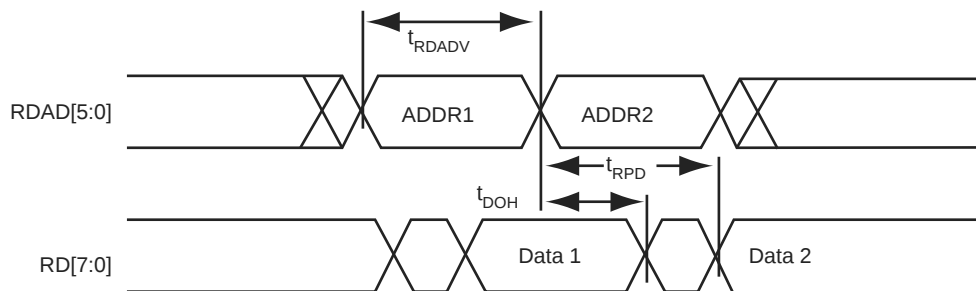
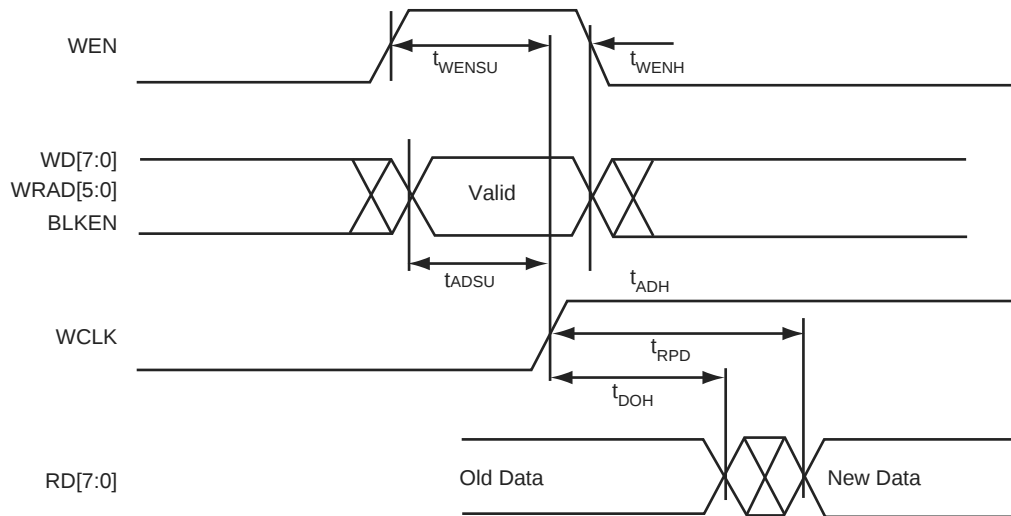
Figure 32 • 42MX SRAM Asynchronous Read Operation—Type 1 (Read Address Controlled)

Figure 33 • 42MX SRAM Asynchronous Read Operation—Type 2 (Write Address Controlled)

3.10.7 Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution, which is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi's patented antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 μm lithography, offer nominal levels of 100 Ω resistance and 7.0 fF capacitance per antifuse.

MX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90 percent of interconnects using only two antifuses.

3.11 Timing Characteristics

Device timing characteristics fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all MX devices. Internal routing delays are device-dependent; actual delays are not determined until after place-and-route of the user's design is complete. Delay values may then be determined by using the Designer software utility or by performing simulation with post-layout delays.

3.11.1 Critical Nets and Typical Nets

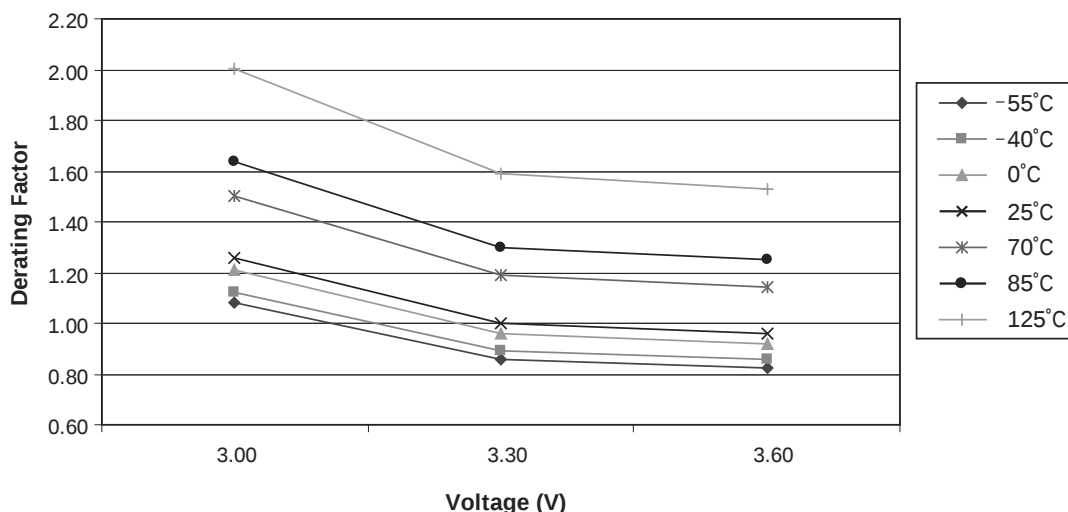
Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment in Microsemi's Designer software prior to placement and routing. Up to 6% of the nets in a design may be designated as critical.

3.11.2 Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks add

Table 31 • 40MX Temperature and Voltage Derating Factors (Normalized to T_J = 25°C, V_{CC} = 3.3 V)

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
3.60	0.83	0.85	0.92	0.96	1.14	1.25	1.53

Figure 37 • 40MX Junction Temperature and Voltage Derating Curves (Normalized to T_J = 25°C, V_{CC} = 3.3 V)

Note: This derating factor applies to all routing and propagation delays

3.11.5 PCI System Timing Specification

The following tables list the critical PCI timing parameters and the corresponding timing parameters for the MX PCI-compliant devices.

3.11.6 PCI Models

Microsemi provides synthesizable VHDL and Verilog-HDL models for a PCI Target interface, a PCI Target and Target+DMA Master interface. Contact the Microsemi sales representative for more details.

Table 32 • Clock Specification for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC}	CLK Cycle Time	30	–	4.0	–	4.0	–	ns
t _{HIGH}	CLK High Time	11	–	1.9	–	1.9	–	ns
t _{LOW}	CLK Low Time	11	–	1.9	–	1.9	–	ns

Table 33 • Timing Parameters for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{VAL}	CLK to Signal Valid—Bused Signals	2	11	2.0	9.0	2.0	9.0	ns
t _{VAL(PTP)}	CLK to Signal Valid—Point-to-Point	2 ²	12	2.0	9.0	2.0	9.0	ns
t _{ON}	Float to Active	2	–	2.0	4.0	2.0	4.0	ns
t _{OFF}	Active to Float	–	28	–	8.3 ¹	–	8.3 ¹	ns
t _{SU}	Input Set-Up Time to CLK—Bused Signals	7	–	1.5	–	1.5	–	ns

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ¹												
t _{DLH}	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t _{DHL}	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t _{ENZH}	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t _{ENZL}	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t _{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t _{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d _{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer utility from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading

Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t _{PD2}	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t _{CO}	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t _{GO}	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays ¹												
t _{RD1}	FO = 1 Routing Delay		1.9		2.2		2.5		3.0		4.2	ns
t _{RD2}	FO = 2 Routing Delay		2.7		3.1		3.5		4.1		5.7	ns
t _{RD3}	FO = 3 Routing Delay		3.4		3.9		4.4		5.2		7.3	ns
t _{RD4}	FO = 4 Routing Delay		4.1		4.8		5.4		6.3		8.9	ns
t _{RD8}	FO = 8 Routing Delay		7.1		8.1		9.2		10.9		15.2	ns
Logic Module Sequential Timing ²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		4.3		5.0		5.6		6.6		9.2	ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		4.3		5.0		5.6		6.6		9.2	ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		3.4		3.8		4.3		5.1		7.1	ns
t _{DHL}	Data-to-Pad LOW		4.0		4.5		5.1		6.1		8.3	ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t _{ENZL}	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t _{ENHZ}	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t _{ENLZ}	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t _{GLH}	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t _{GHL}	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t _{LSU}	I/O Latch Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d _{TLH}	Capacity Loading, LOW to HIGH		0.00		0.00		0.00		0.10		0.01	ns/pF
d _{THL}	Capacity Loading, HIGH to LOW		0.09		0.10		0.10		0.10		0.10	ns/pF

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Sequential Timing ^{3, 4}												
t _{CO}	Flip-Flop Clock-to-Output	2.1		2.0		2.3		2.7		3.7		ns
t _{GO}	Latch Gate-to-Output	3.4		1.9		2.1		2.5		3.4		ns
t _{SUD}	Flip-Flop (Latch) Set-Up Time	0.4		0.5		0.6		0.7		0.9		ns
t _{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RO}	Flip-Flop (Latch) Reset-to-Output	2.0		2.2		2.5		2.9		4.1		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.2		5.8		6.9		9.6		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.1		6.8		7.7		9.0		12.6		ns
Input Module Propagation Delays												
t _{INPY}	Input Data Pad-to-Y	1.4		1.6		1.8		2.2		3.0		ns
t _{INGO}	Input Latch Gate-to-Output	1.8		1.9		2.2		2.6		3.6		ns
t _{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t _{ILA}	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
10	I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O
11	I/O	I/O	I/O	I/O
12	NC	MODE	MODE	MODE
13	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	I/O	I/O	I/O	I/O
18	GND	I/O	I/O	I/O
19	GND	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	VCCA	VCCI	VCCI
23	I/O	VCCI	VCCA	VCCA
24	I/O	I/O	I/O	I/O
25	VCC	I/O	I/O	I/O
26	VCC	I/O	I/O	I/O
27	I/O	I/O	I/O	I/O
28	I/O	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	I/O	I/O	I/O	I/O
31	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	VCC	I/O	I/O	I/O
34	I/O	I/O	I/O	TMS, I/O
35	I/O	I/O	I/O	TDI, I/O
36	I/O	I/O	I/O	WD, I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	WD, I/O
39	I/O	I/O	I/O	WD, I/O
40	GND	I/O	I/O	I/O
41	I/O	I/O	I/O	I/O
42	I/O	I/O	I/O	I/O
43	I/O	VCCA	VCCA	VCCA
44	I/O	I/O	I/O	WD, I/O
45	I/O	I/O	I/O	WD, I/O
46	VCC	I/O	I/O	WD, I/O

Figure 42 • PQ144

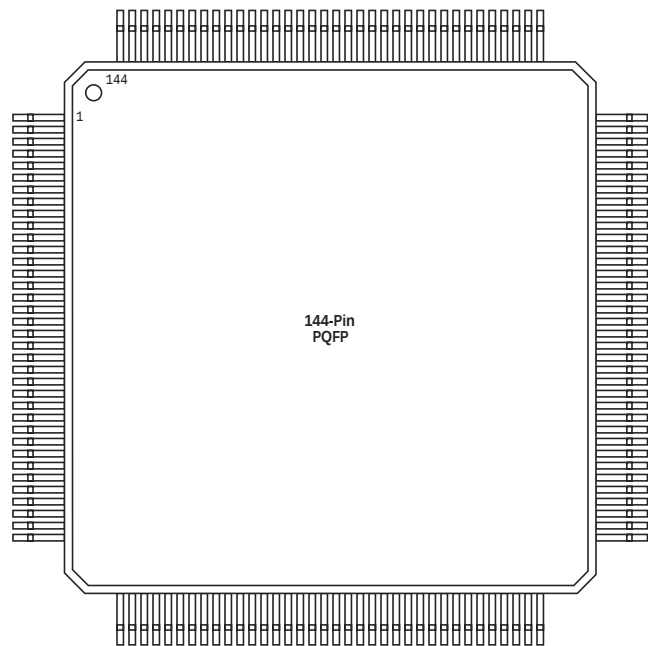


Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
1	I/O
2	MODE
3	I/O
4	I/O
5	I/O

Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
6	I/O
7	I/O
8	I/O
9	GNDQ
10	GNDI
11	NC
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	VSV
19	VCC
20	VCCI
21	NC
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	GND
29	GNDI
30	NC
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	BININ
38	BINOUT
39	I/O
40	I/O
41	I/O
42	I/O

Table 55 • VQ80

VQ80		
Pin Number	A40MX02 Function	A40MX04 Function
13	VCC	VCC
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	NC	I/O
18	NC	I/O
19	NC	I/O
20	VCC	VCC
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	GND	GND
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	VCC	VCC
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O
41	NC	I/O
42	NC	I/O
43	NC	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	GND	GND
48	I/O	I/O

Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	NC	VCCA	VCCA
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	GND	GND	GND
19	NC	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	NC	I/O	I/O
23	GND	GND	GND
24	NC	VCCI	VCCI
25	VCCA	VCCA	VCCA
26	NC	I/O	I/O
27	NC	I/O	I/O
28	VCCI	VCCA	VCCA
29	NC	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	NC	NC	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	NC	I/O	I/O
38	NC	NC	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	GND	GND	GND
46	I/O	I/O	TMS, I/O

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
C3	GND
C4	I/O
C5	WD, I/O
C6	I/O
C7	QCLKC, I/O
C8	I/O
C9	I/O
C10	CLKB
C11	PRA, I/O
C12	WD, I/O
C13	I/O
C14	QCLKD, I/O
C15	I/O
C16	WD, I/O
C17	SDI, I/O
C18	I/O
C19	I/O
C20	I/O
D1	I/O
D2	I/O
D3	I/O
D4	I/O
D5	VCCI
D6	I/O
D7	I/O
D8	VCCA
D9	WD, I/O
D10	VCCI
D11	I/O
D12	VCCI
D13	I/O
D14	VCCI
D15	I/O
D16	VCCA
D17	GND
D18	I/O
D19	I/O

Table 62 • CQ172

21	I/O
22	GND
23	VCCI
24	VSV
25	I/O
26	I/O
27	VCC
28	I/O
29	I/O
30	I/O
31	I/O
32	GND
33	I/O
34	I/O
35	I/O
36	I/O
37	GND
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	BININ
45	BINOUT
46	I/O
47	I/O
48	I/O
49	I/O
50	VCCI
51	I/O
52	I/O
53	I/O
54	I/O
55	GND
56	I/O
57	I/O
58	I/O
59	I/O

Table 62 • CQ172

60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	GND
66	VCC
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	GND
76	I/O
77	I/O
78	I/O
79	I/O
80	VCCI
81	I/O
82	I/O
83	I/O
84	I/O
85	SDO
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	GND

Table 62 • CQ172

99	I/O
100	I/O
101	I/O
102	I/O
103	GND
104	I/O
105	I/O
106	VKS
107	VPP
108	GND
109	VCCI
110	VSV
111	I/O
112	I/O
113	VCC
114	I/O
115	I/O
116	I/O
117	I/O
118	GND
119	I/O
120	I/O
121	I/O
122	I/O
123	GNDI
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	SDI
132	I/O
133	I/O
134	I/O
135	I/O
136	VCCI
137	I/O