Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	101
Number of Gates	14000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx09-1pq160m

- The Transient Current, page 13 is new (SAR 36930).
- Package names were revised according to standards established in *Package Mechanical Drawings* (SAR 34774)

1.7 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document

- In Table 20, page 23, the limits in VI were changed from -0.5 to VCCI + 0.5 to -0.5 to VCCA + 0.5

In Table 22, page 25, V_{OH} was changed from 3.7 to 2.4 for the min in industrial and military. V_{IH} had V_{CCI} and that was changed to VCCA

1.8 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- The Ease of Integration, page 1 was updated
- The Temperature Grade Offerings, page 5 is new
- The Speed Grade Offerings, page 5 is new
- The General Description, page 6 was updated
- The MultiPlex I/O Modules, page 11 was updated
- The User Security, page 12 was updated
- Table 6, page 13 was updated
- The Power Dissipation, page 14 was updated.
- The Static Power Component, page 14 was updated
- The Equivalent Capacitance, page 15 was updated
- Figure 13, page 17 was updated
- Table 10, page 18 was updated.
- Figure 14, page 18 was updated.
- Table 11, page 19 was updated.

Table 1 • **Product profile**

Device	**A40MX02**	**A40MX04**	**A42MX09**	**A42MX16**	**A42MX24**	**A42MX36**
Maximum Flip-Flops	147	273	516	928	1,410	1,822
Clocks	1	1	2	2	2	6
User I/O (maximum)	57	69	104	140	176	202
PCI	–	–	–	–	Yes	Yes
Boundary Scan Test (BST)	–	–	–	–	Yes	Yes
Packages (by pin count)						
PLCC	44, 68	44, 68, 84	84	84	84	–
PQFP	100	100	100, 144, 160	100, 160, 208	160, 208	208, 240
VQFP	80	80	100	100	–	–
TQFP	–	–	176	176	176	–
CQFP	–	–	–	172	–	208, 256
PBGA	–	–	–	–	–	272
CPGA	–	–	132	–	–	–

3 40MX and 42MX FPGAs

3.1 General Description

Microsemi's 40MX and 42MX families offer a cost-effective design solution at 5V. The MX devices are single-chip solutions and provide high performance while shortening the system design and development cycle. MX devices can integrate and consolidate logic implemented in multiple PALs, CPLDs, and FPGAs. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

The MX device architecture is based on Microsemi's patented antifuse technology implemented in a 0.45µm triple-metal CMOS process. With capacities ranging from 3,000 to 54,000 system gates, the MX devices provide performance up to 250 MHz, are live on power-up and have one-fifth the standby power consumption of comparable FPGAs. MX FPGAs provide up to 202 user I/Os and are available in a wide variety of packages and speed grades.

A42MX24 and A42MX36 devices also feature multiPlex I/Os, which support mixed-voltage systems, enable programmable PCI, deliver high-performance operation at both 5.0V and 3.3V, and provide a low-power mode. The devices are fully compliant with the PCI local bus specification (version 2.1). They deliver 200 MHz on-chip operation and 6.1 ns clock-to-output performance.

The 42MX24 and 42MX36 devices include system-level features such as IEEE Standard 1149.1 (JTAG) Boundary Scan Testing and fast wide-decode modules. In addition, the A42MX36 device offers dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The storage elements can efficiently address applications requiring wide data path manipulation and can perform transformation functions such as those required for telecommunications, networking, and DSP.

All MX devices are fully tested over automotive and military temperature ranges. In addition, the largest member of the family, the A42MX36, is available in both CQ208 and CQ256 ceramic packages screened to MIL-STD-883 levels. For easy prototyping and conversion from plastic to ceramic, the CQ208 and PQ208 devices are pin-compatible.

3.2 MX Architectural Overview

The MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within these families are composed of logic modules, I/O modules, routing resources and clock networks, which are the building blocks for fast logic designs. In addition, the A42MX36 device contains embedded dual-port SRAM modules, which are optimized for high-speed data path functions such as FIFOs, LIFOs and scratch pad memory. A42MX24 and A42MX36 also contain wide-decode modules.

3.2.1 Logic Modules

The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources.(see the following figure).

The logic module can implement the four basic logic functions (NAND, AND, OR and NOR) in gates of two, three, or four inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array; latches and flip-flops can be constructed from logic modules whenever required in the application.

3. All outputs unloaded. All inputs = VCC/VCCI or GND

3.8 3.3 V Operating Conditions

The following table shows 3.3 V operating conditions.

Table 16 • **Absolute Maximum Ratings for 40MX Devices***

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCC + 0.5	V
VO	Output Voltage	–0.5 to VCC + 0.5	V
t_{STG}	Storage Temperature	–65 to + 150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 17 • **Absolute Maximum Ratings for 42MX Devices***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCCI+0.5	V
VO	Output Voltage	–0.5 to VCCI+0.5	V
t_{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 18 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCA (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCI (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

All the following tables show various specifications and operating conditions of 40MX and 42MX FPGAs.

3.9.1 Mixed 5.0V/3.3V Electrical Specifications

Table 22 • **Mixed 5.0V/3.3V Electrical Specifications**

		Commercial		Commercial –F		Industrial		Military		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
VOH[1]	IOH = –10 mA	2.4		2.4						V
	IOH = –4 mA					2.4		2.4		V
VOL[1]	IOL = 10 mA		0.5		0.5					V
	IOL = 6 mA						0.4		0.4	V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH[2]		2.0	VCCA + 0.3	2.0	VCCA + 0.3	2.0	VCCA + 0.3	2.0	VCCA + 0.3	V
IL	VIN = 0.5 V		–10		–10		–10		–10	µA
IH	VIN = 2.7 V		–10		–10		–10		–10	µA
Input Transition Time, T_R and T_F			500		500		500		500	ns
C_{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC[3]	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		20		25		25		25	mA
Low Power Mode Standby Current			0.5		ICC – 5.0		ICC – 5.0		ICC – 5.0	mA
IIO I/O source sink current	Can be derived from the *IBIS model* (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCCI = min.
2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
3. All outputs unloaded. All inputs = VCCI or GND

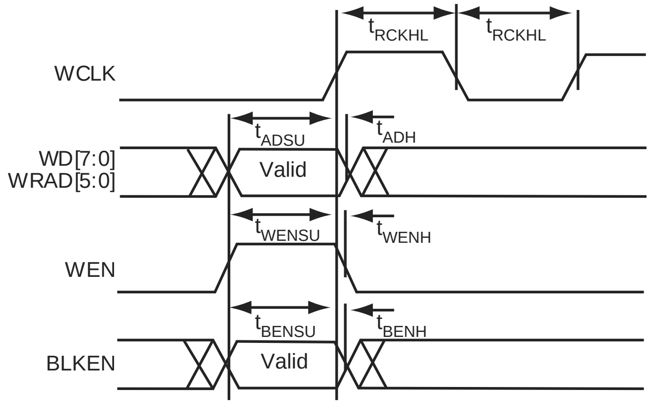
3.9.2 Output Drive Characteristics for 5.0 V PCI Signaling

MX PCI device I/O drivers were designed specifically for high-performance PCI systems. Figure 16, page 28 shows the typical output drive characteristics of the MX devices. MX output drivers are compliant with the PCI Local Bus Specification.

Table 23 • **DC Specification (5.0 V PCI Signaling)[1]**

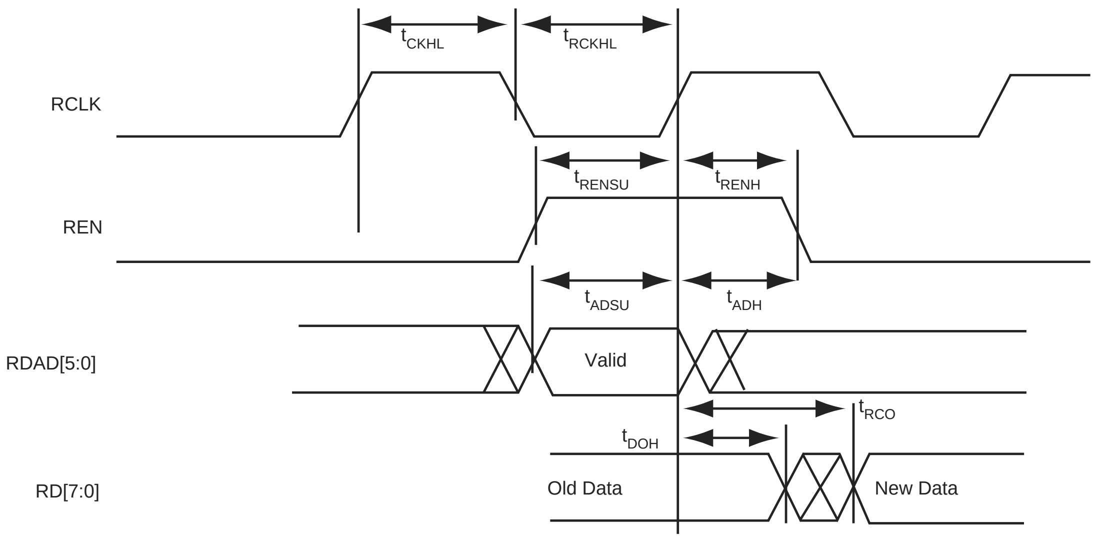
			PCI		MX		
Symbol	**Parameter**	**Condition**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
VCCI	Supply Voltage for I/Os		4.75	5.25	4.75	5.25[2]	V
VIH[3]	Input High Voltage		2.0	VCC + 0.5	2.0	VCCI + 0.3	V
VIL	Input Low Voltage		–0.5	0.8	–0.3	0.8	V
IIH	Input High Leakage Current	VIN = 2.7 V		70	—	10	µA
IIL	Input Low Leakage Current	VIN=0.5 V		–70	—	–10	µA
VOH	Output High Voltage	IOUT = –2 mA IOUT = –6 mA	2.4		 3.84		V
VOL	Output Low Voltage	IOUT = 3 mA, 6 mA		0.55	—	0.33	V

Figure 30 • **42MX SRAM Write Operation**



Note: Identical timing for falling edge clock

Figure 31 • **42MX SRAM Synchronous Read Operation**



Note: Identical timing for falling edge clock

Figure 32 • **42MX SRAM Asynchronous Read Operation—Type 1 (Read Address Controlled)**

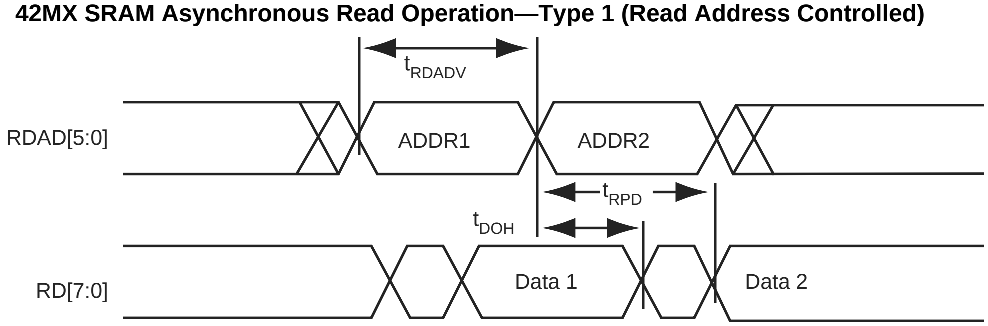


Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[1]												
t_{DLH}	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t_{DHL}	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZH}	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZL}	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t_{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer utility from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading

Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t_{PD1}	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t_{PD2}	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t_{CO}	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t_{GO}	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays[1]												
t_{RD1}	FO = 1 Routing Delay		1.9		2.2		2.5		3.0		4.2	ns
t_{RD2}	FO = 2 Routing Delay		2.7		3.1		3.5		4.1		5.7	ns
t_{RD3}	FO = 3 Routing Delay		3.4		3.9		4.4		5.2		7.3	ns
t_{RD4}	FO = 4 Routing Delay		4.1		4.8		5.4		6.3		8.9	ns
t_{RD8}	FO = 8 Routing Delay		7.1		8.1		9.2		10.9		15.2	ns
Logic Module Sequential Timing[2]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	4.3		5.0		5.6		6.6		9.2		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	4.3		5.0		5.6		6.6		9.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns

Table 37 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t_A	Flip-Flop Clock Input Period	6.8		7.8		8.9		10.4		14.6		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		109		101		92		80		48	MHz
Input Module Propagation Delays												
t_{INYH}	Pad-to-Y HIGH		1.0		1.1		1.3		1.5		2.1	ns
t_{INYL}	Pad-to-Y LOW		0.9		1.0		1.1		1.3		1.9	ns

Table 38 • **A42MX09 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
TTL Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		2.5		2.7		3.1		3.6		5.1	ns
t_{DHL}	Data-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t_{ENZH}	Enable Pad Z to HIGH		2.6		2.9		3.3		3.9		5.5	ns
t_{ENZL}	Enable Pad Z to LOW		2.9		3.2		3.7		4.3		6.1	ns
t_{ENHZ}	Enable Pad HIGH to Z		4.9		5.4		6.2		7.3		10.2	ns
t_{ENLZ}	Enable Pad LOW to Z		5.3		5.9		6.7		7.9		11.1	ns
t_{GLH}	G-to-Pad HIGH		2.6		2.9		3.3		3.8		5.3	ns
t_{GHL}	G-to-Pad LOW		2.6		2.9		3.3		3.8		5.3	ns
t_{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.2		5.8		6.6		7.7		10.8	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.4		8.2		9.3		10.9		15.3	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.04		0.04		0.04		0.05		0.07	ns/pF

Table 42 • **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		3.1		3.5		3.9		4.6		6.4	ns
t_{DHL}	Data-to-Pad LOW		2.4		2.6		3.0		3.5		4.9	ns
t_{ENZH}	Enable Pad Z to HIGH		2.5		2.8		3.2		3.8		5.3	ns
t_{ENZL}	Enable Pad Z to LOW		2.8		3.1		3.5		4.2		5.8	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.2		5.7		6.5		7.6		10.7	ns
t_{ENLZ}	Enable Pad LOW to Z		4.8		5.3		6.0		7.1		9.9	ns
t_{GLH}	G-to-Pad HIGH		4.9		5.4		6.2		7.2		10.1	ns
t_{GHL}	G-to-Pad LOW		4.9		5.4		6.2		7.2		10.1	ns
t_{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.5		6.1		6.9		8.1		11.3	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.6		11.8		13.4		15.7		22.0	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. D*ata applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

Table 43 • **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Logic Module Combinatorial Functions[1]												
t_{PD}	Internal Array Module Delay		2.0		1.8		2.1		2.5		3.4	ns
t_{PDD}	Internal Decode Module Delay		1.1		2.2		2.5		3.0		4.2	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		1.7		1.3		1.4		1.7		2.3	ns
t_{RD2}	FO = 2 Routing Delay		2.0		1.6		1.8		2.1		3.0	ns
t_{RD3}	FO = 3 Routing Delay		1.1		2.0		2.2		2.6		3.7	ns
t_{RD4}	FO = 4 Routing Delay		1.5		2.3		2.6		3.1		4.3	ns
t_{RD5}	FO = 8 Routing Delay		1.8		3.7		4.2		5.0		7.0	ns

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
TTL Output Module Timing[5] (continued)													
t_{LH}	I/O Latch Output Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d_{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing[5]													
t_{DLH}	Data-to-Pad HIGH			4.8		5.3		5.5		6.4		9.0	ns
t_{DHL}	Data-to-Pad LOW			3.5		3.9		4.1		4.9		6.8	ns
t_{ENZH}	Enable Pad Z to HIGH			3.6		4.0		4.5		5.3		7.4	ns
t_{ENZL}	Enable Pad Z to LOW			3.4		4.0		5.0		5.8		8.2	ns
t_{ENHZ}	Enable Pad HIGH to Z			7.2		8.0		9.0		10.7		14.9	ns
t_{ENLZ}	Enable Pad LOW to Z			6.7		7.5		8.5		9.9		13.9	ns
t_{GLH}	G-to-Pad HIGH			6.8		7.6		8.6		10.1		14.2	ns
t_{GHL}	G-to-Pad LOW			6.8		7.6		8.6		10.1		14.2	ns
t_{LSU}	I/O Latch Set-Up		0.7		0.7		0.8		1.0		1.4		ns
t_{LH}	I/O Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d_{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 486	3.9 4.6		4.3 5.2		4.9 5.8		5.7 6.9		8.1 9.6		ns ns
t_P	Minimum Period ($1/f_{MAX}$)	FO = 32 FO = 486	7.8 8.6		8.7 9.5		9.5 10.4		10.8 11.9		18.2 19.9		ns ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 48 • **PL68**

PL68		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	GND	GND
67	I/O	I/O
68	I/O	I/O

Figure 40 • **PL84**

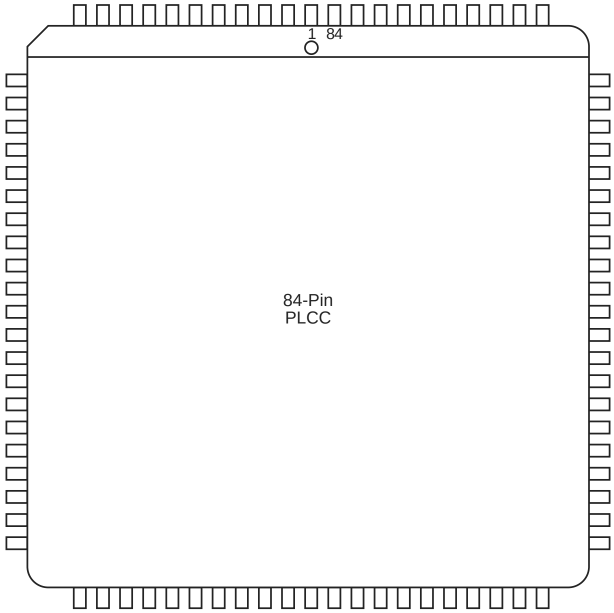


Table 49 • **PL84**

PL84				
Pin Number	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
1	I/O	I/O	I/O	I/O
2	I/O	CLKB, I/O	CLKB, I/O	CLKB, I/O
3	I/O	I/O	I/O	I/O
4	VCC	PRB, I/O	PRB, I/O	PRB, I/O
5	I/O	I/O	I/O	WD, I/O
6	I/O	GND	GND	GND
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	WD, I/O
9	I/O	I/O	I/O	WD, I/O

Table 51 • **PQ144**

PQ144	
Pin Number	**A42MX09 Function**
80	GNDI
81	NC
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	I/O
88	VKS
89	VPP
90	VCC
91	VCCI
92	NC
93	VSV
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	GND
101	GNDI
102	NC
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	I/O
109	I/O
110	SDI
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	GNDQ

Table 57 • **TQ176**

TQ176			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	NC	VCCA	VCCA
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	GND	GND	GND
19	NC	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	NC	I/O	I/O
23	GND	GND	GND
24	NC	VCCI	VCCI
25	VCCA	VCCA	VCCA
26	NC	I/O	I/O
27	NC	I/O	I/O
28	VCCI	VCCA	VCCA
29	NC	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	NC	NC	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	NC	I/O	I/O
38	NC	NC	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	GND	GND	GND
46	I/O	I/O	TMS, I/O

Table 57 • **TQ176**

TQ176			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
158	CLKB, I/O	CLKB, I/O	CLKB, I/O
159	I/O	I/O	I/O
160	PRB, I/O	PRB, I/O	PRB, I/O
161	NC	I/O	WD, I/O
162	I/O	I/O	WD, I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	NC	NC	WD, I/O
166	NC	I/O	WD, I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	I/O	I/O	I/O
170	NC	VCCI	VCCI
171	I/O	I/O	WD, I/O
172	I/O	I/O	WD, I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	DCLK, I/O	DCLK, I/O	DCLK, I/O
176	I/O	I/O	I/O

Figure 49 • **CQ208**

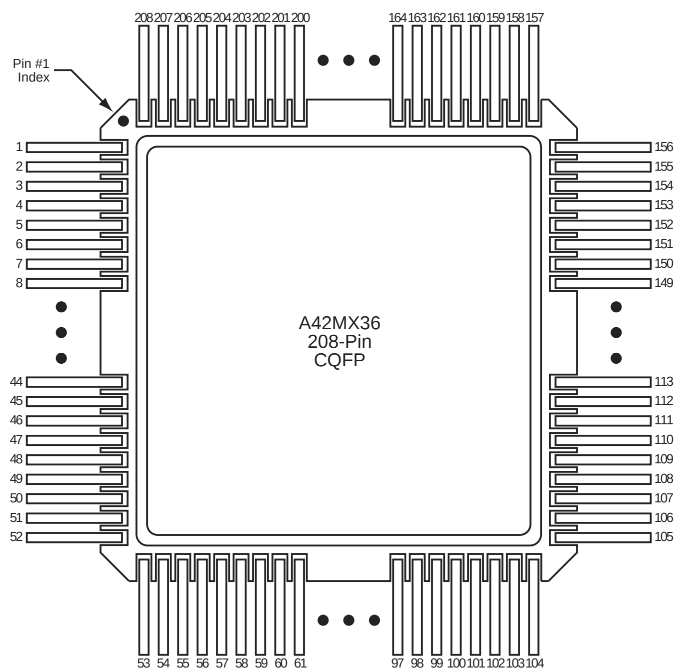


Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
207	I/O
208	I/O
209	QCLKC, I/O
210	I/O
211	WD, I/O
212	WD, I/O
213	I/O
214	I/O
215	WD, I/O
216	WD, I/O
217	I/O
218	PRB, I/O
219	I/O
220	CLKB, I/O
221	I/O
222	GND
223	GND
224	VCCA
225	VCCI
226	I/O
227	CLKA, I/O
228	I/O
229	PRA, I/O
230	I/O
231	I/O
232	WD, I/O
233	WD, I/O
234	I/O
235	I/O
236	I/O
237	I/O
238	I/O
239	I/O
240	QCLKD, I/O
241	I/O
242	WD, I/O
243	GND

Table 61 • **PG132**

PG132	
Pin Number	**A42MX09 Function**
B3	I/O
A2	I/O
C3	DCLK
B5	GNDA
E12	GNDA
J2	GNDA
M9	GNDA
B9	GNDI
C5	GNDI
E11	GNDI
F4	GNDI
J3	GNDI
J11	GNDI
L5	GNDI
L9	GNDI
C9	GNDQ
E3	GNDQ
K12	GNDQ
D7	VCCA
G3	VCCA
G10	VCCA
L7	VCCA
C7	VCCI
G2	VCCI
G11	VCCI
K7	VCCI

Figure 53 • **CQ172**

Table 62 • **CQ172**

CQ172	
Pin Number	**A42MX16 Function**
1	MODE
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	GND
8	I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	I/O
17	GND
18	I/O
19	I/O
20	I/O

Table 62 • **CQ172**

21	I/O
22	GND
23	VCCI
24	VSV
25	I/O
26	I/O
27	VCC
28	I/O
29	I/O
30	I/O
31	I/O
32	GND
33	I/O
34	I/O
35	I/O
36	I/O
37	GND
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	BININ
45	BINOUT
46	I/O
47	I/O
48	I/O
49	I/O
50	VCCI
51	I/O
52	I/O
53	I/O
54	I/O
55	GND
56	I/O
57	I/O
58	I/O
59	I/O