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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	101
Number of Gates	14000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx09-1pqg160i

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2 40MX and 42MX FPGA Families

2.1 Features

The following sections list out various features of the 40MX and 42MX FPGA family devices.

2.1.1 High Capacity

- Single-Chip ASIC Alternative
- 3,000 to 54,000 System Gates
- Up to 2.5 kbits Configurable Dual-Port SRAM
- Fast Wide-Decode Circuitry
- Up to 202 User-Programmable I/O Pins

2.1.2 High Performance

- 5.6 ns Clock-to-Out
- 250 MHz Performance
- 5 ns Dual-Port SRAM Access
- 100 MHz FIFOs
- 7.5 ns 35-Bit Address Decode

2.1.3 HiRel Features

- Commercial, Industrial, Automotive, and Military Temperature Plastic Packages
- Commercial, Military Temperature, and MIL-STD-883 Ceramic Packages
- QML Certification
- Ceramic Devices Available to DSCC SMD

2.1.4 Ease of Integration

- Mixed-Voltage Operation (5.0 V or 3.3 V for core and I/Os), with PCI-Compliant I/Os
- Up to 100% Resource Utilization and 100% Pin Locking
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Low Power Consumption
- IEEE Standard 1149.1 (JTAG) Boundary Scan Testing

2.2 Product Profile

The following table gives the features of the products.

Table 1 • **Product profile**

Device	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
Capacity						
System Gates	3,000	6,000	14,000	24,000	36,000	54,000
SRAM Bits	–	–	–	–	–	2,560
Logic Modules						
Sequential	–	–	348	624	954	1,230
Combinatorial	295	547	336	608	912	1,184
Decode	–	–	–	–	24	24
Clock-to-Out	9.5 ns	9.5 ns	5.6 ns	6.1 ns	6.1 ns	6.3 ns
SRAM Modules (64x4 or 32x8)	–	–	–	–	–	10
Dedicated Flip-Flops	–	–	348	624	954	1,230

Table 1 • **Product profile**

Device	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
Maximum Flip-Flops	147	273	516	928	1,410	1,822
Clocks	1	1	2	2	2	6
User I/O (maximum)	57	69	104	140	176	202
PCI	–	–	–	–	Yes	Yes
Boundary Scan Test (BST)	–	–	–	–	Yes	Yes
Packages (by pin count)						
PLCC	44, 68	44, 68, 84	84	84	84	–
PQFP	100	100	100, 144, 160	100, 160, 208	160, 208	208, 240
VQFP	80	80	100	100	–	–
TQFP	–	–	176	176	176	–
CQFP	–	–	–	172	–	208, 256
PBGA	–	–	–	–	–	272
CPGA	–	–	132	–	–	–

2.6 Temperature Grade Offerings

Table 4 • **Temperature Grade Offerings**

Package	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PLCC 44	C, I, M	C, I, M				
PLCC 68	C, I, A, M	C, I, M				
PLCC 84		C, I, A, M	C, I, A, M	C, I, M	C, I, M	
PQFP 100	C, I, A, M	C, I, A, M	C, I, A, M	C, I, M		
PQFP 144			C			
PQFP 160			C, I, A, M	C, I, M	C, I, A, M	
PQFP 208				C, I, A, M	C, I, A, M	C, I, A, M
PQFP 240						C, I, A, M
VQFP 80	C, I, A, M	C, I, A, M				
VQFP 100			C, I, A, M	C, I, A, M		
TQFP 176			C, I, A, M	C, I, A, M	C, I, A, M	
PBGA 272						C, I, M
CQFP 172				C, M, B		
CQFP 208						C, M, B
CQFP 256						C, M, B
CPGA 132			C, M, B			

Note: C = Commercial
I = Industrial
A = Automotive
M = Military
B = MIL-STD-883 Class B

2.7 Speed Grade Offerings

Table 5 • **Speed Grade Offerings**

	– F	Std	–1	–2	–3
C	P	P	P	P	P
I		P	P	P	P
A		P			
M		P	P		
B		P	P		

Note: See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local *Microsemi Sales representative* for device availability.

Figure 8 • **Clock Networks of 42MX Devices**

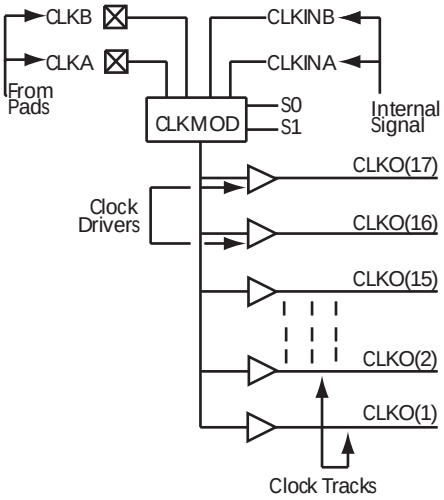
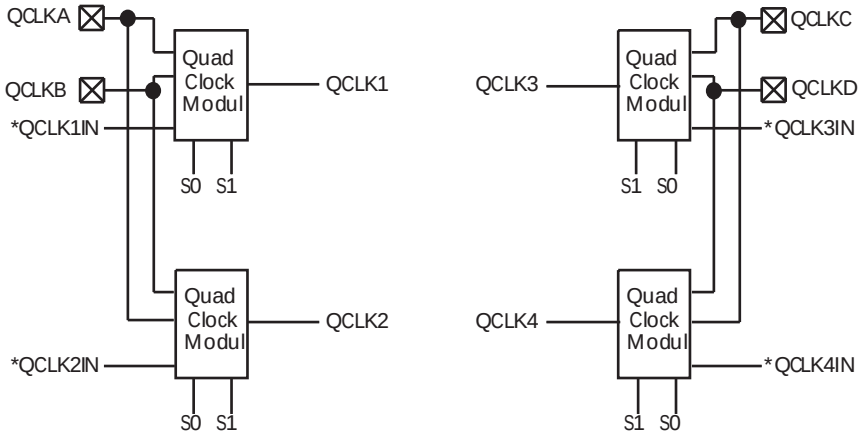


Figure 9 • **Quadrant Clock Network of A42MX36 Devices**



Note: *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

3.2.5 MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 10, page 12 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (See the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 10, page 12). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. See the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 µA.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 11, page 12). When the PCI fuse is not programmed, the output drive is standard.

3.9.3 Output Drive Characteristics for 3.3 V PCI Signaling

Table 25 • **DC Specification (3.3 V PCI Signaling)[1]**

			PCI		MX		
Symbol	**Parameter**	**Condition**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
VCCI	Supply Voltage for I/Os		3.0	3.6	3.0	3.6[2]	V
VIH	Input High Voltage		0.5	VCC + 0.5	0.5	VCCI + 0.3	V
VIL	Input Low Voltage		–0.5	0.8	–0.3	0.8	V
IIH	Input High Leakage Current	VIN = 2.7 V		70		10	µA
IIL	Input Leakage Current			–70		–10	µA
VOH	Output High Voltage	IOUT = –2 mA	0.9		3.3		V
VOL	Output Low Voltage	IOUT = 3 mA, 6 mA		0.1		0.1 VCCI	V
C_{IN}	Input Pin Capacitance			10		10	pF
C_{CLK}	CLK Pin Capacitance		5	12		10	pF
L_{PIN}	Pin Inductance			20		< 8 nH[3]	nH

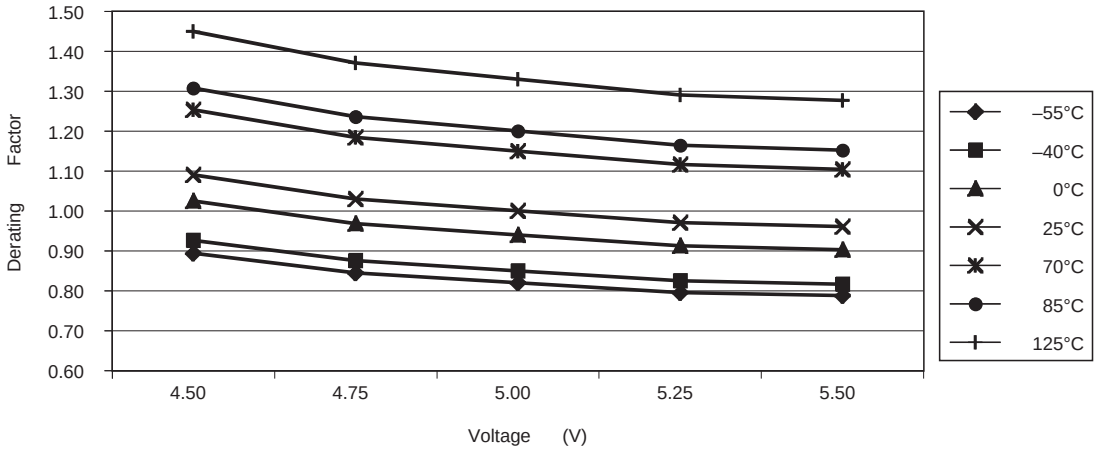
1. PCI Local Bus Specification, Version 2.1, Section 4.2.2.1.
2. Maximum rating for VCCI –0.5 V to 7.0V.
3. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

Table 26 • **AC Specifications for (3.3 V PCI Signaling)***

			PCI		MX		
Symbol	**Parameter**	**Condition**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
ICL	Low Clamp Current	–5 < VIN ≤ –1	–25 + (VIN +1) /0.015		–60	–10	mA
Slew (r)	Output Rise Slew Rate	0.2 V to 0.6 V load	1	4	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	0.6 V to 0.2 V load	1	4	2.8	4.0	V/ns

Note: *PCI Local Bus Specification, Version 2.1, Section 4.2.2.2.

Figure 35 • **40MX Junction Temperature and Voltage Derating Curves (Normalized to TJ = 25°C, VCC = 5.0 V)**

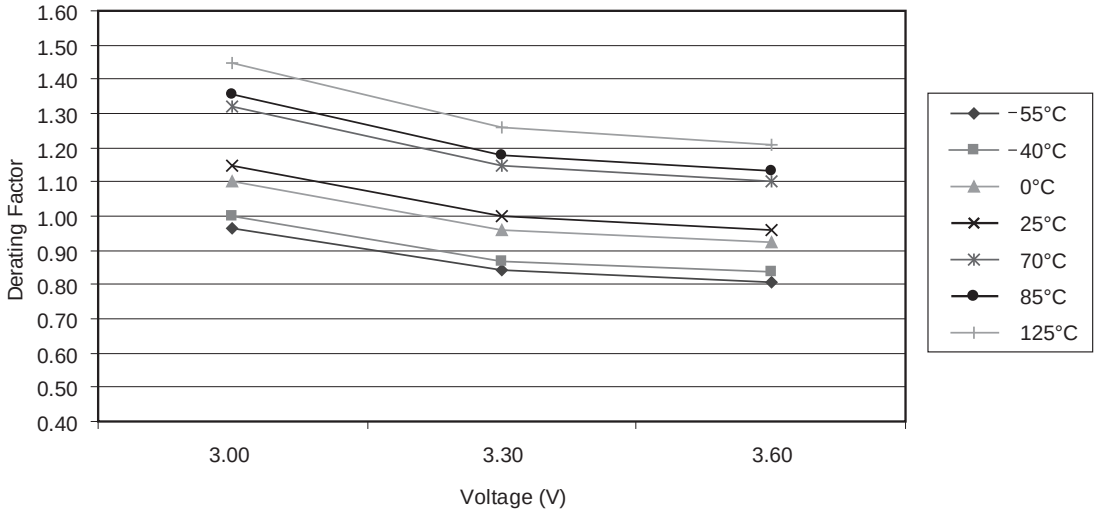


Note: This derating factor applies to all routing and propagation delays

Table 30 • **42MX Temperature and Voltage Derating Factors(Normalized to TJ = 25°C, VCCA = 3.3 V)**

	Temperature						
42MX Voltage	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
3.00	0.97	1.00	1.10	1.15	1.32	1.36	1.45
3.30	0.84	0.87	0.96	1.00	1.15	1.18	1.26
3.60	0.81	0.84	0.92	0.96	1.10	1.13	1.21

Figure 36 • **42MX Junction Temperature and Voltage Derating Curves (Normalized to TJ = 25°C, VCCA = 3.3 V)**



Note: This derating factor applies to all routing and propagation delays

Table 31 • **40MX Temperature and Voltage Derating Factors (Normalized to TJ = 25°C, VCC = 3.3 V)**

	Temperature						
40MX Voltage	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
3.00	1.08	1.12	1.21	1.26	1.50	1.64	2.00
3.30	0.86	0.89	0.96	1.00	1.19	1.30	1.59

Table 35 • **A40MX02 Timing Characteristics (Nominal 3.3 V Operation) *(continued)***
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RD1}	FO = 1 Routing Delay			2.0		2.2		2.5		3.0		4.2	ns
t_{RD2}	FO = 2 Routing Delay			2.7		3.1		3.5		4.1		5.7	ns
t_{RD3}	FO = 3 Routing Delay			3.4		3.9		4.4		5.2		7.3	ns
t_{RD4}	FO = 4 Routing Delay			4.2		4.8		5.4		6.3		8.9	ns
t_{RD8}	FO = 8 Routing Delay			7.1		8.2		9.2		10.9		15.2	ns
Logic Module Sequential Timing[2]													
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up		4.3		4.9		5.6		6.6		9.2		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up		4.3		4.9		5.6		6.6		9.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		4.6		5.3		6.0		7.0		9.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		4.6		5.3		6.0		7.0		9.8		ns
t_A	Flip-Flop Clock Input Period		6.8		7.8		8.9		10.4		14.6		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)			109		101		92		80		48	MHz
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			1.0		1.1		1.3		1.5		2.1	ns
t_{INYL}	Pad-to-Y LOW			0.9		1.0		1.1		1.3		1.9	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO = 1 Routing Delay			2.9		3.4		3.8		4.5		6.3	ns
t_{IRD2}	FO = 2 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t_{IRD3}	FO = 3 Routing Delay			4.4		5.0		5.7		6.7		9.4	ns
t_{IRD4}	FO = 4 Routing Delay			5.1		5.9		6.7		7.8		11.0	ns
t_{IRD8}	FO = 8 Routing Delay			8.0		9.26		10.5		12.6		17.3	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 16 FO = 128		6.4 6.4		7.4 7.4		8.3 8.3		9.8 9.8		13.7 13.7	ns
t_{CKL}	Input HIGH to LOW	FO = 16 FO = 128		6.7 6.7		7.8 7.8		8.8 8.8		10.4 10.4		14.5 14.5	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 16 FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 16 FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t_{CKSW}	Maximum Skew	FO = 16 FO = 128		0.6 0.8		0.6 0.9		0.7 1.0		0.8 1.2		1.2 1.6	ns

Table 37 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[4]												
t_{DLH}	Data-to-Pad HIGH		5.5		6.4		7.2		8.5		11.9	ns
t_{DHL}	Data-to-Pad LOW		4.8		5.5		6.2		7.3		10.2	ns
t_{ENZH}	Enable Pad Z to HIGH		4.7		5.5		6.2		7.3		10.2	ns
t_{ENZL}	Enable Pad Z to LOW		6.8		7.9		8.9		10.5		14.7	ns
t_{ENHZ}	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9	ns
t_{ENLZ}	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7	ns
d_{TLH}	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading.

Table 38 • **A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays[1]												
t_{PD1}	Single Module		1.2		1.3		1.5		1.8		2.5	ns
t_{CO}	Sequential Clock-to-Q		1.3		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch G-to-Q		1.2		1.4		1.6		1.8		2.6	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.6		1.8		2.1		2.9	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t_{RD2}	FO = 2 Routing Delay		0.9		1.0		1.2		1.4		1.9	ns
t_{RD3}	FO = 3 Routing Delay		1.2		1.3		1.5		1.7		2.4	ns
t_{RD4}	FO = 4 Routing Delay		1.4		1.5		1.7		2.0		2.9	ns
t_{RD8}	FO = 8 Routing Delay		2.3		2.6		2.9		3.4		4.8	ns
Logic Module Sequential Timing[3, 4]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.3		0.4		0.4		0.5		0.7		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.4		0.5		0.5		0.6		0.8		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.4		3.8		4.3		5.0		7.0		ns

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		3.4		3.8		4.3		5.1		7.1	ns
t_{DHL}	Data-to-Pad LOW		4.0		4.5		5.1		6.1		8.3	ns
t_{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t_{ENZL}	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t_{ENLZ}	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t_{GLH}	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t_{GHL}	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t_{LSU}	I/O Latch Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad),64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.00		0.00		0.00		0.10		0.01	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.09		0.10		0.10		0.10		0.10	ns/pF

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		3.4		3.8		5.5		6.4		9.0	ns
t_{DHL}	Data-to-Pad LOW		4.1		4.5		4.2		5.0		7.0	ns
t_{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t_{ENZL}	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t_{ENLZ}	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t_{GLH}	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t_{GHL}	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t_{LSU}	I/O Latch Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. *Delays based on 35 pF loading.*

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays[1]												
t_{PD1}	Single Module		1.4		1.5		1.7		2.0		2.8	ns
t_{CO}	Sequential Clock-to-Q		1.4		1.6		1.8		2.1		3.0	ns
t_{GO}	Latch G-to-Q		1.4		1.5		1.7		2.0		2.8	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.6		1.7		2.0		2.3		3.3	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.8		0.9		1.0		1.2		1.6	ns
t_{RD2}	FO = 2 Routing Delay		1.0		1.2		1.3		1.5		2.1	ns

Table 44 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Asynchronous SRAM Operations													
t_{RPD}	Asynchronous Access Time			8.1		9.0		10.2		12.0		16.8	ns
t_{RDADV}	Read Address Valid		8.8		9.8		11.1		13.0		18.2		ns
t_{ADSU}	Address/Data Set-Up Time		1.6		1.8		2.0		2.4		3.4		ns
t_{ADH}	Address/Data Hold Time		0.0		0.0		0.0		0.0		0.0		ns
t_{RENSUA}	Read Enable Set-Up to Address Valid		0.6		0.7		0.8		0.9		1.3		ns
t_{RENHA}	Read Enable Hold		3.4		3.8		4.3		5.0		7.0		ns
t_{WENSU}	Write Enable Set-Up		2.7		3.0		3.4		4.0		5.6		ns
t_{WENH}	Write Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time			1.2		1.3		1.5		1.8		2.5	ns
Input Module Propagation Delays													
t_{INPY}	Input Data Pad-to-Y			1.0		1.1		1.3		1.5		2.1	ns
t_{INGO}	Input Latch Gate-to-Output			1.4		1.6		1.8		2.1		2.9	ns
t_{INH}	Input Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up		0.5		0.5		0.6		0.7		1.0		ns
t_{ILA}	Latch Active Pulse Width		4.7		5.2		5.9		6.9		9.7		ns
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			2.0		2.2		2.5		2.9		4.1	ns
t_{IRD2}	FO = 2 Routing Delay			2.3		2.6		2.9		3.4		4.8	ns
t_{IRD3}	FO = 3 Routing Delay			2.6		2.9		3.3		3.9		5.5	ns
t_{IRD4}	FO = 4 Routing Delay			3.0		3.3		3.8		4.4		6.2	ns
t_{IRD8}	FO = 8 Routing Delay			4.3		4.8		5.5		6.4		9.0	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		2.7		3.0		3.4		4.0		5.6	ns
		FO = 635		3.0		3.3		3.8		4.4		6.2	ns
t_{CKL}	Input HIGH to LOW	FO = 32		3.8		4.2		4.8		5.6		7.8	ns
		FO = 635		4.9		5.4		6.1		7.2		10.1	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	1.8		2.0		2.2		2.6		3.6		ns
		FO = 635	2.0		2.2		2.5		2.9		4.1		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	1.8		2.0		2.2		2.6		3.6		ns
		FO = 635	2.0		2.2		2.5		2.9		4.1		ns
t_{CKSW}	Maximum Skew	FO = 32		0.8		0.8		0.9		1.0		1.4	ns
		FO = 635		0.8		0.8		0.9		1.0		1.4	ns

4 Package Pin Assignments

The following figures and tables give the details of the package pin assignments.

Figure 38 • **PL44**

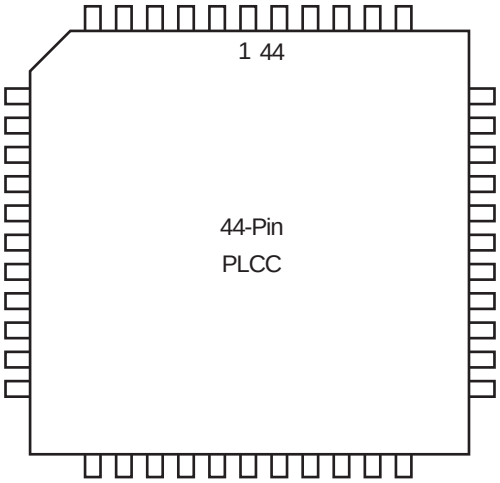


Table 47 • **PL44**

PL44		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
1	I/O	I/O
2	I/O	I/O
3	VCC	VCC
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	GND	GND
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	VCC	VCC
15	I/O	I/O
16	VCC	VCC
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O

Table 47 • **PL44**

PL44		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
21	GND	GND
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	VCC	VCC
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	CLK, I/O	CLK, I/O
34	MODE	MODE
35	VCC	VCC
36	SDI, I/O	SDI, I/O
37	DCLK, I/O	DCLK, I/O
38	PRA, I/O	PRA, I/O
39	PRB, I/O	PRB, I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	GND	GND
44	I/O	I/O

Table 52 • **PQ160**

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
58	VCCI	VCCI	VCCI
59	GND	GND	GND
60	VCCA	VCCA	VCCA
61	LP	LP	LP
62	I/O	I/O	TCK, I/O
63	I/O	I/O	I/O
64	GND	GND	GND
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	I/O	I/O	I/O
69	GND	GND	GND
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	I/O	I/O	I/O
77	NC	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	GND	GND	GND
81	I/O	I/O	I/O
82	SDO, I/O	SDO, I/O	SDO, TDO, I/O
83	I/O	I/O	WD, I/O
84	I/O	I/O	WD, I/O
85	I/O	I/O	I/O
86	NC	VCCI	VCCI
87	I/O	I/O	I/O
88	I/O	I/O	WD, I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O

Table 52 • **PQ160**

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	VCCA	VCCA
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	VCCA	VCCA
139	VCCI	VCCI	VCCI
140	GND	GND	GND
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	GND	GND	GND
146	NC	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	NC	VCCA	VCCA
151	NC	I/O	I/O
152	NC	I/O	I/O
153	NC	I/O	I/O
154	NC	I/O	I/O
155	GND	GND	GND
156	I/O	I/O	I/O
157	I/O	I/O	I/O
158	I/O	I/O	I/O
159	MODE	MODE	MODE
160	GND	GND	GND

Table 53 • **PQ208**

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
21	I/O	I/O	I/O
22	GND	GND	GND
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	GND	GND	GND
28	VCCI	VCCI	VCCI
29	VCCA	VCCA	VCCA
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	VCCA	VCCA	VCCA
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	NC	I/O	I/O
42	NC	I/O	I/O
43	NC	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	NC	I/O	I/O
52	GND	GND	GND
53	GND	GND	GND
54	I/O	TMS, I/O	TMS, I/O
55	I/O	TDI, I/O	TDI, I/O
56	I/O	I/O	I/O
57	I/O	WD, I/O	WD, I/O

Table 57 • **TQ176**

TQ176			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
158	CLKB, I/O	CLKB, I/O	CLKB, I/O
159	I/O	I/O	I/O
160	PRB, I/O	PRB, I/O	PRB, I/O
161	NC	I/O	WD, I/O
162	I/O	I/O	WD, I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	NC	NC	WD, I/O
166	NC	I/O	WD, I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	I/O	I/O	I/O
170	NC	VCCI	VCCI
171	I/O	I/O	WD, I/O
172	I/O	I/O	WD, I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	DCLK, I/O	DCLK, I/O	DCLK, I/O
176	I/O	I/O	I/O

Figure 49 • **CQ208**

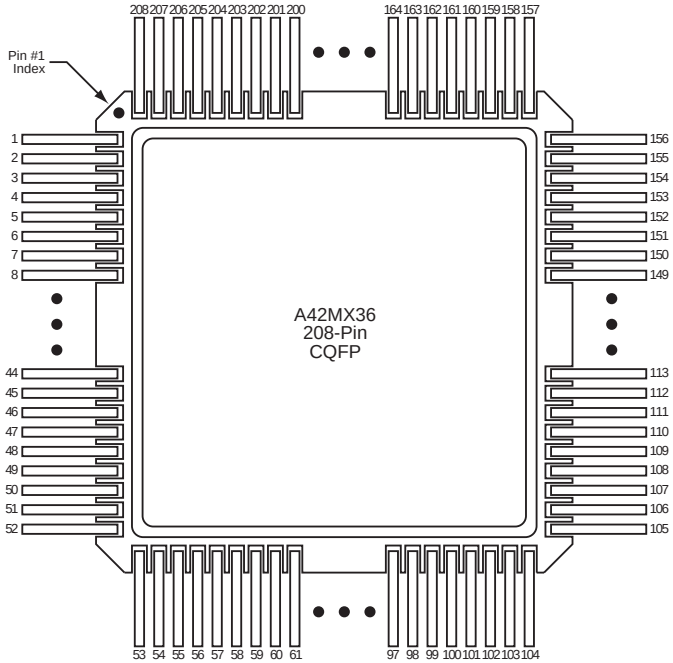


Table 58 • **CQ208**

CQ208	
Pin Number	**A42MX36 Function**
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	GND
53	GND
54	TMS, I/O
55	TDI, I/O
56	I/O
57	WD, I/O
58	WD, I/O
59	I/O
60	VCCI
61	I/O
62	I/O
63	I/O
64	I/O
65	QCLKA, I/O
66	WD, I/O
67	WD, I/O
68	I/O
69	I/O
70	WD, I/O
71	WD, I/O
72	I/O
73	I/O

Table 61 • **PG132**

PG132	
Pin Number	**A42MX09 Function**
F2	I/O
F1	I/O
G1	I/O
G4	VSV
H1	I/O
H2	I/O
H3	I/O
H4	I/O
J1	I/O
K1	I/O
L1	I/O
K2	I/O
M1	I/O
K3	I/O
L2	I/O
N1	I/O
L3	BININ
M2	BINOUT
N2	I/O
M3	I/O
L4	I/O
N3	I/O
M4	I/O
N4	I/O
M5	I/O
K6	I/O
N5	I/O
N6	I/O
L6	I/O
M6	I/O
M7	I/O
N7	I/O
N8	I/O
M8	I/O
L8	I/O
K8	I/O
N9	I/O