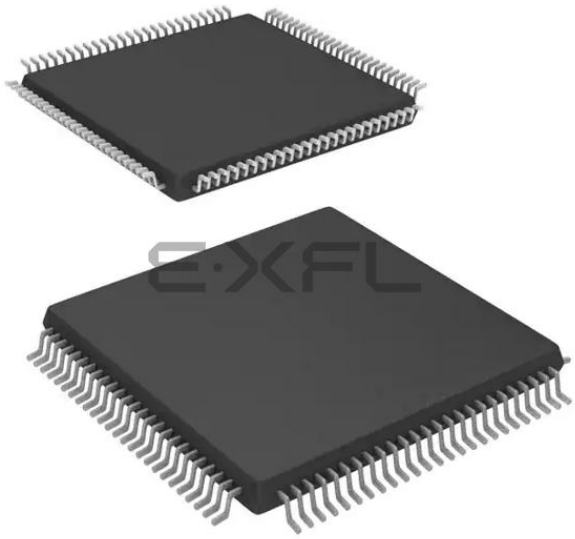

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 83 |
| Number of Gates | 14000 |
| Voltage - Supply | 3V ~ 3.6V, 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a42mx09-1vqg100i |

***Figure 13 •*** **Silicon Explorer II Setup with 42MX**

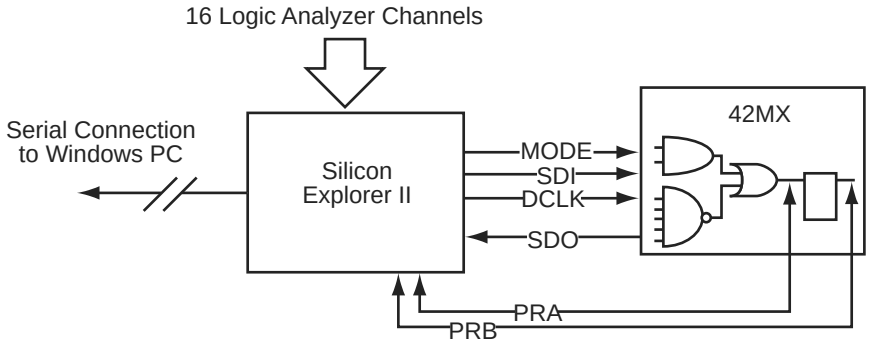



***Table 8 •*** **Device Configuration Options for Probe Capability**

| Security Fuse(s) Programmed | Mode | PRA, PRB[1] | SDI, SDO, DCLK[1] |
|---|---|---|---|
| No | LOW | User I/Os[2] | User I/Os[2] |
| No | HIGH | Probe Circuit Outputs | Probe Circuit Inputs |
| Yes | – | Probe Circuit Secured | Probe Circuit Secured |

1. *Avoid using SDI, SDO, DCLK, PRA and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
2. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. See the Pin Descriptions,* page 83 *for information on unused I/O pins*

## 3.4.7 Design Consideration

It is recommended to use a series 70Ω termination resistor on every probe connector (SDI, SDO, MODE, DCLK, PRA and PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

## 3.4.8 IEEE Standard 1149.1 Boundary Scan Test (BST) Circuitry

42MX24 and 42MX36 devices are compatible with IEEE Standard 1149.1 (informally known as Joint Testing Action Group Standard or JTAG), which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic MX boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers and instruction register (Figure 14, page 18). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and some optional instructions. Table 9, page 18 describes the ports that control JTAG testing, while Table 10, page 18 describes the test instructions supported by these MX devices.

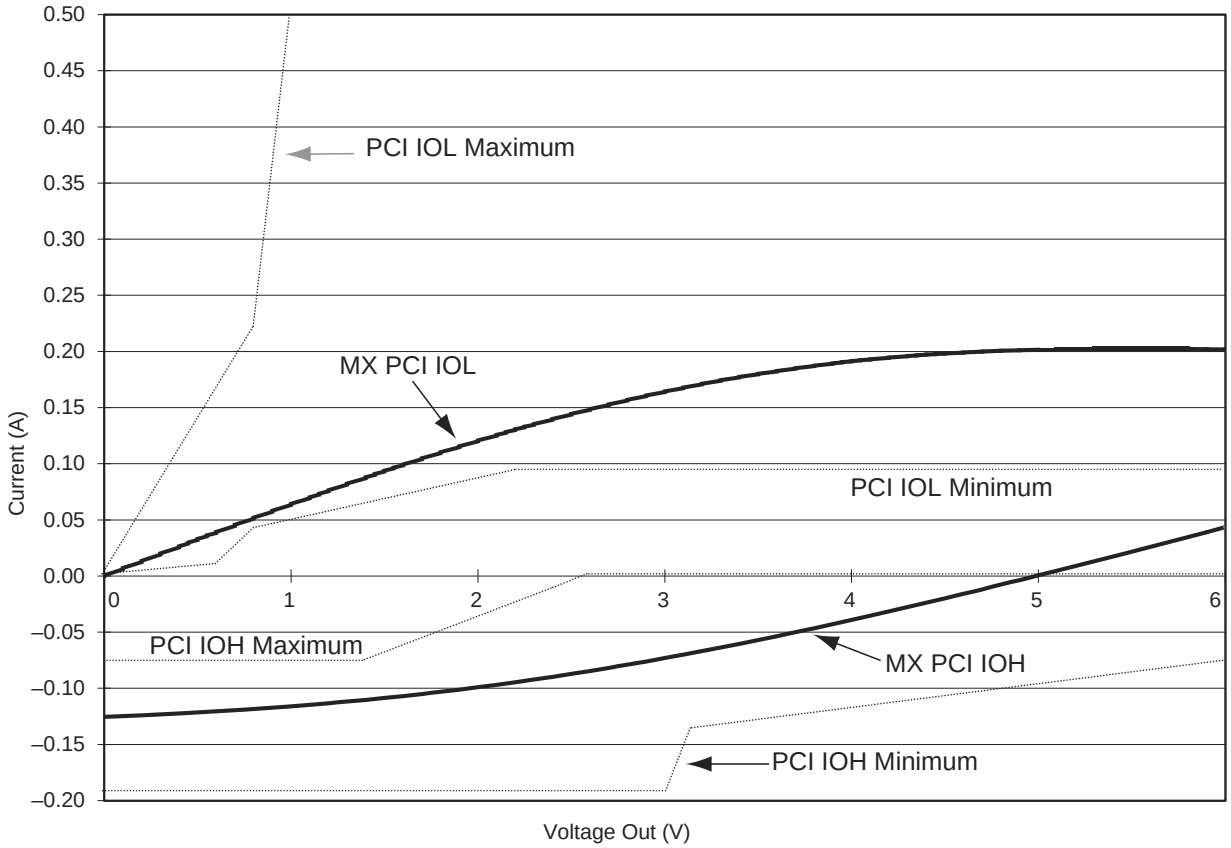
Each test section is accessed through the TAP, which has four associated pins: TCK (test clock input), TDI and TDO (test data input and output), and TMS (test mode selector).

The TAP controller is a four-bit state machine. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles.

42MX24 and 42MX36 devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

***Figure 16 •*** **Typical Output Drive Characteristics (Based Upon Measured Data)**




## 3.9.4 Junction Temperature ($T_J$)

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a \quad (1)$$

**EQ 4**

where:

- $T_a$ = Ambient Temperature
- $\Delta T$ = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$ (2)
- P = Power
- $\theta_{ja}$ = Junction to ambient of package. $\theta_{ja}$ numbers are located in Table 27, page 29.

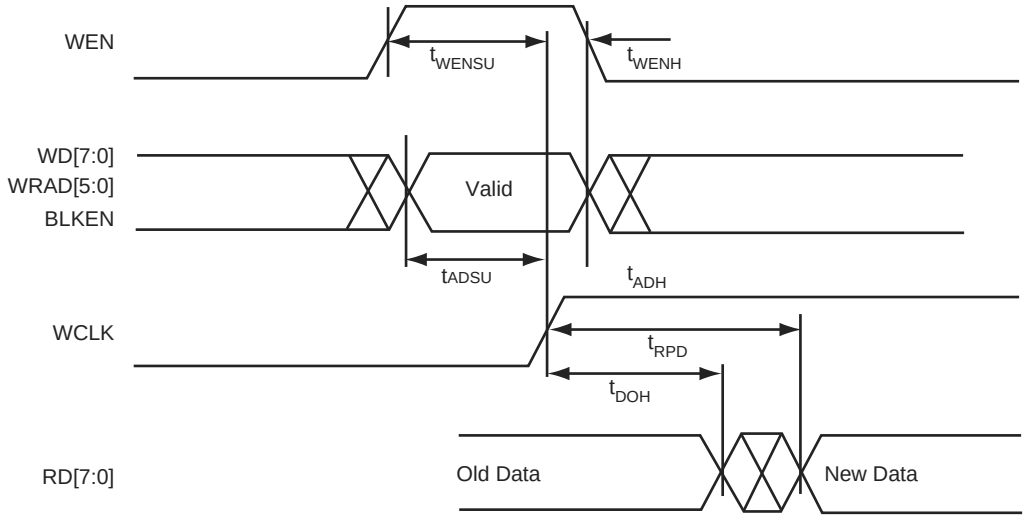
## 3.9.5 Package Thermal Characteristics

The device junction-to-case thermal characteristic is $\theta_{jc}$, and the junction-to-ambient air characteristic is $\theta_{ja}$. The thermal characteristics for $\theta_{ja}$ are shown with two different air flow rates.

The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of $\theta_{ja}$.

***Figure 33 •*** **42MX SRAM Asynchronous Read Operation—Type 2 (Write Address Controlled)**




## 3.10.7 Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution, which is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi's patented antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 µm lithography, offer nominal levels of 100 Ω resistance and 7.0 fF capacitance per antifuse.

MX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90 percent of interconnects using only two antifuses.

# 3.11 Timing Characteristics

Device timing characteristics fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all MX devices. Internal routing delays are device-dependent; actual delays are not determined until after place-and-route of the user's design is complete. Delay values may then be determined by using the Designer software utility or by performing simulation with post-layout delays.

## 3.11.1 Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment in Microsemi's Designer software prior to placement and routing. Up to 6% of the nets in a design may be designated as critical.

## 3.11.2 Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks add

***Table 34 •*** **A40MX02 Timing Characteristics (Nominal 5.0 V Operation) *(continued)***
**(Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Input Module Propagation Delays** | | | | | | | | | | | | | |
| $t_{INYH}$ | Pad-to-Y HIGH | | | 0.7 | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{INYL}$ | Pad-to-Y LOW | | | 0.6 | | 0.7 | | 0.8 | | 1.0 | | 1.3 | ns |
| **Input Module Predicted Routing Delays[1]** | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.1 | | 2.4 | | 2.2 | | 3.2 | | 4.5 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 2.6 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 3.1 | | 3.6 | | 4.1 | | 4.8 | | 6.7 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 3.6 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 5.7 | | 6.6 | | 7.5 | | 8.8 | | 12.4 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input Low to HIGH | FO = 16 | | 4.6 | | 5.3 | | 6.0 | | 7.0 | | 9.8 | ns |
| | | FO = 128 | | 4.6 | | 5.3 | | 6.0 | | 7.0 | | 9.8 | |
| $t_{CKL}$ | Input High to LOW | FO = 16 | | 4.8 | | 5.6 | | 6.3 | | 7.4 | | 10.4 | ns |
| | | FO = 128 | | 4.8 | | 5.6 | | 6.3 | | 7.4 | | 10.4 | |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 16 | 2.2 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | | ns |
| | | FO = 128 | 2.4 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | | |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 16 | 2.2 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | | ns |
| | | FO = 128 | 2.4 | | 2.7 | | 3.01 | | 3.6 | | 5.1 | | |
| $t_{CKSW}$ | Maximum Skew | FO = 16 | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| | | FO = 128 | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.2 | |
| $t_P$ | Minimum Period | FO = 16 | 4.7 | | 5.4 | | 6.1 | | 7.2 | | 10.0 | | ns |
| | | FO = 128 | 4.8 | | 5.6 | | 6.3 | | 7.5 | | 10.4 | | |
| $f_{MAX}$ | Maximum Frequency | FO = 16 | | 188 | | 175 | | 160 | | 139 | | 83 | MHz |
| | | FO = 128 | | 181 | | 168 | | 154 | | 134 | | 80 | |

***Table 36 •*** **A40MX04 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **CMOS Output Module Timing[1]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 3.9 | | 4.5 | | 5.1 | | 6.05 | | 8.5 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 4.9 | | 5.6 | | 6.4 | | 7.5 | | 10.5 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 7.9 | | 9.1 | | 10.4 | | 12.2 | | 17.0 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.9 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | ns |
| $d_{TLH}$ | Delta LOW to HIGH | | 0.03 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| $d_{THL}$ | Delta HIGH to LOW | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer utility from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading

***Table 37 •*** **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCC = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Propagation Delays** | | | | | | | | | | | | |
| $t_{PD1}$ | Single Module | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{PD2}$ | Dual-Module Macros | | 3.7 | | 4.3 | | 4.9 | | 5.7 | | 8.0 | ns |
| $t_{CO}$ | Sequential Clock-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{GO}$ | Latch G-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| **Logic Module Predicted Routing Delays[1]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 3.0 | | 4.2 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 4.1 | | 4.8 | | 5.4 | | 6.3 | | 8.9 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 7.1 | | 8.1 | | 9.2 | | 10.9 | | 15.2 | ns |
| **Logic Module Sequential Timing[2]** | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Set-Up | 4.3 | | 5.0 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_{HD}$[3] | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 4.3 | | 5.0 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |

***Table 39 •*** **A42MX09 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.9 | | 2.1 | | 2.4 | | 2.9 | | 4.0 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 3.2 | | 3.6 | | 4.1 | | 4.8 | | 6.7 | ns |
| **Logic Module Sequential Timing [3, 4]** | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Set-Up | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 0.9 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 1.2 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.8 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 6.2 | | 6.9 | | 7.8 | | 9.2 | | 12.9 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 5.0 | | 5.6 | | 6.2 | | 7.1 | | 9.9 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Buffer Latch Set-Up | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTSU}$ | Output Buffer Latch Set-Up | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 161 | | 146 | | 135 | | 117 | | 70 | MHz |

***Table 40 •*** **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **CMOS Output Module Timing[5]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 3.2 | | 3.6 | | 4.0 | | 4.7 | | 6.6 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 2.5 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 2.7 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 3.0 | | 3.3 | | 3.8 | | 4.4 | | 6.2 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 5.4 | | 6.0 | | 6.8 | | 8.0 | | 11.2 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.0 | | 5.6 | | 6.3 | | 7.4 | | 10.4 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | 5.1 | | 5.6 | | 6.4 | | 7.5 | | 10.5 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | 5.1 | | 5.6 | | 6.4 | | 7.5 | | 10.5 | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 5.7 | | 6.3 | | 7.1 | | 8.4 | | 11.9 | ns |
| $t_{ACO}$ | Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 8.0 | | 8.9 | | 10.1 | | 11.9 | | 16.7 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.06 | ns/pF |

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, point and position whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

***Table 41 •*** **A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Logic Module Propagation Delays[1]** | | | | | | | | | | | | |
| $t_{PD1}$ | Single Module | | 1.9 | | 2.1 | | 2.4 | | 2.8 | | 4.0 | ns |
| $t_{CO}$ | Sequential Clock-to-Q | | 2.0 | | 2.2 | | 2.5 | | 3.0 | | 4.2 | ns |
| $t_{GO}$ | Latch G-to-Q | | 1.9 | | 2.1 | | 2.4 | | 2.8 | | 4.0 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset-to-Q | | 2.2 | | 2.4 | | 2.8 | | 3.3 | | 4.6 | ns |
| **Logic Module Predicted Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 1.1 | | 1.2 | | 1.4 | | 1.6 | | 2.3 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.5 | | 1.6 | | 1.8 | | 2.1 | | 3.0 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 3.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 2.2 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.5 | ns |

***Table 44 •*** **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Combinatorial Functions[1]** | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module Delay | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{PDD}$ | Internal Decode Module Delay | | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.3 | ns |
| **Logic Module Predicted Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{RD3}$ | FO =3 Routing Delay | | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.4 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{RD5}$ | FO = 8 Routing Delay | | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | ns |
| $t_{RDD}$ | Decode-to-Output Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| **Logic Module Sequential Timing[3, 4]** | | | | | | | | | | | | |
| $t_{CO}$ | Flip-Flop Clock-to-Output | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{GO}$ | Latch Gate-to-Output | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{SUD}$ | Flip-Flop (Latch) Set-Up Time | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RO}$ | Flip-Flop (Latch) Reset-to-Output | | 1.6 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.4 | | 4.8 | | 5.5 | | 6.4 | | 9.0 | | ns |
| **Synchronous SRAM Operations** | | | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 6.8 | | 7.5 | | 8.5 | | 10.0 | | 14.0 | | ns |
| $t_{WC}$ | Write Cycle Time | 6.8 | | 7.5 | | 8.5 | | 10.0 | | 14.0 | | ns |
| $t_{RCKHL}$ | Clock HIGH/LOW Time | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | | ns |
| $t_{RCO}$ | Data Valid After Clock HIGH/LOW | | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | ns |
| $t_{ADSU}$ | Address/Data Set-Up Time | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.4 | | ns |
| **Synchronous SRAM Operations (continued)** | | | | | | | | | | | | |
| $t_{ADH}$ | Address/Data Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RENSU}$ | Read Enable Set-Up | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | | ns |
| $t_{RENH}$ | Read Enable Hold | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | | ns |
| $t_{WENSU}$ | Write Enable Set-Up | 2.7 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | | ns |
| $t_{WENH}$ | Write Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{BENS}$ | Block Enable Set-Up | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | | ns |
| $t_{BENH}$ | Block Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |

***Table 44 •*** **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Asynchronous SRAM Operations** | | | | | | | | | | | | | |
| $t_{RPD}$ | Asynchronous Access Time | | | 8.1 | | 9.0 | | 10.2 | | 12.0 | | 16.8 | ns |
| $t_{RDADV}$ | Read Address Valid | | 8.8 | | 9.8 | | 11.1 | | 13.0 | | 18.2 | | ns |
| $t_{ADSU}$ | Address/Data Set-Up Time | | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.4 | | ns |
| $t_{ADH}$ | Address/Data Hold Time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RENSUA}$ | Read Enable Set-Up to Address Valid | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | | ns |
| $t_{RENHA}$ | Read Enable Hold | | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | | ns |
| $t_{WENSU}$ | Write Enable Set-Up | | 2.7 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | | ns |
| $t_{WENH}$ | Write Enable Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{DOH}$ | Data Out Hold Time | | | 1.2 | | 1.3 | | 1.5 | | 1.8 | | 2.5 | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | | |
| $t_{INPY}$ | Input Data Pad-to-Y | | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{INGO}$ | Input Latch Gate-to-Output | | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| $t_{INH}$ | Input Latch Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Latch Set-Up | | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{ILA}$ | Latch Active Pulse Width | | 4.7 | | 5.2 | | 5.9 | | 6.9 | | 9.7 | | ns |
| **Input Module Predicted Routing Delays[2]** | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 2.3 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 2.6 | | 2.9 | | 3.3 | | 3.9 | | 5.5 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 3.0 | | 3.3 | | 3.8 | | 4.4 | | 6.2 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 4.3 | | 4.8 | | 5.5 | | 6.4 | | 9.0 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 32 | | 2.7 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| | | FO = 635 | | 3.0 | | 3.3 | | 3.8 | | 4.4 | | 6.2 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 32 | | 3.8 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | ns |
| | | FO = 635 | | 4.9 | | 5.4 | | 6.1 | | 7.2 | | 10.1 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 32 | 1.8 | | 2.0 | | 2.2 | | 2.6 | | 3.6 | | ns |
| | | FO = 635 | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | | ns |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 1.8 | | 2.0 | | 2.2 | | 2.6 | | 3.6 | | ns |
| | | FO = 635 | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 0.8 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| | | FO = 635 | | 0.8 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |

***Table 45 •*** **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| $t_{ACO}$ | Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | 10.9 | | 12.1 | | 13.7 | | 16.1 | | 22.5 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | 0.10 | | 0.11 | | 0.12 | | 0.14 | | 0.20 | ns/pF |
| $d_{THL}$ | Capacitive Loading, HIGH to LOW | | 0.10 | | 0.11 | | 0.12 | | 0.14 | | 0.20 | ns/pF |
| **CMOS Output Module Timing[5]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 4.9 | | 5.5 | | 6.2 | | 7.3 | | 10.3 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 3.4 | | 3.8 | | 4.3 | | 5.1 | | 7.1 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 7.7 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 4.1 | | 4.6 | | 5.2 | | 6.1 | | 8.5 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 7.4 | | 8.2 | | 9.3 | | 10.9 | | 15.3 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 6.9 | | 7.6 | | 8.7 | | 10.2 | | 14.3 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | 7.0 | | 7.8 | | 8.9 | | 10.4 | | 14.6 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | 7.0 | | 7.8 | | 8.9 | | 10.4 | | 14.6 | ns |
| $t_{LSU}$ | I/O Latch Set-Up | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{LH}$ | I/O Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | 7.9 | | 8.8 | | 10.0 | | 11.8 | | 16.5 | ns |

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. Delays based on 35 pF loading.

# 3.12 Pin Descriptions

This section lists the pin descriptions for 40MX and 42MX series FPGAs.

**CLK/A/B, I/O Global Clock**

Clock inputs for clock distribution networks. CLK is for 40MX while CLKA and CLKB are for 42MX devices. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**DCLK, I/ODiagnostic Clock**

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**GND, Ground**

Input LOW supply voltage.

**I/O, Input/Output**

***Table 50 •*** **PQ 100**

| **PQ100** | | | | |
|---|---|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** | **A42MX09 Function** | **A42MX16 Function** |
| 56 | VCC | VCC | I/O | I/O |
| 57 | I/O | I/O | GND | GND |
| 58 | I/O | I/O | I/O | I/O |
| 59 | I/O | I/O | I/O | I/O |
| 60 | I/O | I/O | I/O | I/O |
| 61 | I/O | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O | I/O |
| 63 | GND | GND | I/O | I/O |
| 64 | I/O | I/O | LP | LP |
| 65 | I/O | I/O | VCCA | VCCA |
| 66 | I/O | I/O | VCCI | VCCI |
| 67 | I/O | I/O | VCCA | VCCA |
| 68 | I/O | I/O | I/O | I/O |
| 69 | VCC | VCC | I/O | I/O |
| 70 | I/O | I/O | I/O | I/O |
| 71 | I/O | I/O | I/O | I/O |
| 72 | I/O | I/O | GND | GND |
| 73 | I/O | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O | I/O |
| 77 | NC | NC | I/O | I/O |
| 78 | NC | NC | I/O | I/O |
| 79 | NC | NC | SDI, I/O | SDI, I/O |
| 80 | NC | I/O | I/O | I/O |
| 81 | NC | I/O | I/O | I/O |
| 82 | NC | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O | I/O |
| 84 | I/O | I/O | GND | GND |
| 85 | I/O | I/O | I/O | I/O |
| 86 | GND | GND | I/O | I/O |
| 87 | GND | GND | PRA, I/O | PRA, I/O |
| 88 | I/O | I/O | I/O | I/O |
| 89 | I/O | I/O | CLKA, I/O | CLKA, I/O |
| 90 | CLK, I/O | CLK, I/O | VCCA | VCCA |
| 91 | I/O | I/O | I/O | I/O |
| 92 | MODE | MODE | CLKB, I/O | CLKB, I/O |

***Table 56 •*** **VQ100**

| **VQ100** | | |
|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** |
| 21 | I/O | I/O |
| 22 | I/O | I/O |
| 23 | I/O | I/O |
| 24 | I/O | I/O |
| 25 | I/O | I/O |
| 26 | I/O | I/O |
| 27 | I/O | I/O |
| 28 | I/O | I/O |
| 29 | I/O | I/O |
| 30 | I/O | I/O |
| 31 | I/O | I/O |
| 32 | GND | GND |
| 33 | I/O | I/O |
| 34 | I/O | I/O |
| 35 | I/O | I/O |
| 36 | I/O | I/O |
| 37 | I/O | I/O |
| 38 | VCCA | VCCA |
| 39 | I/O | I/O |
| 40 | I/O | I/O |
| 41 | I/O | I/O |
| 42 | I/O | I/O |
| 43 | I/O | I/O |
| 44 | GND | GND |
| 45 | I/O | I/O |
| 46 | I/O | I/O |
| 47 | I/O | I/O |
| 48 | I/O | I/O |
| 49 | I/O | I/O |
| 50 | SDO, I/O | SDO, I/O |
| 51 | I/O | I/O |
| 52 | I/O | I/O |
| 53 | I/O | I/O |
| 54 | I/O | I/O |
| 55 | GND | GND |
| 56 | I/O | I/O |

***Table 58 •*** **CQ208**

| **CQ208** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 1 | GND |
| 2 | VCCA |
| 3 | MODE |
| 4 | I/O |
| 5 | I/O |
| 6 | I/O |
| 7 | I/O |
| 8 | I/O |
| 9 | I/O |
| 10 | I/O |
| 11 | I/O |
| 12 | I/O |
| 13 | I/O |
| 14 | I/O |
| 15 | I/O |
| 16 | I/O |
| 17 | VCCA |
| 18 | I/O |
| 19 | I/O |
| 20 | I/O |
| 21 | I/O |
| 22 | GND |
| 23 | I/O |
| 24 | I/O |
| 25 | I/O |
| 26 | I/O |
| 27 | GND |
| 28 | VCCI |
| 29 | VCCA |
| 30 | I/O |
| 31 | I/O |
| 32 | VCCA |
| 33 | I/O |
| 34 | I/O |
| 35 | I/O |
| 36 | I/O |

***Figure 50 •*** **CQ256**

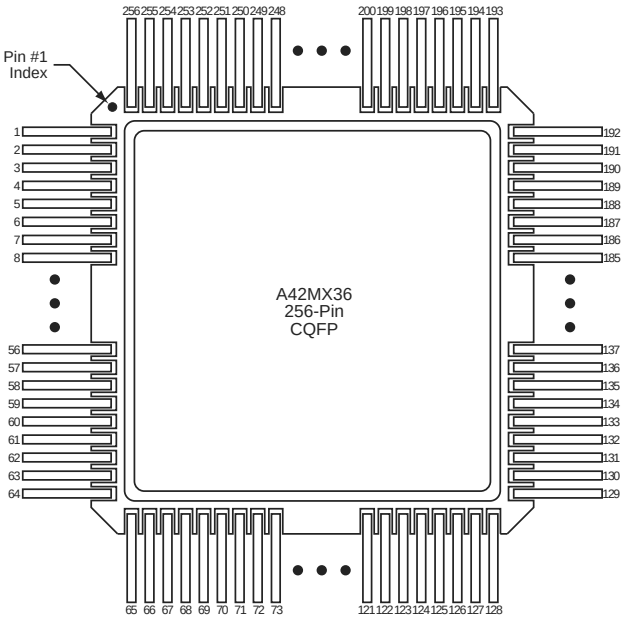



***Table 59 •*** **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 1 | NC |
| 2 | GND |
| 3 | I/O |
| 4 | I/O |
| 5 | I/O |
| 6 | I/O |
| 7 | I/O |
| 8 | I/O |
| 9 | I/O |
| 10 | GND |
| 11 | I/O |
| 12 | I/O |
| 13 | I/O |
| 14 | I/O |
| 15 | I/O |
| 16 | I/O |
| 17 | I/O |
| 18 | I/O |
| 19 | I/O |
| 20 | I/O |
| 21 | I/O |

***Table 59 •*** **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 170 | VCCA |
| 171 | I/O |
| 172 | I/O |
| 173 | I/O |
| 174 | I/O |
| 175 | I/O |
| 176 | I/O |
| 177 | I/O |
| 178 | I/O |
| 179 | I/O |
| 180 | GND |
| 181 | I/O |
| 182 | I/O |
| 183 | I/O |
| 184 | I/O |
| 185 | I/O |
| 186 | I/O |
| 187 | I/O |
| 188 | MODE |
| 189 | VCCA |
| 190 | GND |
| 191 | NC |
| 192 | NC |
| 193 | NC |
| 194 | I/O |
| 195 | DCLK, I/O |
| 196 | I/O |
| 197 | I/O |
| 198 | I/O |
| 199 | WD, I/O |
| 200 | WD, I/O |
| 201 | VCCI |
| 202 | I/O |
| 203 | I/O |
| 204 | I/O |
| 205 | I/O |
| 206 | GND |

***Table 59 •*** **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 244 | WD, I/O |
| 245 | I/O |
| 246 | I/O |
| 247 | I/O |
| 248 | VCCI |
| 249 | I/O |
| 250 | WD, I/O |
| 251 | WD, I/O |
| 252 | I/O |
| 253 | SDI, I/O |
| 254 | I/O |
| 255 | GND |
| 256 | NC |

***Figure 51 •*** **BG272**

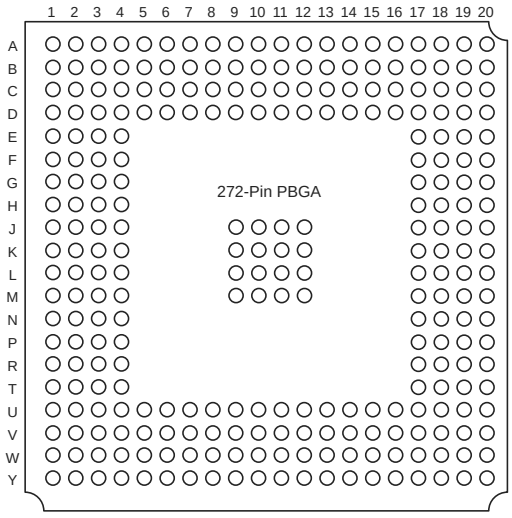



***Table 60 •*** **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| A1 | GND |
| A2 | GND |
| A3 | I/O |
| A4 | WD, I/O |
| A5 | I/O |

***Table 60 •*** **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| A6 | I/O |
| A7 | WD, I/O |
| A8 | WD, I/O |
| A9 | I/O |
| A10 | I/O |
| A11 | CLKA |
| A12 | I/O |
| A13 | I/O |
| A14 | I/O |
| A15 | I/O |
| A16 | WD, I/O |
| A17 | I/O |
| A18 | I/O |
| A19 | GND |
| A20 | GND |
| B1 | GND |
| B2 | GND |
| B3 | DCLK, I/O |
| B4 | I/O |
| B5 | I/O |
| B6 | I/O |
| B7 | WD, I/O |
| B8 | I/O |
| B9 | PRB, I/O |
| B10 | I/O |
| B11 | I/O |
| B12 | WD, I/O |
| B13 | I/O |
| B14 | I/O |
| B15 | WD, I/O |
| B16 | I/O |
| B17 | WD, I/O |
| B18 | I/O |
| B19 | GND |
| B20 | GND |
| C1 | I/O |
| C2 | MODE |

***Table 60 •*** **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| C3 | GND |
| C4 | I/O |
| C5 | WD, I/O |
| C6 | I/O |
| C7 | QCLKC, I/O |
| C8 | I/O |
| C9 | I/O |
| C10 | CLKB |
| C11 | PRA, I/O |
| C12 | WD, I/O |
| C13 | I/O |
| C14 | QCLKD, I/O |
| C15 | I/O |
| C16 | WD, I/O |
| C17 | SDI, I/O |
| C18 | I/O |
| C19 | I/O |
| C20 | I/O |
| D1 | I/O |
| D2 | I/O |
| D3 | I/O |
| D4 | I/O |
| D5 | VCCI |
| D6 | I/O |
| D7 | I/O |
| D8 | VCCA |
| D9 | WD, I/O |
| D10 | VCCI |
| D11 | I/O |
| D12 | VCCI |
| D13 | I/O |
| D14 | VCCI |
| D15 | I/O |
| D16 | VCCA |
| D17 | GND |
| D18 | I/O |
| D19 | I/O |

***Table 60 •*** **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| D20 | I/O |
| E1 | I/O |
| E2 | I/O |
| E3 | I/O |
| E4 | VCCA |
| E17 | VCCI |
| E18 | I/O |
| E19 | I/O |
| E20 | I/O |
| F1 | I/O |
| F2 | I/O |
| F3 | I/O |
| F4 | VCCI |
| F17 | I/O |
| F18 | I/O |
| F19 | I/O |
| F20 | I/O |
| G1 | I/O |
| G2 | I/O |
| G3 | I/O |
| G4 | VCCI |
| G17 | VCCI |
| G18 | I/O |
| G19 | I/O |
| G20 | I/O |
| H1 | I/O |
| H2 | I/O |
| H3 | I/O |
| H4 | VCCA |
| H17 | I/O |
| H18 | I/O |
| H19 | I/O |
| H20 | I/O |
| J1 | I/O |
| J2 | I/O |
| J3 | I/O |
| J4 | VCCI |

***Table 61 •*** **PG132**

| **PG132** | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| N10 | I/O |
| M10 | I/O |
| N11 | I/O |
| L10 | I/O |
| M11 | I/O |
| N12 | SDO |
| M12 | I/O |
| L11 | I/O |
| N13 | I/O |
| M13 | I/O |
| K11 | I/O |
| L12 | I/O |
| L13 | I/O |
| K13 | I/O |
| H10 | I/O |
| J12 | I/O |
| J13 | I/O |
| H11 | I/O |
| H12 | I/O |
| H13 | VKS |
| G13 | VPP |