Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	83
Number of Gates	14000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx09-2pqg100

Contents

A sample calculation of the absolute maximum power dissipation allowed for a TQ176 package at commercial temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (°\text{C})}{\theta_{ja}(°(\text{C}/\text{W}))} = \frac{150°\text{C} - 70°\text{C}}{(28°\text{C})/\text{W}} = 2.86\text{W}$$

EQ 5

The maximum power dissipation for military-grade devices is a function of θ_{jc}. A sample calculation of the absolute maximum power dissipation allowed for CQFP 208-pin package at military temperature and still air is given in the following equation

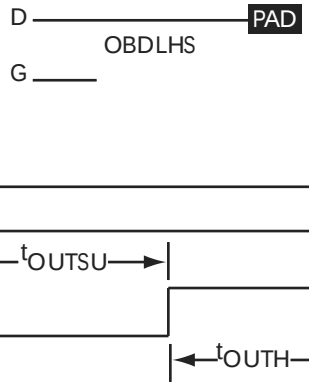
$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (°\text{C})}{\theta_{jc}(°(\text{C}/\text{W}))} = \frac{150°\text{C} - 125°\text{C}}{(6.3°\text{C})/\text{W}} = 3.97\text{W}$$

EQ 6

Table 27 • **Package Thermal Characteristics**

			θ_{ja}			
Plastic Packages	**Pin Count**	θ_{jc}	**Still Air**	**1.0 m/s 200 ft/min.**	**2.5 m/s 500 ft/min.**	**Units**
Plastic Quad Flat Pack	100	12.0	27.8	23.4	21.2	°C/W
Plastic Quad Flat Pack	144	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	160	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	208	8.0	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack	240	8.5	25.6	22.3	20.8	°C/W
Plastic Leaded Chip Carrier	44	16.0	20.0	24.5	22.0	°C/W
Plastic Leaded Chip Carrier	68	13.0	25.0	21.0	19.4	°C/W
Plastic Leaded Chip Carrier	84	12.0	22.5	18.9	17.6	°C/W
Thin Plastic Quad Flat Pack	176	11.0	24.7	19.9	18.0	°C/W
Very Thin Plastic Quad Flat Pack	80	12.0	38.2	31.9	29.4	°C/W
Very Thin Plastic Quad Flat Pack	100	10.0	35.3	29.4	27.1	°C/W
Plastic Ball Grid Array	272	3.0	18.3	14.9	13.9	°C/W
Ceramic Packages						
Ceramic Pin Grid Array	132	4.8	25.0	20.6	18.7	°C/W
Ceramic Quad Flat Pack	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack	256	2.0	20.0	16.5	15.0	°C/W

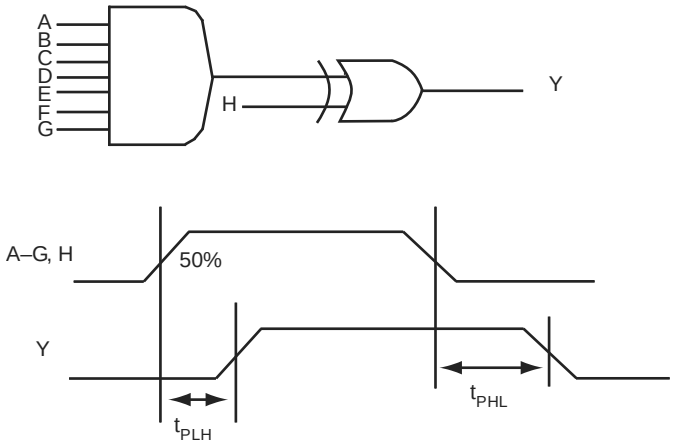
Figure 27 • **Output Buffer Latches**



3.10.4 Decode Module Timing

The following figure shows decode module timing.

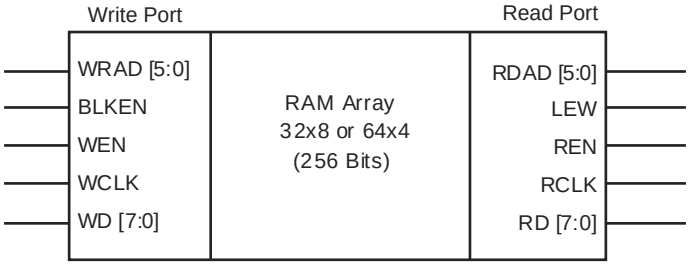
Figure 28 • **Decode Module Timing**



3.10.5 SRAM Timing Characteristics

The following figure shows SRAM timing characteristics.

Figure 29 • **SRAM Timing Characteristics**



3.10.6 Dual-Port SRAM Timing Waveforms

The following figures show dual-port SRAM timing waveforms.

Table 34 • **A40MX02 Timing Characteristics (Nominal 5.0 V Operation) *(continued)***
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			0.7		0.8		0.9		1.1		1.5	ns
t_{INYL}	Pad-to-Y LOW			0.6		0.7		0.8		1.0		1.3	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO = 1 Routing Delay			2.1		2.4		2.2		3.2		4.5	ns
t_{IRD2}	FO = 2 Routing Delay			2.6		3.0		3.4		4.0		5.6	ns
t_{IRD3}	FO = 3 Routing Delay			3.1		3.6		4.1		4.8		6.7	ns
t_{IRD4}	FO = 4 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t_{IRD8}	FO = 8 Routing Delay			5.7		6.6		7.5		8.8		12.4	ns
Global Clock Network													
t_{CKH}	Input Low to HIGH	FO = 16		4.6		5.3		6.0		7.0		9.8	ns
		FO = 128		4.6		5.3		6.0		7.0		9.8	
t_{CKL}	Input High to LOW	FO = 16		4.8		5.6		6.3		7.4		10.4	ns
		FO = 128		4.8		5.6		6.3		7.4		10.4	
t_{PWH}	Minimum Pulse Width HIGH	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.1		3.6		5.1		
t_{PWL}	Minimum Pulse Width LOW	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.01		3.6		5.1		
t_{CKSW}	Maximum Skew	FO = 16		0.4		0.5		0.5		0.6		0.8	ns
		FO = 128		0.5		0.6		0.7		0.8		1.2	
t_P	Minimum Period	FO = 16	4.7		5.4		6.1		7.2		10.0		ns
		FO = 128	4.8		5.6		6.3		7.5		10.4		
f_{MAX}	Maximum Frequency	FO = 16		188		175		160		139		83	MHz
		FO = 128		181		168		154		134		80	

Table 36 • **A40MX04 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[1]												
t_{DLH}	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t_{DHL}	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZH}	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZL}	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t_{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer utility from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading

Table 37 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t_{PD1}	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t_{PD2}	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t_{CO}	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t_{GO}	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays[1]												
t_{RD1}	FO = 1 Routing Delay		1.9		2.2		2.5		3.0		4.2	ns
t_{RD2}	FO = 2 Routing Delay		2.7		3.1		3.5		4.1		5.7	ns
t_{RD3}	FO = 3 Routing Delay		3.4		3.9		4.4		5.2		7.3	ns
t_{RD4}	FO = 4 Routing Delay		4.1		4.8		5.4		6.3		8.9	ns
t_{RD8}	FO = 8 Routing Delay		7.1		8.1		9.2		10.9		15.2	ns
Logic Module Sequential Timing[2]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	4.3		5.0		5.6		6.6		9.2		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	4.3		5.0		5.6		6.6		9.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns

Table 37 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays1													
t_{IRD1}	FO = 1 Routing Delay			2.9		3.3		3.8		4.5		6.3	ns
t_{IRD2}	FO = 2 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t_{IRD3}	FO = 3 Routing Delay			4.4		5.0		5.7		6.7		9.4	ns
t_{IRD4}	FO = 4 Routing Delay			5.1		5.9		6.7		7.8		11.0	ns
t_{IRD8}	FO = 8 Routing Delay			8.0		9.3		10.5		12.4		17.2	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 16		6.4		7.4		8.4		9.9		13.8	ns
		FO = 128		6.4		7.4		8.4		9.9		13.8	
t_{CKL}	Input HIGH to LOW	FO = 16		6.8		7.8		8.9		10.4		14.6	ns
		FO = 128		6.8		7.8		8.9		10.4		14.6	
t_{PWH}	Minimum Pulse Width HIGH	FO = 16	3.1		3.6		4.1		4.8		6.7		ns
		FO = 128	3.3		3.8		4.3		5.1		7.1		
t_{PWL}	Minimum Pulse Width LOW	FO = 16	3.1		3.6		4.1		4.8		6.7		ns
		FO = 128	3.3		3.8		4.3		5.1		7.1		
t_{CKSW}	Maximum Skew	FO = 16		0.6		0.6		0.7		0.8		1.2	ns
		FO = 128		0.8		0.9		1.0		1.2		1.6	
t_P	Minimum Period	FO = 16	6.5		7.5		8.5		10.1		14.1		ns
		FO = 128	6.8		7.8		8.9		10.4		14.6		
f_{MAX}	Maximum Frequency	FO = 16		113		105		96		83		50	MHz
		FO = 128		109		101		92		80		48	
TTL Output Module Timing[4]													
t_{DLH}	Data-to-Pad HIGH			4.7		5.4		6.1		7.2		10.0	ns
t_{DHL}	Data-to-Pad LOW			5.6		6.4		7.3		8.6		12.0	ns
t_{ENZH}	Enable Pad Z to HIGH			5.2		6.0		6.9		8.1		11.3	ns
t_{ENZL}	Enable Pad Z to LOW			6.6		7.6		8.6		10.1		14.1	ns
t_{ENHZ}	Enable Pad HIGH to Z			11.1		12.8		14.5		17.1		23.9	ns
t_{ENLZ}	Enable Pad LOW to Z			8.2		9.5		10.7		12.6		17.7	ns
d_{TLH}	Delta LOW to HIGH			0.03		0.03		0.04		0.04		0.06	ns/pF
d_{THL}	Delta HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF

Table 39 • **A42MX09 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		3.4		3.8		5.5		6.4		9.0	ns
t_{DHL}	Data-to-Pad LOW		4.1		4.5		4.2		5.0		7.0	ns
t_{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t_{ENZL}	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t_{ENLZ}	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t_{GLH}	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t_{GHL}	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t_{LSU}	I/O Latch Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. *Delays based on 35 pF loading.*

Table 40 • **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays[1]												
t_{PD1}	Single Module		1.4		1.5		1.7		2.0		2.8	ns
t_{CO}	Sequential Clock-to-Q		1.4		1.6		1.8		2.1		3.0	ns
t_{GO}	Latch G-to-Q		1.4		1.5		1.7		2.0		2.8	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.6		1.7		2.0		2.3		3.3	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.8		0.9		1.0		1.2		1.6	ns
t_{RD2}	FO = 2 Routing Delay		1.0		1.2		1.3		1.5		2.1	ns

Table 42 • **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		3.1		3.5		3.9		4.6		6.4	ns
t_{DHL}	Data-to-Pad LOW		2.4		2.6		3.0		3.5		4.9	ns
t_{ENZH}	Enable Pad Z to HIGH		2.5		2.8		3.2		3.8		5.3	ns
t_{ENZL}	Enable Pad Z to LOW		2.8		3.1		3.5		4.2		5.8	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.2		5.7		6.5		7.6		10.7	ns
t_{ENLZ}	Enable Pad LOW to Z		4.8		5.3		6.0		7.1		9.9	ns
t_{GLH}	G-to-Pad HIGH		4.9		5.4		6.2		7.2		10.1	ns
t_{GHL}	G-to-Pad LOW		4.9		5.4		6.2		7.2		10.1	ns
t_{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.5		6.1		6.9		8.1		11.3	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.6		11.8		13.4		15.7		22.0	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. D*ata applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

Table 43 • **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Combinatorial Functions[1]												
t_{PD}	Internal Array Module Delay		2.0		1.8		2.1		2.5		3.4	ns
t_{PDD}	Internal Decode Module Delay		1.1		2.2		2.5		3.0		4.2	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		1.7		1.3		1.4		1.7		2.3	ns
t_{RD2}	FO = 2 Routing Delay		2.0		1.6		1.8		2.1		3.0	ns
t_{RD3}	FO = 3 Routing Delay		1.1		2.0		2.2		2.6		3.7	ns
t_{RD4}	FO = 4 Routing Delay		1.5		2.3		2.6		3.1		4.3	ns
t_{RD5}	FO = 8 Routing Delay		1.8		3.7		4.2		5.0		7.0	ns

Table 45 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RD5}	FO = 8 Routing Delay		4.6		5.2		5.8		6.9		9.6	ns
t_{RDD}	Decode-to-Output Routing Delay		0.5		0.5		0.6		0.7		1.0	ns
Logic Module Sequential Timing[3, 4]												
t_{CO}	Flip-Flop Clock-to-Output		1.8		2.0		2.3		2.7		3.7	ns
t_{GO}	Latch Gate-to-Output		1.8		2.0		2.3		2.7		3.7	ns
t_{SUD}	Flip-Flop (Latch) Set-Up Time	0.4		0.5		0.6		0.7		0.9		ns
t_{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		2.2		2.4		2.7		3.2		4.5	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	1.0		1.1		1.2		1.4		2.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.2		5.8		6.9		9.6		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.1		6.8		7.7		9.0		12.6		ns
Synchronous SRAM Operations												
t_{RC}	Read Cycle Time	9.5		10.5		11.9		14.0		19.6		ns
t_{WC}	Write Cycle Time	9.5		10.5		11.9		14.0		19.6		ns
t_{RCKHL}	Clock HIGH/LOW Time	4.8		5.3		6.0		7.0		9.8		ns
t_{RCO}	Data Valid After Clock HIGH/LOW		4.8		5.3		6.0		7.0		9.8	ns
t_{ADSU}	Address/Data Set-Up Time	2.3		2.5		2.8		3.4		4.8		ns

Table 50 • **PQ 100**

PQ100				
Pin Number	**A40MX02 Function**	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**
56	VCC	VCC	I/O	I/O
57	I/O	I/O	GND	GND
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	I/O	I/O	I/O	I/O
61	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	GND	GND	I/O	I/O
64	I/O	I/O	LP	LP
65	I/O	I/O	VCCA	VCCA
66	I/O	I/O	VCCI	VCCI
67	I/O	I/O	VCCA	VCCA
68	I/O	I/O	I/O	I/O
69	VCC	VCC	I/O	I/O
70	I/O	I/O	I/O	I/O
71	I/O	I/O	I/O	I/O
72	I/O	I/O	GND	GND
73	I/O	I/O	I/O	I/O
74	I/O	I/O	I/O	I/O
75	I/O	I/O	I/O	I/O
76	I/O	I/O	I/O	I/O
77	NC	NC	I/O	I/O
78	NC	NC	I/O	I/O
79	NC	NC	SDI, I/O	SDI, I/O
80	NC	I/O	I/O	I/O
81	NC	I/O	I/O	I/O
82	NC	I/O	I/O	I/O
83	I/O	I/O	I/O	I/O
84	I/O	I/O	GND	GND
85	I/O	I/O	I/O	I/O
86	GND	GND	I/O	I/O
87	GND	GND	PRA, I/O	PRA, I/O
88	I/O	I/O	I/O	I/O
89	I/O	I/O	CLKA, I/O	CLKA, I/O
90	CLK, I/O	CLK, I/O	VCCA	VCCA
91	I/O	I/O	I/O	I/O
92	MODE	MODE	CLKB, I/O	CLKB, I/O

Table 53 • **PQ208**

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
95	NC	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	VCCI	VCCI	VCCI
99	I/O	I/O	I/O
100	I/O	WD, I/O	WD, I/O
101	I/O	WD, I/O	WD, I/O
102	I/O	I/O	I/O
103	SDO, I/O	SDO, TDO, I/O	SDO, TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	VCCA	VCCA
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	NC	I/O	I/O
113	NC	I/O	I/O
114	NC	I/O	I/O
115	NC	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	I/O	I/O	I/O
126	GND	GND	GND
127	I/O	I/O	I/O
128	I/O	TCK, I/O	TCK, I/O
129	LP	LP	LP
130	VCCA	VCCA	VCCA
131	GND	GND	GND

Table 55 • **VQ80**

VQ80		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
49	I/O	I/O
50	CLK, I/O	CLK, I/O
51	I/O	I/O
52	MODE	MODE
53	VCC	VCC
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	GND	GND
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	VCC	**VCC**
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O

Table 56 • **VQ100**

VQ100		
Pin Number	**A42MX09 Function**	**A42MX16 Function**
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	LP	LP
63	VCCA	VCCA
64	VCCI	VCCI
65	VCCA	VCCA
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	GND	GND
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	SDI, I/O	SDI, I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	GND	GND
83	I/O	I/O
84	I/O	I/O
85	PRA, I/O	PRA, I/O
86	I/O	I/O
87	CLKA, I/O	CLKA, I/O
88	VCCA	VCCA
89	I/O	I/O
90	CLKB, I/O	CLKB, I/O
91	I/O	I/O
92	PRB, I/O	PRB, I/O

Table 57 • **TQ176**

TQ176			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
158	CLKB, I/O	CLKB, I/O	CLKB, I/O
159	I/O	I/O	I/O
160	PRB, I/O	PRB, I/O	PRB, I/O
161	NC	I/O	WD, I/O
162	I/O	I/O	WD, I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	NC	NC	WD, I/O
166	NC	I/O	WD, I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	I/O	I/O	I/O
170	NC	VCCI	VCCI
171	I/O	I/O	WD, I/O
172	I/O	I/O	WD, I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	DCLK, I/O	DCLK, I/O	DCLK, I/O
176	I/O	I/O	I/O

Figure 49 • **CQ208**

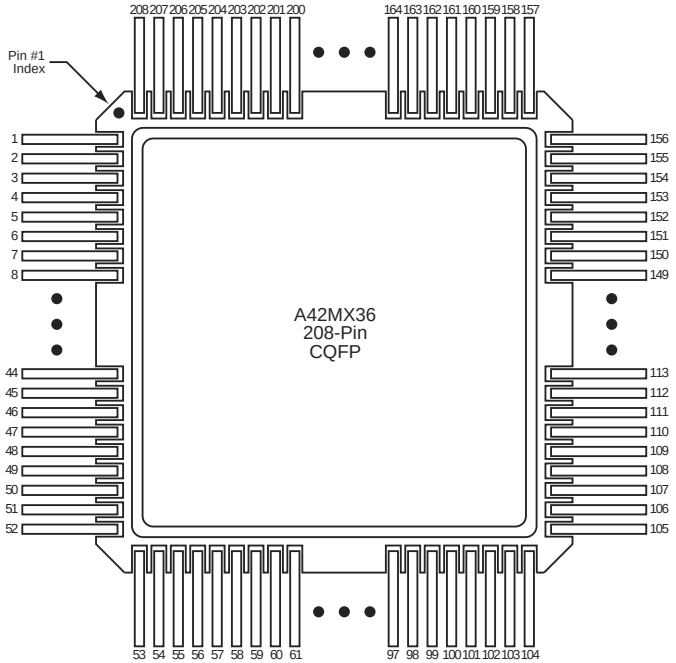


Table 58 • **CQ208**

CQ208	
Pin Number	**A42MX36 Function**
1	GND
2	VCCA
3	MODE
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	VCCA
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	VCCI
29	VCCA
30	I/O
31	I/O
32	VCCA
33	I/O
34	I/O
35	I/O
36	I/O

Figure 50 • **CQ256**

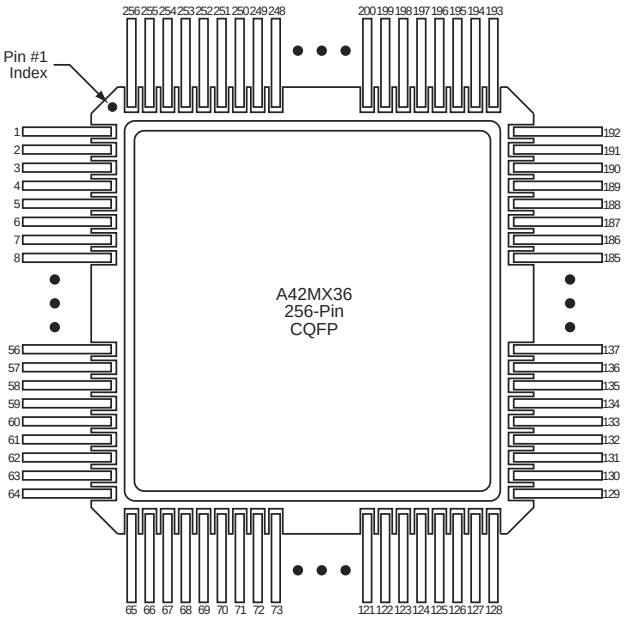


Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
1	NC
2	GND
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	GND
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
59	I/O
60	VCCA
61	GND
62	GND
63	NC
64	NC
65	NC
66	I/O
67	SDO, TDO, I/O
68	I/O
69	WD, I/O
70	WD, I/O
71	I/O
72	VCCI
73	I/O
74	I/O
75	I/O
76	WD, I/O
77	GND
78	WD, I/O
79	I/O
80	QCLKB, I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	WD, I/O
88	WD, I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	VCCI

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
D20	I/O
E1	I/O
E2	I/O
E3	I/O
E4	VCCA
E17	VCCI
E18	I/O
E19	I/O
E20	I/O
F1	I/O
F2	I/O
F3	I/O
F4	VCCI
F17	I/O
F18	I/O
F19	I/O
F20	I/O
G1	I/O
G2	I/O
G3	I/O
G4	VCCI
G17	VCCI
G18	I/O
G19	I/O
G20	I/O
H1	I/O
H2	I/O
H3	I/O
H4	VCCA
H17	I/O
H18	I/O
H19	I/O
H20	I/O
J1	I/O
J2	I/O
J3	I/O
J4	VCCI

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
M10	GND
M11	GND
M12	GND
M17	I/O
M18	I/O
M19	I/O
M20	I/O
N1	I/O
N2	I/O
N3	I/O
N4	VCCI
N17	VCCI
N18	I/O
N19	I/O
N20	I/O
P1	I/O
P2	I/O
P3	I/O
P4	VCCA
P17	I/O
P18	I/O
P19	I/O
P20	I/O
R1	I/O
R2	I/O
R3	I/O
R4	VCCI
R17	VCCI
R18	I/O
R19	I/O
R20	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T17	VCCA
T18	I/O

Table 61 • **PG132**

PG132	
Pin Number	**A42MX09 Function**
G12	VSV
F13	I/O
F12	I/O
F11	I/O
F10	I/O
E13	I/O
D13	I/O
D12	I/O
C13	I/O
B13	I/O
D11	I/O
C12	I/O
A13	I/O
C11	I/O
B12	SDI
B11	I/O
C10	I/O
A12	I/O
A11	I/O
B10	I/O
D8	I/O
A10	I/O
C8	I/O
A9	I/O
B8	PRBA
A8	I/O
B7	CLKA
A7	I/O
B6	CLKB
A6	I/O
C6	PRBB
A5	I/O
D6	I/O
A4	I/O
B4	I/O
A3	I/O
C4	I/O