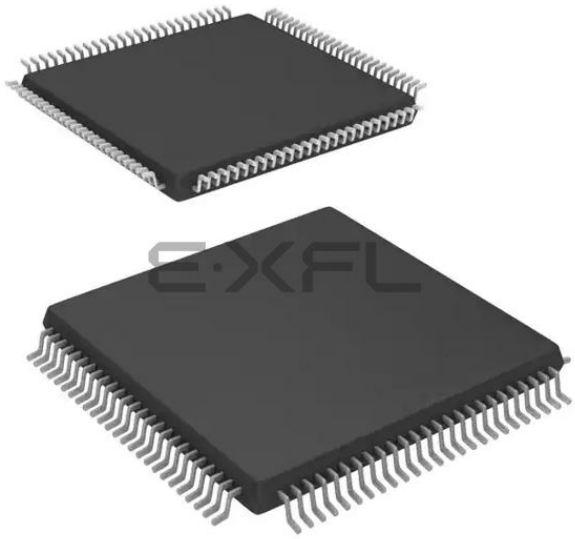

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Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	83
Number of Gates	14000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx09-3vqg100

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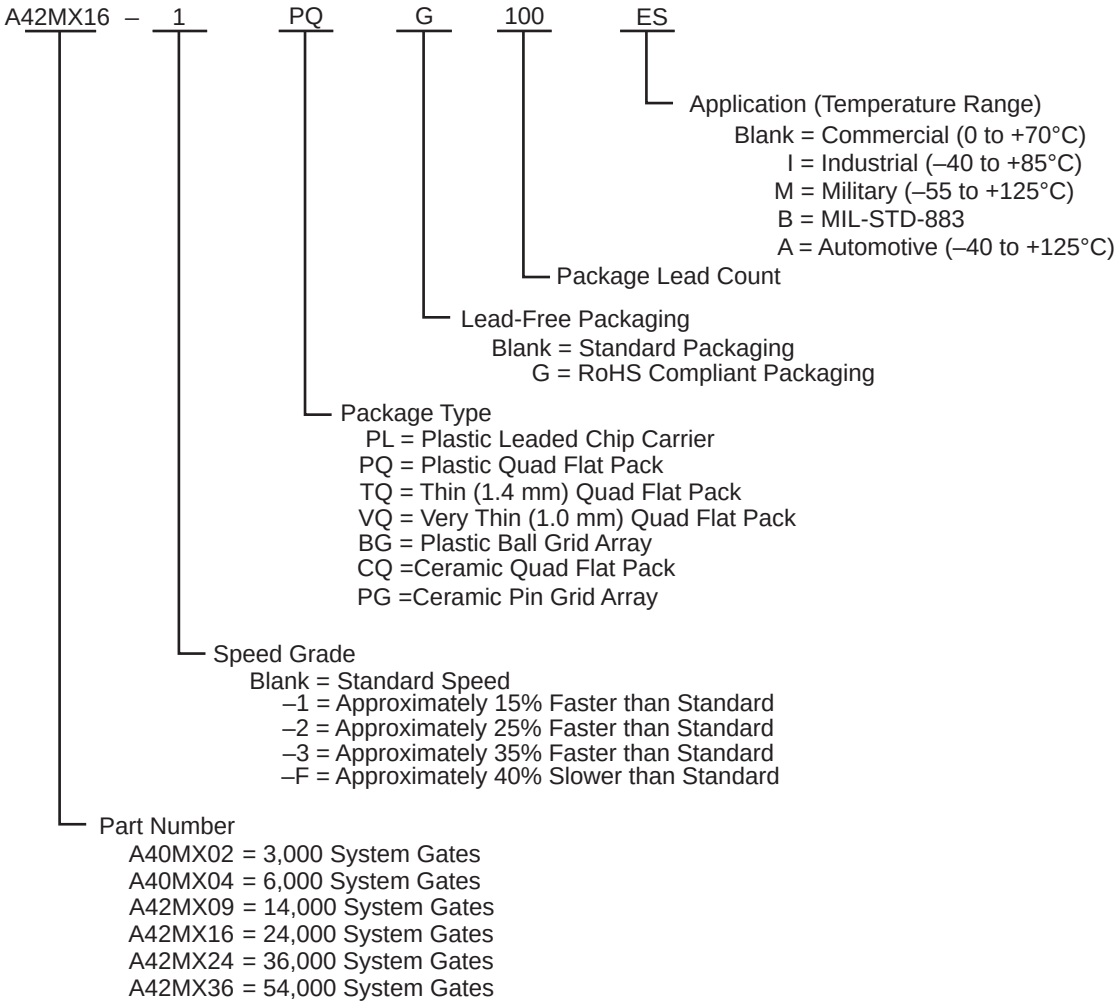
2.3 Ordering Information

The following figure shows ordering information.All the following tables show plastic and ceramic device resources, temperature and speed grade offerings.

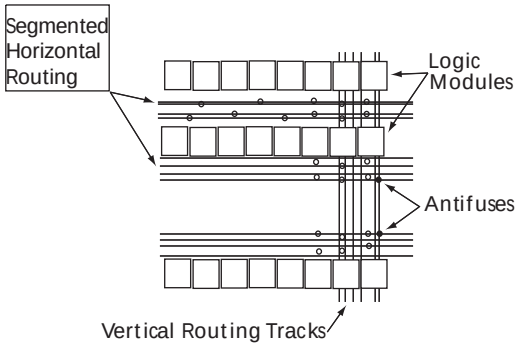
Figure 1 • **Ordering Information**



3.2.3.3 Antifuse Structures

An antifuse is a “normally open” structure. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient programming algorithms. There are no pre-existing connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For instance, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Figure 7 • **MX Routing Structure**



3.2.4 Clock Networks

The 40MX devices have one global clock distribution network (CLK). A signal can be put on the CLK network by being routed through the CLKBUF buffer.

In 42MX devices, there are two low-skew, high-fanout clock distribution networks, referred to as CLKA and CLKB. Each network has a clock module (CLKMOD) that can select the source of the clock signal from any of the following (Figure 8, page 11):

- Externally from the CLKA pad, using CLKBUF buffer
- Externally from the CLKB pad, using CLKBUF buffer
- Internally from the CLKINTA input, using CLKINT buffer
- Internally from the CLKINTB input, using CLKINT buffer

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

Clock input pads in both 40MX and 42MX devices can also be used as normal I/Os, bypassing the clock networks.

The A42MX36 device has four additional register control resources, called quadrant clock networks (Figure 9, page 11). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

Figure 8 • **Clock Networks of 42MX Devices**

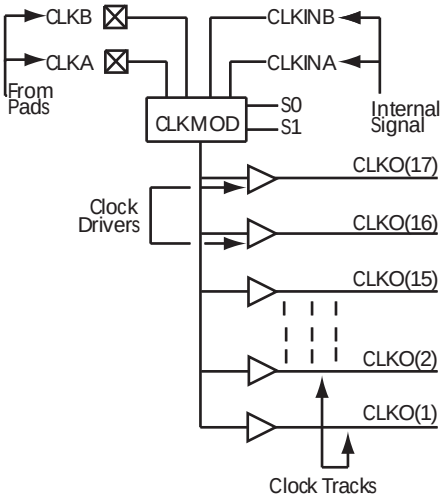
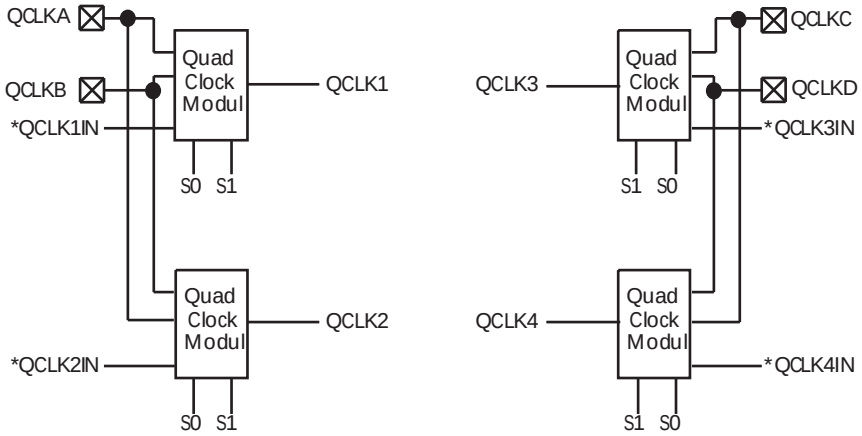


Figure 9 • **Quadrant Clock Network of A42MX36 Devices**



Note: *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

3.2.5 MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 10, page 12 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (See the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 10, page 12). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. See the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 µA.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 11, page 12). When the PCI fuse is not programmed, the output drive is standard.

A sample calculation of the absolute maximum power dissipation allowed for a TQ176 package at commercial temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (°\text{C})}{\theta_{ja}(°(\text{C/W}))} = \frac{150°\text{C} - 70°\text{C}}{(28°\text{C})/\text{W}} = 2.86\text{W}$$

EQ 5

The maximum power dissipation for military-grade devices is a function of θ_{jc}. A sample calculation of the absolute maximum power dissipation allowed for CQFP 208-pin package at military temperature and still air is given in the following equation

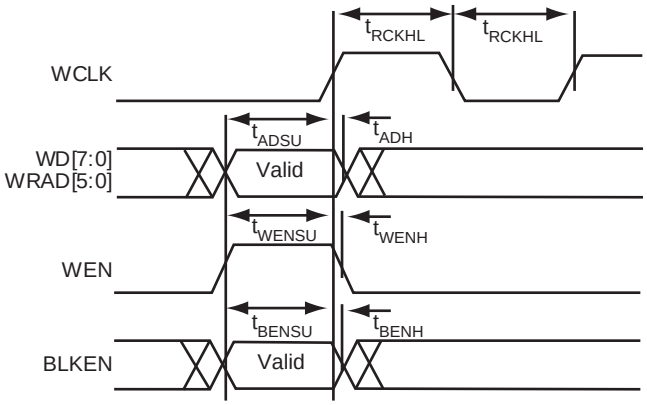
$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (°\text{C})}{\theta_{jc}(°(\text{C/W}))} = \frac{150°\text{C} - 125°\text{C}}{(6.3°\text{C})/\text{W}} = 3.97\text{W}$$

EQ 6

Table 27 • **Package Thermal Characteristics**

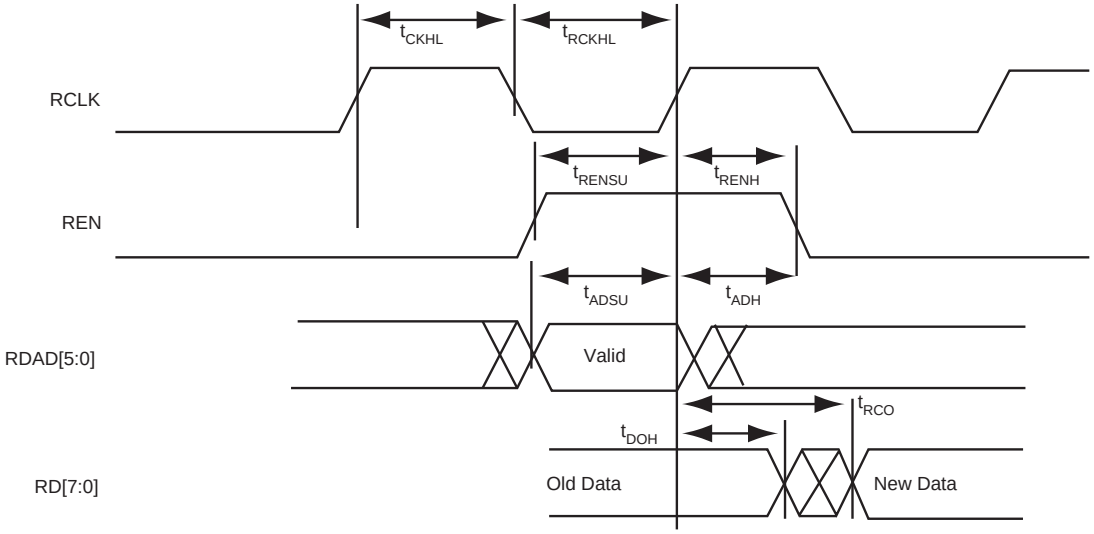
			θ_{ja}			
Plastic Packages	**Pin Count**	θ_{jc}	**Still Air**	**1.0 m/s 200 ft/min.**	**2.5 m/s 500 ft/min.**	**Units**
Plastic Quad Flat Pack	100	12.0	27.8	23.4	21.2	°C/W
Plastic Quad Flat Pack	144	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	160	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	208	8.0	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack	240	8.5	25.6	22.3	20.8	°C/W
Plastic Leaded Chip Carrier	44	16.0	20.0	24.5	22.0	°C/W
Plastic Leaded Chip Carrier	68	13.0	25.0	21.0	19.4	°C/W
Plastic Leaded Chip Carrier	84	12.0	22.5	18.9	17.6	°C/W
Thin Plastic Quad Flat Pack	176	11.0	24.7	19.9	18.0	°C/W
Very Thin Plastic Quad Flat Pack	80	12.0	38.2	31.9	29.4	°C/W
Very Thin Plastic Quad Flat Pack	100	10.0	35.3	29.4	27.1	°C/W
Plastic Ball Grid Array	272	3.0	18.3	14.9	13.9	°C/W
Ceramic Packages						
Ceramic Pin Grid Array	132	4.8	25.0	20.6	18.7	°C/W
Ceramic Quad Flat Pack	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack	256	2.0	20.0	16.5	15.0	°C/W

Figure 30 • **42MX SRAM Write Operation**



Note: Identical timing for falling edge clock

Figure 31 • **42MX SRAM Synchronous Read Operation**



Note: Identical timing for falling edge clock

Figure 32 • **42MX SRAM Asynchronous Read Operation—Type 1 (Read Address Controlled)**

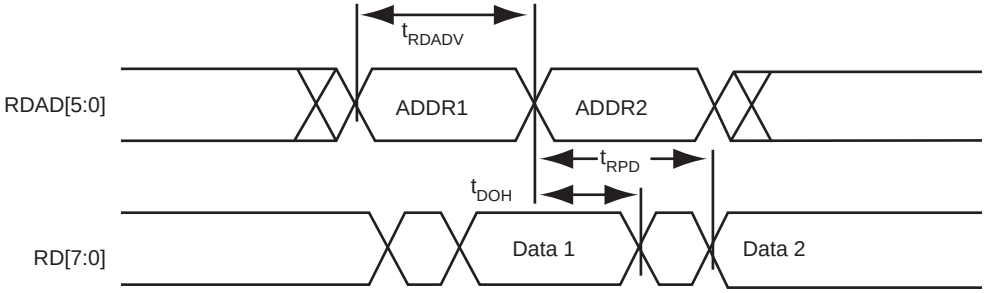


Table 33 • **Timing Parameters for 33 MHz PCI**

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{SU(PTP)}$	Input Set-Up Time to CLK—Point-to-Point	10, 12[2]	–	1.5	–	1.5	–	ns
t_H	Input Hold to CLK	0	–	0	–	0	–	ns

1. TOFF is system dependent. MX PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.
2. REQ# and GNT# are point-to-point signals and have different output valid delay and input setup times than do bussed signals. GNT# has a setup of 10; REW# has a setup of 12.

3.11.6.1 Timing Characteristics

The following tables list the timing characteristics.

Table 34 • **A40MX02 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t_{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t_{PD2}	Dual-Module Macros		2.7		3.1		3.5		4.1		5.7	ns
t_{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays[1]												
t_{RD1}	FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.8	ns
t_{RD2}	FO = 2 Routing Delay		1.8		2.1		2.4		2.8		3.9	ns
t_{RD3}	FO = 3 Routing Delay		2.3		2.7		3.0		3.6		5.0	ns
t_{RD4}	FO = 4 Routing Delay		2.9		3.3		3.7		4.4		6.1	ns
t_{RD8}	FO = 8 Routing Delay		4.9		5.7		6.5		7.6		10.6	ns
Logic Module Sequential Timing[2]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t_A	Flip-Flop Clock Input Period	4.8		5.6		6.3		7.5		10.4		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		181		168		154		134		80	MHz

Table 38 • **A42MX09 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			1.0		1.2		1.3		1.6		2.2	ns
t_{INYL}	Pad-to-Y LOW			0.8		0.9		1.0		1.2		1.7	ns
t_{INGH}	G to Y HIGH			1.3		1.4		1.6		1.9		2.7	ns
t_{INGL}	G to Y LOW			1.3		1.4		1.6		1.9		2.7	ns
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			2.0		2.2		2.5		3.0		4.2	ns
t_{IRD2}	FO = 2 Routing Delay			2.3		2.5		2.9		3.4		4.7	ns
t_{IRD3}	FO = 3 Routing Delay			2.5		2.8		3.2		3.7		5.2	ns
t_{IRD4}	FO = 4 Routing Delay			2.8		3.1		3.5		4.1		5.7	ns
t_{IRD8}	FO = 8 Routing Delay			3.7		4.1		4.7		5.5		7.7	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		2.4		2.7		3.0		3.6		5.0	ns
		FO = 256		2.7		3.0		3.4		4.0		5.5	ns
t_{CKL}	Input HIGH to LOW	FO = 32		3.5		3.9		4.4		5.2		7.3	ns
		FO = 256		3.9		4.3		4.9		5.7		8.0	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t_{CKSW}	Maximum Skew	FO = 32		0.3		0.3		0.4		0.5		0.6	ns
		FO = 256		0.3		0.3		0.4		0.5		0.6	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	2.3		2.6		3.0		3.5		4.9		ns
		FO = 256	2.2		2.4		3.3		3.9		5.5		ns
t_P	Minimum Period	FO = 32	3.4		3.7		4.0		4.7		7.8		ns
		FO = 256	3.7		4.1		4.5		5.2		8.6		ns
f_{MAX}	Maximum Frequency	FO = 32		296		269		247		215		129	MHz
		FO = 256		268		244		224		195		117	MHz

Table 39 • **A42MX09 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			1.5		1.6		1.8		2.17		3.0	ns
t_{INYL}	Pad-to-Y LOW			1.2		1.3		1.4		1.7		2.4	ns
t_{INGH}	G to Y HIGH			1.8		2.0		2.3		2.7		3.7	ns
t_{INGL}	G to Y LOW			1.8		2.0		2.3		2.7		3.7	ns
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			2.8		3.2		3.6		4.2		5.9	ns
t_{IRD2}	FO = 2 Routing Delay			3.2		3.5		4.0		4.7		6.6	ns
t_{IRD3}	FO = 3 Routing Delay			3.5		3.9		4.4		5.2		7.3	ns
t_{IRD4}	FO = 4 Routing Delay			3.9		4.3		4.9		5.7		8.0	ns
t_{IRD8}	FO = 8 Routing Delay			5.2		5.8		6.6		7.7		10.8	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		4.1		4.5		5.1		6.0		8.4	ns
		FO = 256		4.5		5.0		5.6		6.7		9.3	ns
t_{CKL}	Input HIGH to LOW	FO = 32		5.0		5.5		6.2		7.3		10.2	ns
		FO = 256		5.4		6.0		6.8		8.0		11.2	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	1.7		1.9		2.1		2.5		3.5		ns
		FO = 256	1.9		2.1		2.3		2.7		3.8		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	1.7		1.9		2.1		2.5		3.5		ns
		FO = 256	1.9		2.1		2.3		2.7		3.8		ns
t_{CKSW}	Maximum Skew	FO = 32		0.4		0.5		0.5		0.6		0.9	ns
		FO = 256		0.4		0.5		0.5		0.6		0.9	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	3.3		3.7		4.2		4.9		6.9		ns
		FO = 256	3.7		4.1		4.6		5.5		7.6		ns
t_P	Minimum Period	FO = 32	5.6		6.2		6.7		7.8		12.9		ns
		FO = 256	6.1		6.8		7.4		8.5		14.2		ns
f_{MAX}	Maximum Frequency	FO = 32		177		161		148		129		77	MHz
		FO = 256		161		146		135		117		70	MHz

Table 40 • **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RD3}	FO = 3 Routing Delay			1.3		1.4		1.6		1.9		2.7	ns
t_{RD4}	FO = 4 Routing Delay			1.6		1.7		2.0		2.3		3.2	ns
t_{RD8}	FO = 8 Routing Delay			2.6		2.9		3.2		3.8		5.3	ns
Logic Module Sequential Timing[3,4]													
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up		0.3		0.4		0.4		0.5		0.7		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up		0.7		0.8		0.9		1.0		1.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		3.4		3.8		4.3		5.0		7.1		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		4.5		5.0		5.6		6.6		9.2		ns
t_A	Flip-Flop Clock Input Period		6.8		7.6		8.6		10.1		14.1		ns
t_{INH}	Input Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Set-Up		0.5		0.5		0.6		0.7		1.0		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up		0.5		0.5		0.6		0.7		1.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency			215		195		179		156		94	MHz
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			1.1		1.2		1.3		1.6		2.2	ns
t_{INYL}	Pad-to-Y LOW			0.8		0.9		1.0		1.2		1.7	ns
t_{INGH}	G to Y HIGH			1.4		1.6		1.8		2.1		2.9	ns
t_{INGL}	G to Y LOW			1.4		1.6		1.8		2.1		2.9	ns
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			1.8		2.0		2.3		2.7		4.0	ns
t_{IRD2}	FO = 2 Routing Delay			2.1		2.3		2.6		3.1		4.3	ns
t_{IRD3}	FO = 3 Routing Delay			2.3		2.6		3.0		3.5		4.9	ns
t_{IRD4}	FO = 4 Routing Delay			2.6		3.0		3.3		3.9		5.4	ns
t_{IRD8}	FO = 8 Routing Delay			3.6		4.0		4.6		5.4		7.5	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		2.6		2.9		3.3		3.9		5.4	ns
		FO = 384		2.9		3.2		3.6		4.3		6.0	ns
t_{CKL}	Input HIGH to LOW	FO = 32		3.8		4.2		4.8		5.6		7.8	ns
		FO = 384		4.5		5.0		5.6		6.6		9.2	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	3.2		3.5		4.0		4.7		6.6		ns
		FO = 384	3.7		4.1		4.6		5.4		7.6		ns

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays												
t_{INPY}	Input Data Pad-to-Y		1.0		1.1		1.3		1.5		2.1	ns
t_{INGO}	Input Latch Gate-to-Output		1.3		1.4		1.6		1.9		2.6	ns
t_{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{ILA}	Latch Active Pulse Width	4.7		5.2		5.9		6.9		9.7		ns

Table 44 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions[1]												
t_{PD}	Internal Array Module Delay		1.3		1.5		1.7		2.0		2.7	ns
t_{PDD}	Internal Decode Module Delay		1.6		1.8		2.0		2.4		3.3	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.2		1.4		2.0	ns
t_{RD2}	FO = 2 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t_{RD3}	FO =3 Routing Delay		1.6		1.8		2.0		2.4		3.4	ns
t_{RD4}	FO = 4 Routing Delay		2.0		2.2		2.5		2.9		4.1	ns
t_{RD5}	FO = 8 Routing Delay		3.3		3.7		4.2		4.9		6.9	ns
t_{RDD}	Decode-to-Output Routing Delay		0.3		0.4		0.4		0.5		0.7	ns
Logic Module Sequential Timing[3, 4]												
t_{CO}	Flip-Flop Clock-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch Gate-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t_{SUD}	Flip-Flop (Latch) Set-Up Time	0.3		0.3		0.4		0.5		0.7		ns
t_{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		1.6		1.7		2.0		2.3		3.2	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.5		6.4		9.0		ns
Synchronous SRAM Operations												
t_{RC}	Read Cycle Time	6.8		7.5		8.5		10.0		14.0		ns
t_{WC}	Write Cycle Time	6.8		7.5		8.5		10.0		14.0		ns
t_{RCKHL}	Clock HIGH/LOW Time	3.4		3.8		4.3		5.0		7.0		ns
t_{RCO}	Data Valid After Clock HIGH/LOW		3.4		3.8		4.3		5.0		7.0	ns
t_{ADSU}	Address/Data Set-Up Time	1.6		1.8		2.0		2.4		3.4		ns
Synchronous SRAM Operations (continued)												
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Set-Up	0.6		0.7		0.8		0.9		1.3		ns
t_{RENH}	Read Enable Hold	3.4		3.8		4.3		5.0		7.0		ns
t_{WENSU}	Write Enable Set-Up	2.7		3.0		3.4		4.0		5.6		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Set-Up	2.8		3.1		3.5		4.1		5.7		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		ns

4 Package Pin Assignments

The following figures and tables give the details of the package pin assignments.

Figure 38 • **PL44**

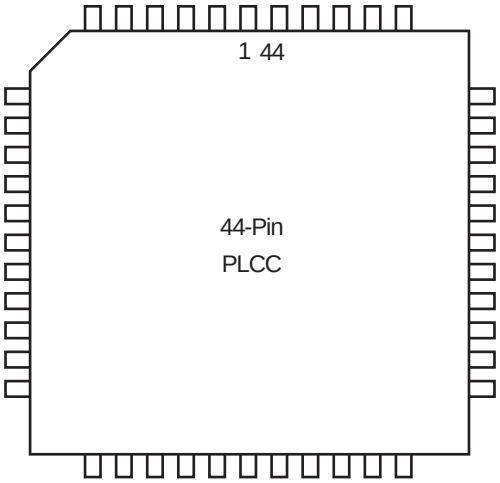


Table 47 • **PL44**

PL44		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
1	I/O	I/O
2	I/O	I/O
3	VCC	VCC
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	GND	GND
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	VCC	VCC
15	I/O	I/O
16	VCC	VCC
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O

Table 52 • **PQ160**

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	VCCA	VCCA
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	VCCA	VCCA
139	VCCI	VCCI	VCCI
140	GND	GND	GND
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	GND	GND	GND
146	NC	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	NC	VCCA	VCCA
151	NC	I/O	I/O
152	NC	I/O	I/O
153	NC	I/O	I/O
154	NC	I/O	I/O
155	GND	GND	GND
156	I/O	I/O	I/O
157	I/O	I/O	I/O
158	I/O	I/O	I/O
159	MODE	MODE	MODE
160	GND	GND	GND

Table 54 • **PQ240**

PQ240	
Pin Number	**A42MX36 Function**
163	WD, I/O
164	WD, I/O
165	I/O
166	QCLKA, I/O
167	I/O
168	I/O
169	I/O
170	I/O
171	I/O
172	VCCI
173	I/O
174	WD, I/O
175	WD, I/O
176	I/O
177	I/O
178	TDI, I/O
179	TMS, I/O
180	GND
181	VCCA
182	GND
183	I/O
184	I/O
185	I/O
186	I/O
187	I/O
188	I/O
189	I/O
190	I/O
191	I/O
192	VCCI
193	I/O
194	I/O
195	I/O
196	I/O
197	I/O
198	I/O
199	I/O

Table 54 • **PQ240**

PQ240	
Pin Number	**A42MX36 Function**
200	I/O
201	I/O
202	I/O
203	I/O
204	I/O
205	I/O
206	VCCA
207	I/O
208	I/O
209	VCCA
210	VCCI
211	I/O
212	I/O
213	I/O
214	I/O
215	I/O
216	I/O
217	I/O
218	I/O
219	VCCA
220	I/O
221	I/O
222	I/O
223	I/O
224	I/O
225	I/O
226	I/O
227	VCCI
228	I/O
229	I/O
230	I/O
231	I/O
232	I/O
233	I/O
234	I/O
235	I/O
236	I/O

Table 55 • **VQ80**

VQ80		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
49	I/O	I/O
50	CLK, I/O	CLK, I/O
51	I/O	I/O
52	MODE	MODE
53	VCC	VCC
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	GND	GND
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	VCC	**VCC**
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O

Table 56 • **VQ100**

VQ100		
Pin Number	**A42MX09 Function**	**A42MX16 Function**
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	LP	LP
63	VCCA	VCCA
64	VCCI	VCCI
65	VCCA	VCCA
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	GND	GND
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	SDI, I/O	SDI, I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	GND	GND
83	I/O	I/O
84	I/O	I/O
85	PRA, I/O	PRA, I/O
86	I/O	I/O
87	CLKA, I/O	CLKA, I/O
88	VCCA	VCCA
89	I/O	I/O
90	CLKB, I/O	CLKB, I/O
91	I/O	I/O
92	PRB, I/O	PRB, I/O

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
170	VCCA
171	I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	I/O
177	I/O
178	I/O
179	I/O
180	GND
181	I/O
182	I/O
183	I/O
184	I/O
185	I/O
186	I/O
187	I/O
188	MODE
189	VCCA
190	GND
191	NC
192	NC
193	NC
194	I/O
195	DCLK, I/O
196	I/O
197	I/O
198	I/O
199	WD, I/O
200	WD, I/O
201	VCCI
202	I/O
203	I/O
204	I/O
205	I/O
206	GND

Table 61 • **PG132**

PG132	
Pin Number	**A42MX09 Function**
B3	I/O
A2	I/O
C3	DCLK
B5	GNDA
E12	GNDA
J2	GNDA
M9	GNDA
B9	GNDI
C5	GNDI
E11	GNDI
F4	GNDI
J3	GNDI
J11	GNDI
L5	GNDI
L9	GNDI
C9	GNDQ
E3	GNDQ
K12	GNDQ
D7	VCCA
G3	VCCA
G10	VCCA
L7	VCCA
C7	VCCI
G2	VCCI
G11	VCCI
K7	VCCI