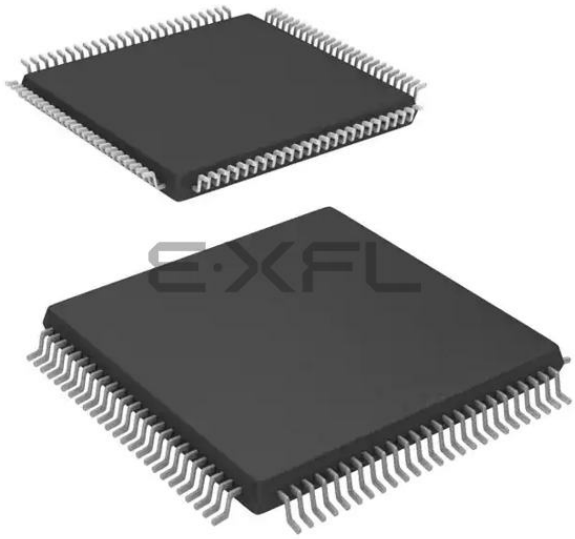

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	83
Number of Gates	14000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx09-fvq100

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- Table 15, page 21 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 22, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 23, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

1.2 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Added CQFP package information for A42MX16 device in Product Profile, page 1 and Ceramic Device Resources, page 4 (SAR 79522).
- Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in Temperature Grade Offerings, page 5 (SAR 79519)
- Changed Silicon Sculptor II to Silicon Sculptor in Programming, page 12 (SAR 38754)
- Added Figure 53, page 158 CQ172 package (SAR 79522).

1.3 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Added Figure 42, page 97 PQ144 Package for A42MX09 device (SAR 69776)
- Added Figure 52, page 153 PQ132 Package for A42MX09 device (SAR 69776)

1.4 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Added information on power-up behavior for A42MX24 and A42MX36 devices to the Power Supply, page 13 (SAR 42096
- Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793)

1.5 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- The FuseLock logo and accompanying text was removed from the User Security, page 12. This marking is no longer used on Microsemi devices (PCN 0915)
- The Development Tool Support, page 19 was updated (SAR 38512)

1.6 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- Ordering Information, page 3 was updated to include lead-free package ordering codes (SAR 21968)
- The User Security, page 12 was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673)

2.3 Ordering Information

The following figure shows ordering information.All the following tables show plastic and ceramic device resources, temperature and speed grade offerings.

Figure 1 • **Ordering Information**

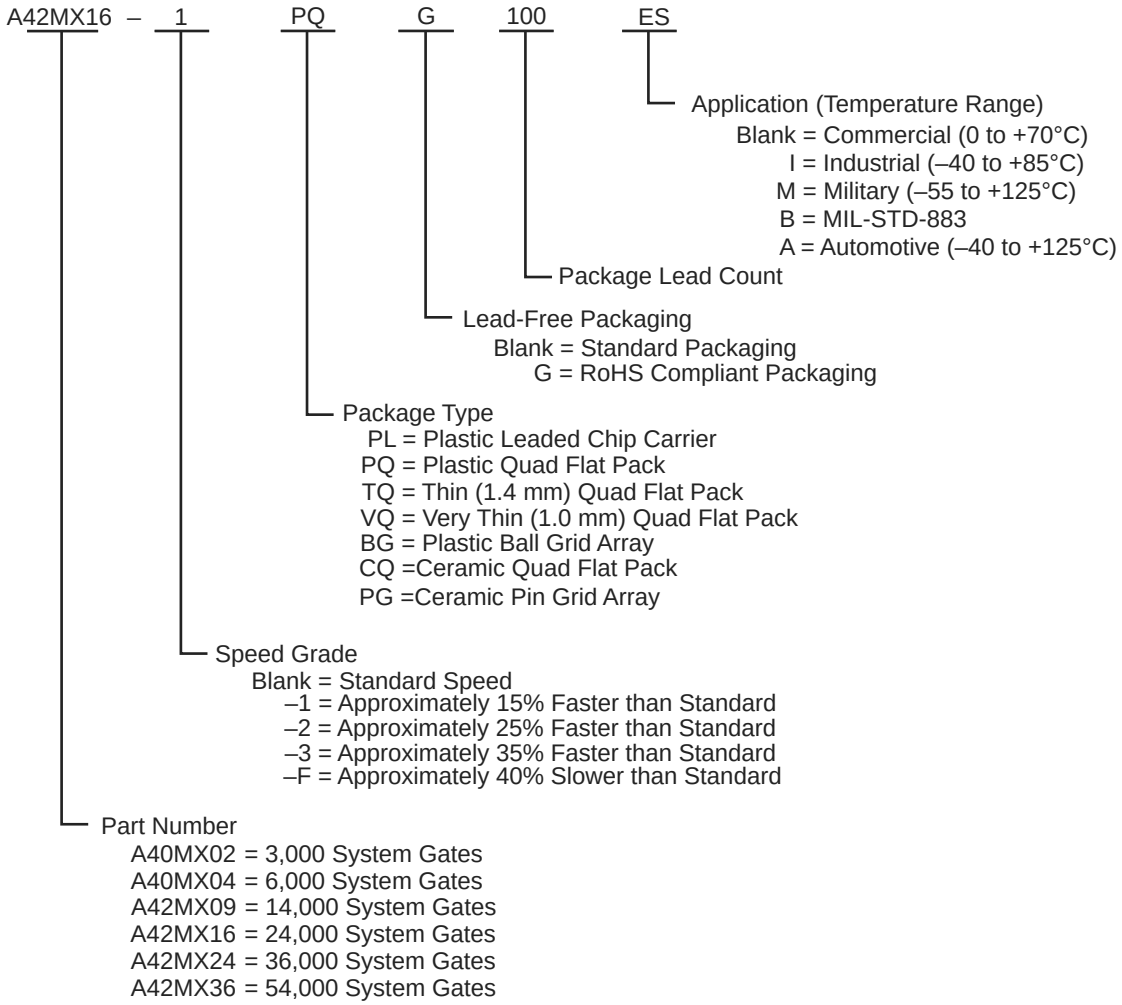
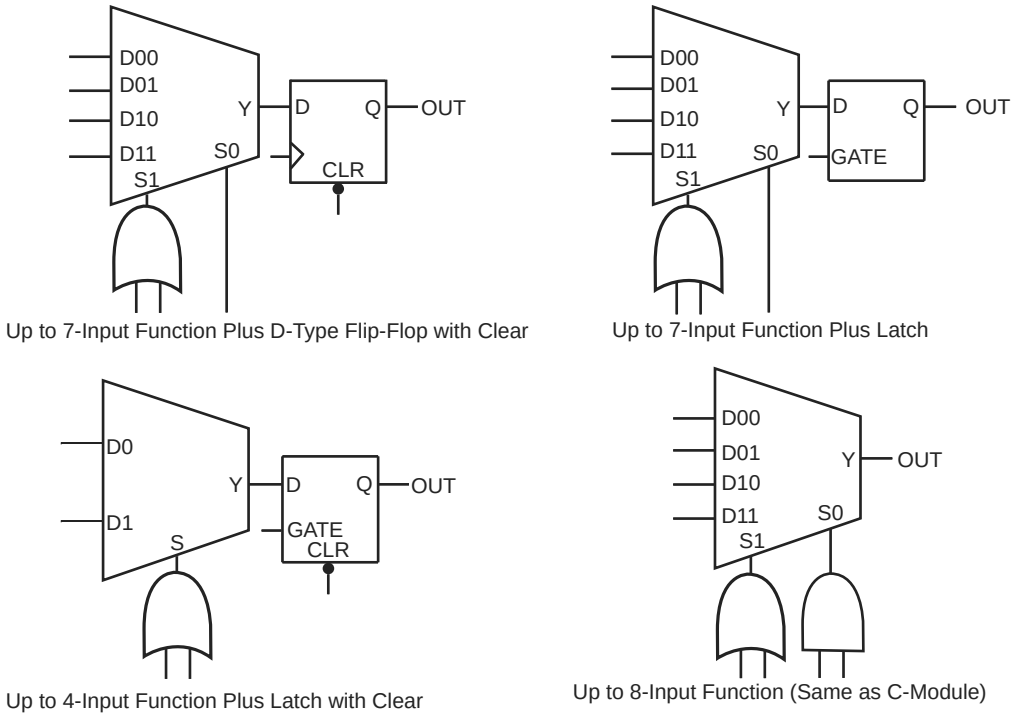


Figure 4 • **42MX S-Module Implementation**



A42MX24 and A42MX36 devices contain D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry, providing a fast, wide-input AND function similar to that found in CPLD architectures (Figure 5, page 9). The D-module allows A42MX24 and A42MX36 devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin, and can also be fed back into the array to be incorporated into other logic.

3.2.2 Dual-Port SRAM Modules

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the A42MX36 dual-port SRAM block is shown in Figure 6, page 9.

The A42MX36 SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]), which are connected to segmented vertical routing tracks.

The A42MX36 dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring FIFO and LIFO queues. The ACTgen Macro Builder within Microsemi's designer software provides capability to quickly design memory functions with the SRAM blocks. Unused SRAM blocks can be used to implement registers for other user logic within the design.

Figure 5 • **A42MX24 and A42MX36 D-Module Implementation**

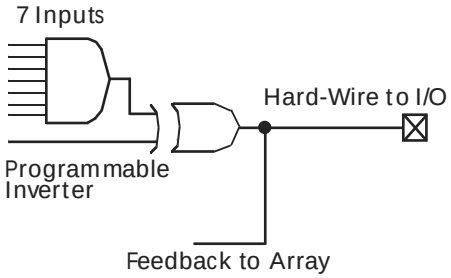
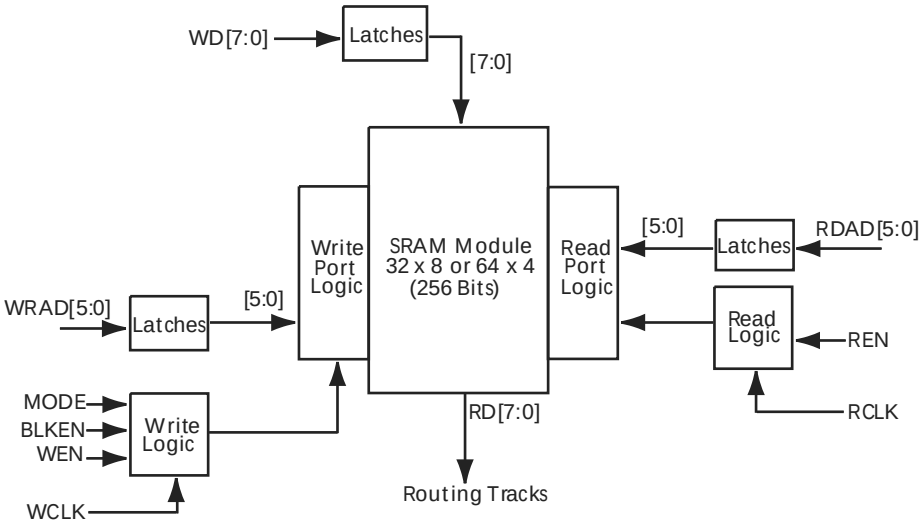


Figure 6 • **A42MX36 Dual-Port SRAM Block**



3.2.3 Routing Structure

The MX architecture uses vertical and horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may be continuous or split into segments. Varying segment lengths allow the interconnect of over 90% of design tracks to occur with only two antifuse connections. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

3.2.3.1 Horizontal Routing

Horizontal routing tracks span the whole row length or are divided into multiple segments and are located in between the rows of modules. Any segment that spans more than one-third of the row length is considered a long horizontal segment. A typical channel is shown in Figure 7, page 10. Within horizontal routing, dedicated routing tracks are used for global clock networks and for power and ground tie-off tracks. Non-dedicated tracks are used for signal nets.

3.2.3.2 Vertical Routing

Another set of routing tracks run vertically through the module. There are three types of vertical tracks: input, output, and long. Long tracks span the column length of the module, and can be divided into multiple segments. Each segment in an input track is dedicated to the input of a particular module; each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing.

Each output segment spans four channels (two above and two below), except near the top and bottom of the array, where edge effects occur. Long vertical tracks contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 7, page 10.

f_{q2} = Average second routed array clock rate in MHz)

Table 7 • **Fixed Capacitance Values for MX FPGAs (pF)**

Device Type	r1 routed_Clk1	r2 routed_Clk2
A40MX02	41.4	N/A
A40MX04	68.6	N/A
A42MX09	118	118
A42MX16	165	165
A42MX24	185	185
A42MX36	220	220

3.4.6 Test Circuitry and Silicon Explorer II Probe

MX devices contain probing circuitry that provides built-in access to every node in a design, via the use of Silicon Explorer II. Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer software, allow users to examine any of the internal nets of the device while it is operating in a prototyping or a production system. The user can probe into an MX device without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle and providing a true representation of the device under actual functional situations.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

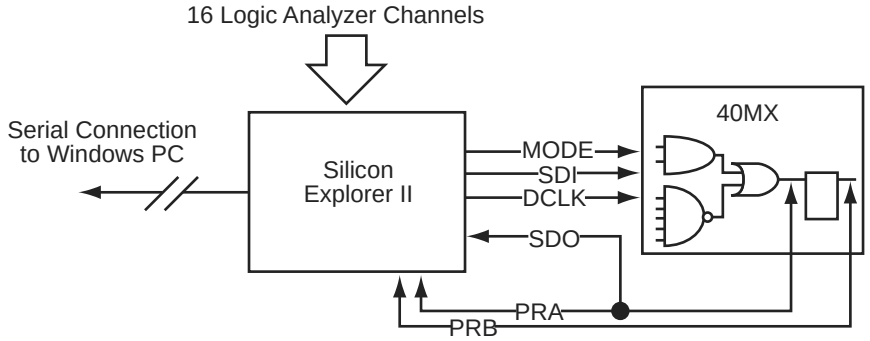
Silicon Explorer II is used to control the MODE, DCLK, SDI and SDO pins in MX devices to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the MODE pin is held HIGH.

Figure 12, page 16 illustrates the interconnection between Silicon Explorer II and 40MX devices, while Figure 13, page 17 illustrates the interconnection between Silicon Explorer II and 42MX devices

To allow for probing capabilities, the security fuses must not be programmed. (See User Security, page 12 for the security fuses of 40MX and 42MX devices). Table 8, page 17 summarizes the possible device configurations for probing.

PRA and PRB pins are dual-purpose pins. When the “Reserve Probe Pin” is checked in the Designer software, PRA and PRB pins are reserved as dedicated outputs for probing. If PRA and PRB pins are required as user I/Os to achieve successful layout and “Reserve Probe Pin” is checked, the layout tool will override the option and place user I/Os on PRA and PRB pins.

Figure 12 • **Silicon Explorer II Setup with 40MX**



Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary-scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

Figure 14 • **42MX IEEE 1149.1 Boundary Scan Circuitry**

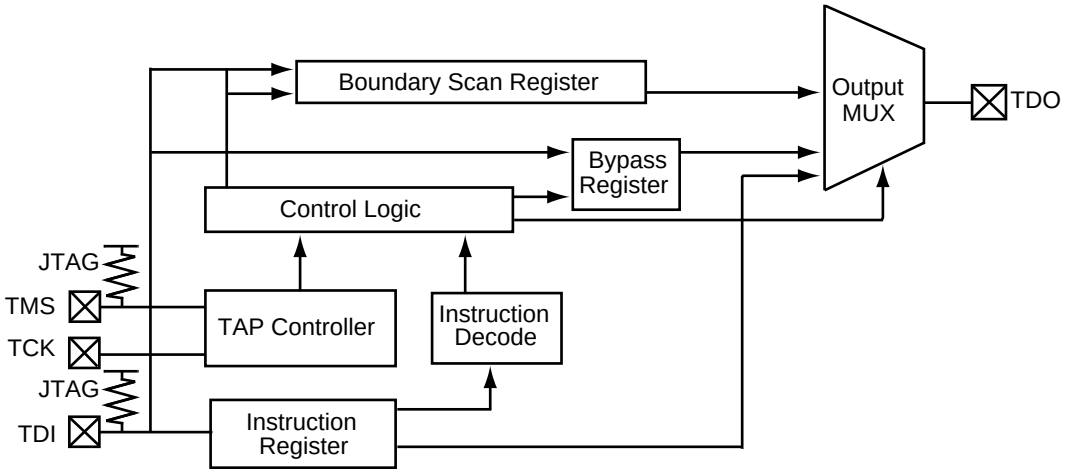


Table 9 • **Test Access Port Descriptions**

Port	Description
TMS (Test Mode Select)	Serial input for the test logic control bits. Data is captured on the rising edge of the test logic clock (TCK).
TCK (Test Clock Input)	Dedicated test logic clock used serially to shift test instruction, test data, and control inputs on the rising edge of the clock, and serially to shift the output data on the falling edge of the clock. The maximum clock frequency for TCK is 20 MHz.
TDI (Test Data Input)	Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock.
TDO (Test Data Output)	Serial output for test instruction and data from the test logic. TDO is set to an Inactive Drive state (high impedance) when data scanning is not in progress.

Table 10 • **Supported BST Public Instructions**

Instruction	IR Code (IR2.IR0)	Instruction Type	Description
EXTEST	000	Mandatory	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
SAMPLE/PRELOAD	001	Mandatory	Allows a snapshot of the signals at the device pins to be captured and examined during operation
HIGH Z	101	Optional	Tristates all I/Os to allow external signals to drive pins. See the IEEE Standard 1149.1 specification.
CLAMP	110	Optional	Allows state of signals driven from component pins to be determined from the Boundary-Scan Register. See the IEEE Standard 1149.1 specification for details.
BYPASS	111	Mandatory	Enables the bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the test chain.

A sample calculation of the absolute maximum power dissipation allowed for a TQ176 package at commercial temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (°\text{C})}{\theta_{ja}(°(\text{C}/\text{W}))} = \frac{150°\text{C} - 70°\text{C}}{(28°\text{C})/\text{W}} = 2.86\text{W}$$

EQ 5

The maximum power dissipation for military-grade devices is a function of θ_{jc}. A sample calculation of the absolute maximum power dissipation allowed for CQFP 208-pin package at military temperature and still air is given in the following equation

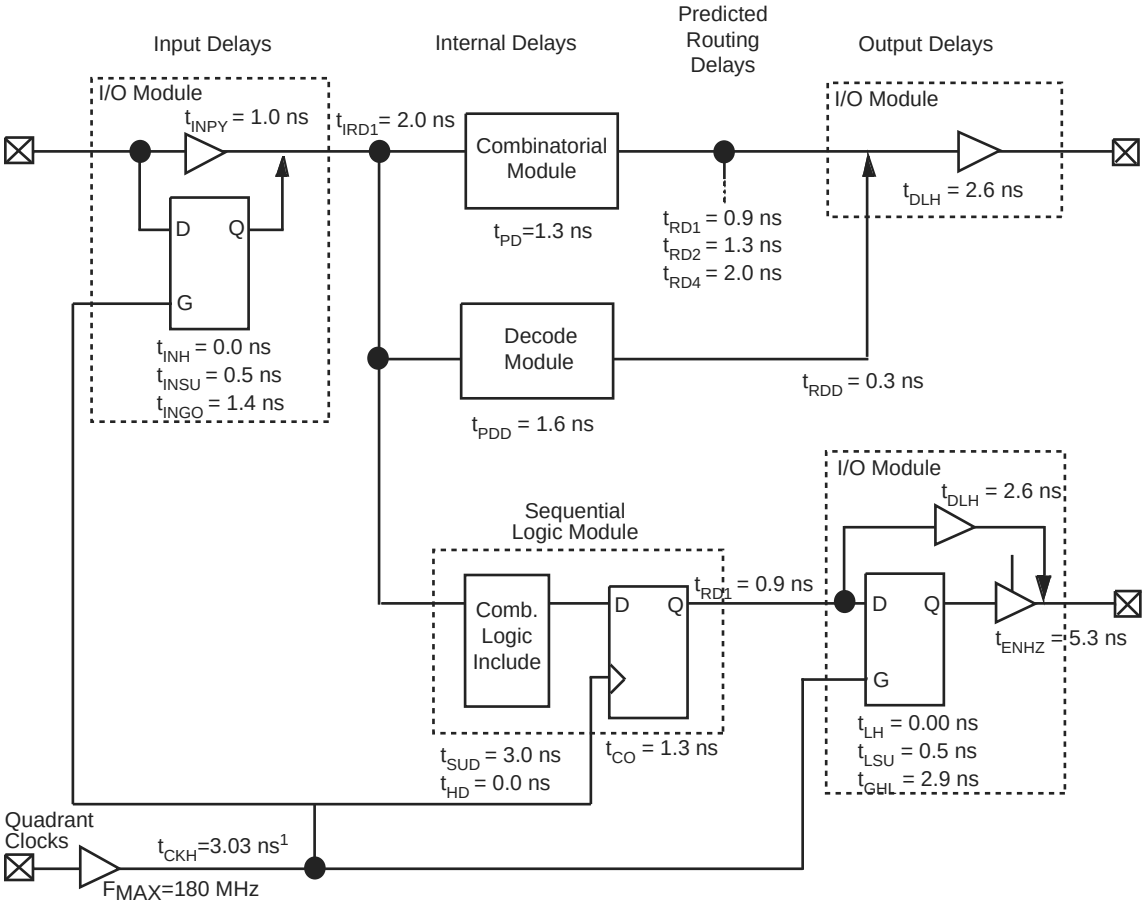
$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (°\text{C})}{\theta_{jc}(°(\text{C}/\text{W}))} = \frac{150°\text{C} - 125°\text{C}}{(6.3°\text{C})/\text{W}} = 3.97\text{W}$$

EQ 6

Table 27 • **Package Thermal Characteristics**

			θ_{ja}			
Plastic Packages	**Pin Count**	θ_{jc}	**Still Air**	**1.0 m/s 200 ft/min.**	**2.5 m/s 500 ft/min.**	**Units**
Plastic Quad Flat Pack	100	12.0	27.8	23.4	21.2	°C/W
Plastic Quad Flat Pack	144	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	160	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	208	8.0	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack	240	8.5	25.6	22.3	20.8	°C/W
Plastic Leaded Chip Carrier	44	16.0	20.0	24.5	22.0	°C/W
Plastic Leaded Chip Carrier	68	13.0	25.0	21.0	19.4	°C/W
Plastic Leaded Chip Carrier	84	12.0	22.5	18.9	17.6	°C/W
Thin Plastic Quad Flat Pack	176	11.0	24.7	19.9	18.0	°C/W
Very Thin Plastic Quad Flat Pack	80	12.0	38.2	31.9	29.4	°C/W
Very Thin Plastic Quad Flat Pack	100	10.0	35.3	29.4	27.1	°C/W
Plastic Ball Grid Array	272	3.0	18.3	14.9	13.9	°C/W
Ceramic Packages						
Ceramic Pin Grid Array	132	4.8	25.0	20.6	18.7	°C/W
Ceramic Quad Flat Pack	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack	256	2.0	20.0	16.5	15.0	°C/W

Figure 19 • **42MX Timing Model (Logic Functions Using Quadrant Clocks)**



Note: 1. Load-dependent

Note: 2. Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions

Table 37 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[4]												
t_{DLH}	Data-to-Pad HIGH		5.5		6.4		7.2		8.5		11.9	ns
t_{DHL}	Data-to-Pad LOW		4.8		5.5		6.2		7.3		10.2	ns
t_{ENZH}	Enable Pad Z to HIGH		4.7		5.5		6.2		7.3		10.2	ns
t_{ENZL}	Enable Pad Z to LOW		6.8		7.9		8.9		10.5		14.7	ns
t_{ENHZ}	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9	ns
t_{ENLZ}	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7	ns
d_{TLH}	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading.

Table 38 • **A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays[1]												
t_{PD1}	Single Module		1.2		1.3		1.5		1.8		2.5	ns
t_{CO}	Sequential Clock-to-Q		1.3		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch G-to-Q		1.2		1.4		1.6		1.8		2.6	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.6		1.8		2.1		2.9	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t_{RD2}	FO = 2 Routing Delay		0.9		1.0		1.2		1.4		1.9	ns
t_{RD3}	FO = 3 Routing Delay		1.2		1.3		1.5		1.7		2.4	ns
t_{RD4}	FO = 4 Routing Delay		1.4		1.5		1.7		2.0		2.9	ns
t_{RD8}	FO = 8 Routing Delay		2.3		2.6		2.9		3.4		4.8	ns
Logic Module Sequential Timing[3, 4]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.3		0.4		0.4		0.5		0.7		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.4		0.5		0.5		0.6		0.8		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.4		3.8		4.3		5.0		7.0		ns

Table 39 • **A42MX09 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		3.4		3.8		5.5		6.4		9.0	ns
t_{DHL}	Data-to-Pad LOW		4.1		4.5		4.2		5.0		7.0	ns
t_{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t_{ENZL}	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t_{ENLZ}	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t_{GLH}	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t_{GHL}	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t_{LSU}	I/O Latch Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. *Delays based on 35 pF loading.*

Table 40 • **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays[1]												
t_{PD1}	Single Module		1.4		1.5		1.7		2.0		2.8	ns
t_{CO}	Sequential Clock-to-Q		1.4		1.6		1.8		2.1		3.0	ns
t_{GO}	Latch G-to-Q		1.4		1.5		1.7		2.0		2.8	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.6		1.7		2.0		2.3		3.3	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.8		0.9		1.0		1.2		1.6	ns
t_{RD2}	FO = 2 Routing Delay		1.0		1.2		1.3		1.5		2.1	ns

Table 40 • **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		3.2		3.6		4.0		4.7		6.6	ns
t_{DHL}	Data-to-Pad LOW		2.5		2.7		3.1		3.6		5.1	ns
t_{ENZH}	Enable Pad Z to HIGH		2.7		3.0		3.4		4.0		5.6	ns
t_{ENZL}	Enable Pad Z to LOW		3.0		3.3		3.8		4.4		6.2	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.4		6.0		6.8		8.0		11.2	ns
t_{ENLZ}	Enable Pad LOW to Z		5.0		5.6		6.3		7.4		10.4	ns
t_{GLH}	G-to-Pad HIGH		5.1		5.6		6.4		7.5		10.5	ns
t_{GHL}	G-to-Pad LOW		5.1		5.6		6.4		7.5		10.5	ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.7		6.3		7.1		8.4		11.9	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.0		8.9		10.1		11.9		16.7	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, point and position whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

Table 41 • **A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]												
t_{PD1}	Single Module		1.9		2.1		2.4		2.8		4.0	ns
t_{CO}	Sequential Clock-to-Q		2.0		2.2		2.5		3.0		4.2	ns
t_{GO}	Latch G-to-Q		1.9		2.1		2.4		2.8		4.0	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		2.2		2.4		2.8		3.3		4.6	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		1.1		1.2		1.4		1.6		2.3	ns
t_{RD2}	FO = 2 Routing Delay		1.5		1.6		1.8		2.1		3.0	ns
t_{RD3}	FO = 3 Routing Delay		1.8		2.0		2.3		2.7		3.8	ns
t_{RD4}	FO = 4 Routing Delay		2.2		2.4		2.7		3.2		4.5	ns
t_{RD8}	FO = 8 Routing Delay		3.6		4.0		4.5		5.3		7.5	ns

Table 44 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Asynchronous SRAM Operations													
t_{RPD}	Asynchronous Access Time			8.1		9.0		10.2		12.0		16.8	ns
t_{RDADV}	Read Address Valid		8.8		9.8		11.1		13.0		18.2		ns
t_{ADSU}	Address/Data Set-Up Time		1.6		1.8		2.0		2.4		3.4		ns
t_{ADH}	Address/Data Hold Time		0.0		0.0		0.0		0.0		0.0		ns
t_{RENSUA}	Read Enable Set-Up to Address Valid		0.6		0.7		0.8		0.9		1.3		ns
t_{RENHA}	Read Enable Hold		3.4		3.8		4.3		5.0		7.0		ns
t_{WENSU}	Write Enable Set-Up		2.7		3.0		3.4		4.0		5.6		ns
t_{WENH}	Write Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time			1.2		1.3		1.5		1.8		2.5	ns
Input Module Propagation Delays													
t_{INPY}	Input Data Pad-to-Y			1.0		1.1		1.3		1.5		2.1	ns
t_{INGO}	Input Latch Gate-to-Output			1.4		1.6		1.8		2.1		2.9	ns
t_{INH}	Input Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up		0.5		0.5		0.6		0.7		1.0		ns
t_{ILA}	Latch Active Pulse Width		4.7		5.2		5.9		6.9		9.7		ns
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			2.0		2.2		2.5		2.9		4.1	ns
t_{IRD2}	FO = 2 Routing Delay			2.3		2.6		2.9		3.4		4.8	ns
t_{IRD3}	FO = 3 Routing Delay			2.6		2.9		3.3		3.9		5.5	ns
t_{IRD4}	FO = 4 Routing Delay			3.0		3.3		3.8		4.4		6.2	ns
t_{IRD8}	FO = 8 Routing Delay			4.3		4.8		5.5		6.4		9.0	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		2.7		3.0		3.4		4.0		5.6	ns
		FO = 635		3.0		3.3		3.8		4.4		6.2	ns
t_{CKL}	Input HIGH to LOW	FO = 32		3.8		4.2		4.8		5.6		7.8	ns
		FO = 635		4.9		5.4		6.1		7.2		10.1	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	1.8		2.0		2.2		2.6		3.6		ns
		FO = 635	2.0		2.2		2.5		2.9		4.1		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	1.8		2.0		2.2		2.6		3.6		ns
		FO = 635	2.0		2.2		2.5		2.9		4.1		ns
t_{CKSW}	Maximum Skew	FO = 32		0.8		0.8		0.9		1.0		1.4	ns
		FO = 635		0.8		0.8		0.9		1.0		1.4	ns

Table 52 • **PQ160**

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
21	CLKA, I/O	CLKA, I/O	CLKA, I/O
22	I/O	I/O	I/O
23	PRA, I/O	PRA, I/O	PRA, I/O
24	NC	I/O	WD, I/O
25	I/O	I/O	WD, I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	NC	I/O	I/O
29	I/O	I/O	WD, I/O
30	GND	GND	GND
31	NC	I/O	WD, I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	VCCI	VCCI
36	I/O	I/O	WD, I/O
37	I/O	I/O	WD, I/O
38	SDI, I/O	SDI, I/O	SDI, I/O
39	I/O	I/O	I/O
40	GND	GND	GND
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	GND	GND	GND
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	NC	I/O	I/O
53	I/O	I/O	I/O
54	NC	VCCA	VCCA
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	VCCA	VCCA	VCCA

Table 54 • **PQ240**

PQ240	
Pin Number	**A42MX36 Function**
15	QCLKC, I/O
16	I/O
17	WD, I/O
18	WD, I/O
19	I/O
20	I/O
21	WD, I/O
22	WD, I/O
23	I/O
24	PRB, I/O
25	I/O
26	CLKB, I/O
27	I/O
28	GND
29	VCCA
30	VCCI
31	I/O
32	CLKA, I/O
33	I/O
34	PRA, I/O
35	I/O
36	I/O
37	WD, I/O
38	WD, I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	QCLKD, I/O
46	I/O
47	WD, I/O
48	WD, I/O
49	I/O
50	I/O
51	I/O

Table 55 • **VQ80**

VQ80		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
49	I/O	I/O
50	CLK, I/O	CLK, I/O
51	I/O	I/O
52	MODE	MODE
53	VCC	VCC
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	GND	GND
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	VCC	**VCC**
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O

Table 58 • **CQ208**

CQ208	
Pin Number	**A42MX36 Function**
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	GND
53	GND
54	TMS, I/O
55	TDI, I/O
56	I/O
57	WD, I/O
58	WD, I/O
59	I/O
60	VCCI
61	I/O
62	I/O
63	I/O
64	I/O
65	QCLKA, I/O
66	WD, I/O
67	WD, I/O
68	I/O
69	I/O
70	WD, I/O
71	WD, I/O
72	I/O
73	I/O

Table 58 • **CQ208**

CQ208	
Pin Number	**A42MX36 Function**
148	I/O
149	I/O
150	GND
151	I/O
152	I/O
153	I/O
154	I/O
155	I/O
156	I/O
157	GND
158	I/O
159	SDI, I/O
160	I/O
161	WD, I/O
162	WD, I/O
163	I/O
164	VCCI
165	I/O
166	I/O
167	I/O
168	WD, I/O
169	WD, I/O
170	I/O
171	QCLKD, I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	WD, I/O
177	WD, I/O
178	PRA, I/O
179	I/O
180	CLKA, I/O
181	I/O
182	VCCI
183	VCCA
184	GND

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
170	VCCA
171	I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	I/O
177	I/O
178	I/O
179	I/O
180	GND
181	I/O
182	I/O
183	I/O
184	I/O
185	I/O
186	I/O
187	I/O
188	MODE
189	VCCA
190	GND
191	NC
192	NC
193	NC
194	I/O
195	DCLK, I/O
196	I/O
197	I/O
198	I/O
199	WD, I/O
200	WD, I/O
201	VCCI
202	I/O
203	I/O
204	I/O
205	I/O
206	GND

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
T19	I/O
T20	I/O
U1	I/O
U2	I/O
U3	I/O
U4	I/O
U5	VCCI
U6	WD, I/O
U7	I/O
U8	I/O
U9	WD, I/O
U10	VCCA
U11	VCCI
U12	I/O
U13	I/O
U14	QCLKB, I/O
U15	I/O
U16	VCCI
U17	I/O
U18	GND
U19	I/O
U20	I/O
V1	I/O
V2	I/O
V3	GND
V4	GND
V5	I/O
V6	I/O
V7	I/O
V8	WD, I/O
V9	I/O
V10	I/O
V11	I/O
V12	I/O
V13	WD, I/O
V14	I/O
V15	WD, I/O