Microchip Technology - A42MX09-PL84A Datasheet

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	72
Number of Gates	14000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx09-pl84a

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- The Transient Current, page 13 is new (SAR 36930).
- Package names were revised according to standards established in *Package Mechanical Drawings* (SAR 34774)

1.7 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document

- In Table 20, page 23, the limits in VI were changed from -0.5 to VCCI + 0.5 to -0.5 to VCCA + 0.5

In Table 22, page 25, V_{OH} was changed from 3.7 to 2.4 for the min in industrial and military. V_{IH} had V_{CCI} and that was changed to VCCA

1.8 Revision 6.0

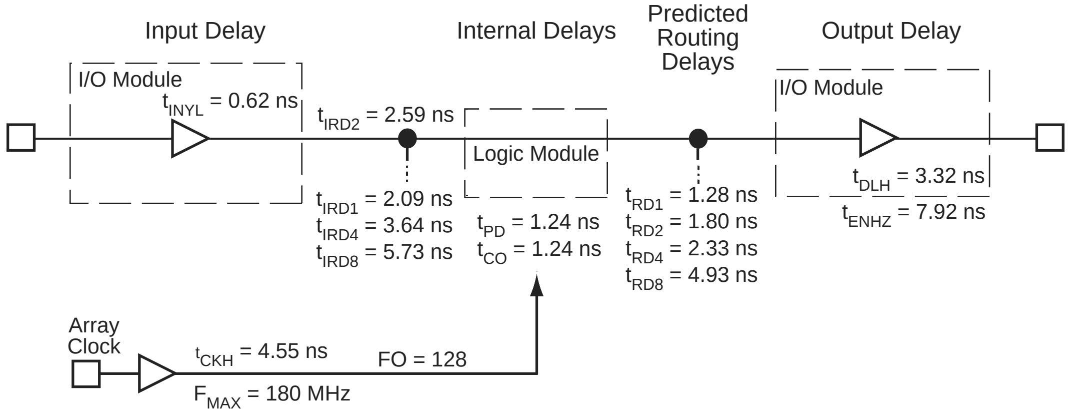
The following is a summary of the changes in revision 6.0 of this document.

- The Ease of Integration, page 1 was updated
- The Temperature Grade Offerings, page 5 is new
- The Speed Grade Offerings, page 5 is new
- The General Description, page 6 was updated
- The MultiPlex I/O Modules, page 11 was updated
- The User Security, page 12 was updated
- Table 6, page 13 was updated
- The Power Dissipation, page 14 was updated.
- The Static Power Component, page 14 was updated
- The Equivalent Capacitance, page 15 was updated
- Figure 13, page 17 was updated
- Table 10, page 18 was updated.
- Figure 14, page 18 was updated.
- Table 11, page 19 was updated.

3.10 Timing Models

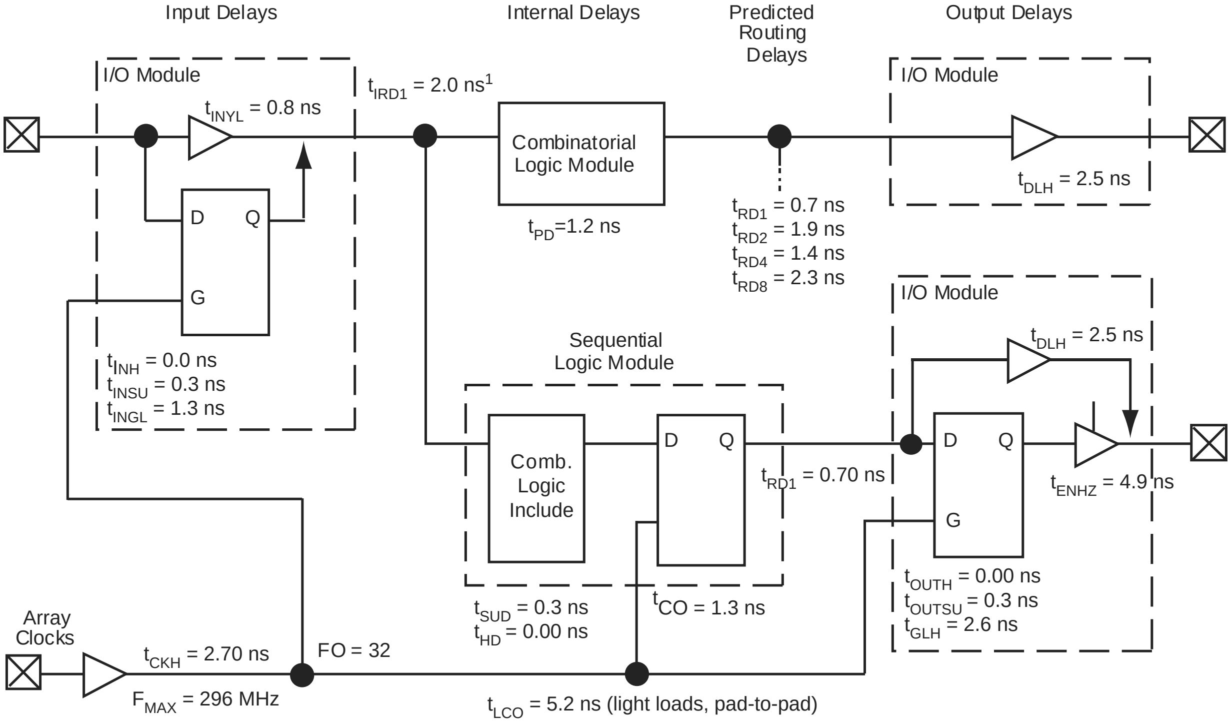
The following figures show various timing models.

Figure 17 • **40MX Timing Model***



Note: Values are shown for 40MX –3 speed devices at 5.0 V worst-case commercial conditions.

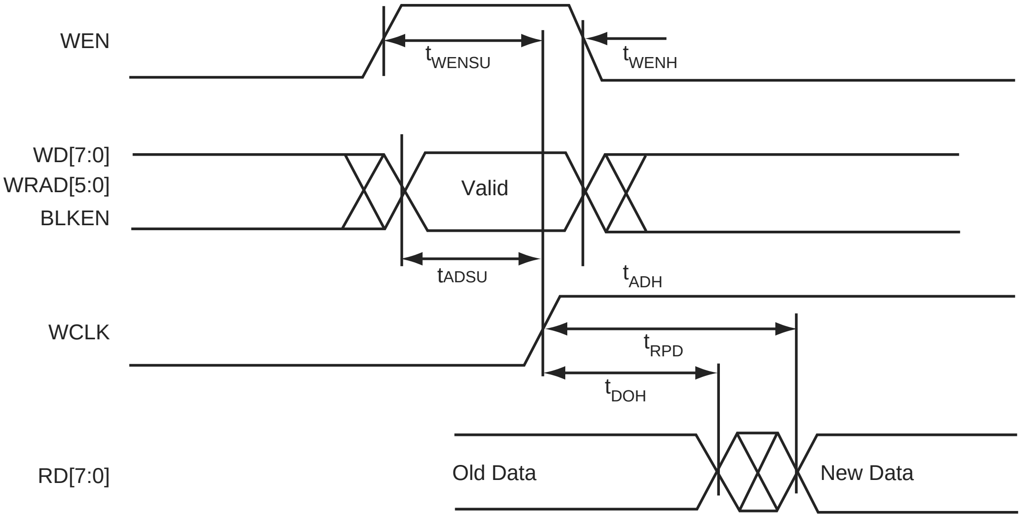
Figure 18 • **42MX Timing Model**



Note: 1. Input module predicted routing delay

Note: 2. Values are shown for A42MX09 –3 at 5.0 V worst-case commercial conditions.

Figure 33 • **42MX SRAM Asynchronous Read Operation—Type 2 (Write Address Controlled)**



3.10.7 Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution, which is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi’s patented antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 µm lithography, offer nominal levels of 100 Ω resistance and 7.0 fF capacitance per antifuse.

MX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90 percent of interconnects using only two antifuses.

3.11 Timing Characteristics

Device timing characteristics fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all MX devices. Internal routing delays are device-dependent; actual delays are not determined until after place-and-route of the user's design is complete. Delay values may then be determined by using the Designer software utility or by performing simulation with post-layout delays.

3.11.1 Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment in Microsemi's Designer software prior to placement and routing. Up to 6% of the nets in a design may be designated as critical.

3.11.2 Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks add

Table 37 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Input Module Predicted Routing Delays1													
t_{IRD1}	FO = 1 Routing Delay			2.9		3.3		3.8		4.5		6.3	ns
t_{IRD2}	FO = 2 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t_{IRD3}	FO = 3 Routing Delay			4.4		5.0		5.7		6.7		9.4	ns
t_{IRD4}	FO = 4 Routing Delay			5.1		5.9		6.7		7.8		11.0	ns
t_{IRD8}	FO = 8 Routing Delay			8.0		9.3		10.5		12.4		17.2	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 16 FO = 128		6.4 6.4		7.4 7.4		8.4 8.4		9.9 9.9		13.8 13.8	ns
t_{CKL}	Input HIGH to LOW	FO = 16 FO = 128		6.8 6.8		7.8 7.8		8.9 8.9		10.4 10.4		14.6 14.6	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 16 FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 16 FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t_{CKSW}	Maximum Skew	FO = 16 FO = 128		0.6 0.8		0.6 0.9		0.7 1.0		0.8 1.2		1.2 1.6	ns
t_P	Minimum Period	FO = 16 FO = 128	6.5 6.8		7.5 7.8		8.5 8.9		10.1 10.4		14.1 14.6		ns
f_{MAX}	Maximum Frequency	FO = 16 FO = 128		113 109		105 101		96 92		83 80		50 48	MHz
TTL Output Module Timing[4]													
t_{DLH}	Data-to-Pad HIGH			4.7		5.4		6.1		7.2		10.0	ns
t_{DHL}	Data-to-Pad LOW			5.6		6.4		7.3		8.6		12.0	ns
t_{ENZH}	Enable Pad Z to HIGH			5.2		6.0		6.9		8.1		11.3	ns
t_{ENZL}	Enable Pad Z to LOW			6.6		7.6		8.6		10.1		14.1	ns
t_{ENHZ}	Enable Pad HIGH to Z			11.1		12.8		14.5		17.1		23.9	ns
t_{ENLZ}	Enable Pad LOW to Z			8.2		9.5		10.7		12.6		17.7	ns
d_{TLH}	Delta LOW to HIGH			0.03		0.03		0.04		0.04		0.06	ns/pF
d_{THL}	Delta HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF

Table 38 • **A42MX09 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			1.0		1.2		1.3		1.6		2.2	ns
t_{INYL}	Pad-to-Y LOW			0.8		0.9		1.0		1.2		1.7	ns
t_{INGH}	G to Y HIGH			1.3		1.4		1.6		1.9		2.7	ns
t_{INGL}	G to Y LOW			1.3		1.4		1.6		1.9		2.7	ns
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			2.0		2.2		2.5		3.0		4.2	ns
t_{IRD2}	FO = 2 Routing Delay			2.3		2.5		2.9		3.4		4.7	ns
t_{IRD3}	FO = 3 Routing Delay			2.5		2.8		3.2		3.7		5.2	ns
t_{IRD4}	FO = 4 Routing Delay			2.8		3.1		3.5		4.1		5.7	ns
t_{IRD8}	FO = 8 Routing Delay			3.7		4.1		4.7		5.5		7.7	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		2.4		2.7		3.0		3.6		5.0	ns
		FO = 256		2.7		3.0		3.4		4.0		5.5	ns
t_{CKL}	Input HIGH to LOW	FO = 32		3.5		3.9		4.4		5.2		7.3	ns
		FO = 256		3.9		4.3		4.9		5.7		8.0	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t_{CKSW}	Maximum Skew	FO = 32		0.3		0.3		0.4		0.5		0.6	ns
		FO = 256		0.3		0.3		0.4		0.5		0.6	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	2.3		2.6		3.0		3.5		4.9		ns
		FO = 256	2.2		2.4		3.3		3.9		5.5		ns
t_P	Minimum Period	FO = 32	3.4		3.7		4.0		4.7		7.8		ns
		FO = 256	3.7		4.1		4.5		5.2		8.6		ns
f_{MAX}	Maximum Frequency	FO = 32		296		269		247		215		129	MHz
		FO = 256		268		244		224		195		117	MHz

Table 42 • **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		**–3 Speed**		**–2 Speed**		**–1 Speed**		**Std Speed**		**–F Speed**		
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays												
t_{INPY}	Input Data Pad-to-Y		1.0		1.1		1.3		1.5		2.1	ns
t_{INGO}	Input Latch Gate-to-Output		1.3		1.4		1.6		1.9		2.6	ns
t_{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{ILA}	Latch Active Pulse Width	4.7		5.2		5.9		6.9		9.7		ns

Table 42 • **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description			**–3 Speed**		**–2 Speed**		**–1 Speed**		**Std Speed**		**–F Speed**		
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			1.8		2.0		2.3		2.7		3.8	ns
t_{IRD2}	FO = 2 Routing Delay			2.1		2.3		2.6		3.1		4.3	ns
t_{IRD3}	FO = 3 Routing Delay			2.3		2.5		2.9		3.4		4.8	ns
t_{IRD4}	FO = 4 Routing Delay			2.5		2.8		3.2		3.7		5.2	ns
t_{IRD8}	FO = 8 Routing Delay			3.4		3.8		4.3		5.1		7.1	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		2.6		2.9		3.3		3.9		5.4	ns
		FO = 486		2.9		3.2		3.6		4.3		5.9	ns
t_{CKL}	Input HIGH to LOW	FO = 32		3.7		4.1		4.6		5.4		7.6	ns
		FO = 486		4.3		4.7		5.4		6.3		8.8	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	2.2		2.4		2.7		3.2		4.5		ns
		FO = 486	2.4		2.6		3.0		3.5		4.9		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	2.2		2.4		2.7		3.2		4.5		ns
		FO = 486	2.4		2.6		3.0		3.5		4.9		ns
t_{CKSW}	Maximum Skew	FO = 32		0.5		0.6		0.7		0.8		1.1	ns
		FO = 486		0.5		0.6		0.7		0.8		1.1	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 486	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	2.8		3.1		3.5		4.1		5.7		ns
		FO = 486	3.3		3.7		4.2		4.9		6.9		ns
t_P	Minimum Period ($1/f_{MAX}$)	FO = 32	4.7		5.2		5.7		6.5		10.9		ns
		FO = 486	5.1		5.7		6.2		7.1		11.9		ns

Table 44 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		**–3 Speed**		**–2 Speed**		**–1 Speed**		**Std Speed**		**–F Speed**		
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Combinatorial Functions[1]												
t_{PD}	Internal Array Module Delay		1.3		1.5		1.7		2.0		2.7	ns
t_{PDD}	Internal Decode Module Delay		1.6		1.8		2.0		2.4		3.3	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.2		1.4		2.0	ns
t_{RD2}	FO = 2 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t_{RD3}	FO =3 Routing Delay		1.6		1.8		2.0		2.4		3.4	ns
t_{RD4}	FO = 4 Routing Delay		2.0		2.2		2.5		2.9		4.1	ns
t_{RD5}	FO = 8 Routing Delay		3.3		3.7		4.2		4.9		6.9	ns
t_{RDD}	Decode-to-Output Routing Delay		0.3		0.4		0.4		0.5		0.7	ns
Logic Module Sequential Timing[3, 4]												
t_{CO}	Flip-Flop Clock-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch Gate-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t_{SUD}	Flip-Flop (Latch) Set-Up Time	0.3		0.3		0.4		0.5		0.7		ns
t_{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		1.6		1.7		2.0		2.3		3.2	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.5		6.4		9.0		ns
Synchronous SRAM Operations												
t_{RC}	Read Cycle Time	6.8		7.5		8.5		10.0		14.0		ns
t_{WC}	Write Cycle Time	6.8		7.5		8.5		10.0		14.0		ns
t_{RCKHL}	Clock HIGH/LOW Time	3.4		3.8		4.3		5.0		7.0		ns
t_{RCO}	Data Valid After Clock HIGH/LOW		3.4		3.8		4.3		5.0		7.0	ns
t_{ADSU}	Address/Data Set-Up Time	1.6		1.8		2.0		2.4		3.4		ns
Synchronous SRAM Operations (continued)												
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Set-Up	0.6		0.7		0.8		0.9		1.3		ns
t_{RENH}	Read Enable Hold	3.4		3.8		4.3		5.0		7.0		ns
t_{WENSU}	Write Enable Set-Up	2.7		3.0		3.4		4.0		5.6		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Set-Up	2.8		3.1		3.5		4.1		5.7		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		ns

Table 49 • **PL84**

PL84				
Pin Number	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
10	I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O
11	I/O	I/O	I/O	I/O
12	NC	MODE	MODE	MODE
13	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	I/O	I/O	I/O	I/O
18	GND	I/O	I/O	I/O
19	GND	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	VCCA	VCCI	VCCI
23	I/O	VCCI	VCCA	VCCA
24	I/O	I/O	I/O	I/O
25	VCC	I/O	I/O	I/O
26	VCC	I/O	I/O	I/O
27	I/O	I/O	I/O	I/O
28	I/O	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	I/O	I/O	I/O	I/O
31	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	VCC	I/O	I/O	I/O
34	I/O	I/O	I/O	TMS, I/O
35	I/O	I/O	I/O	TDI, I/O
36	I/O	I/O	I/O	WD, I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	WD, I/O
39	I/O	I/O	I/O	WD, I/O
40	GND	I/O	I/O	I/O
41	I/O	I/O	I/O	I/O
42	I/O	I/O	I/O	I/O
43	I/O	VCCA	VCCA	VCCA
44	I/O	I/O	I/O	WD, I/O
45	I/O	I/O	I/O	WD, I/O
46	VCC	I/O	I/O	WD, I/O

Table 50 • **PQ 100**

PQ100				
Pin Number	**A40MX02 Function**	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**
19	VCC	V_{CC}	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	GND	GND
23	I/O	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	I/O	I/O	I/O	I/O
26	I/O	I/O	I/O	I/O
27	NC	NC	I/O	I/O
28	NC	NC	I/O	I/O
29	NC	NC	I/O	I/O
30	NC	NC	I/O	I/O
31	NC	I/O	I/O	I/O
32	NC	I/O	I/O	I/O
33	NC	I/O	I/O	I/O
34	I/O	I/O	GND	GND
35	I/O	I/O	I/O	I/O
36	GND	GND	I/O	I/O
37	GND	GND	I/O	I/O
38	I/O	I/O	I/O	I/O
39	I/O	I/O	I/O	I/O
40	I/O	I/O	VCCA	VCCA
41	I/O	I/O	I/O	I/O
42	I/O	I/O	I/O	I/O
43	VCC	VCC	I/O	I/O
44	VCC	VCC	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	GND	GND
47	I/O	I/O	I/O	I/O
48	NC	I/O	I/O	I/O
49	NC	I/O	I/O	I/O
50	NC	I/O	I/O	I/O
51	NC	NC	I/O	I/O
52	NC	NC	SDO, I/O	SDO, I/O
53	NC	NC	I/O	I/O
54	NC	NC	I/O	I/O
55	NC	NC	I/O	I/O

Table 52 • **PQ160**

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
95	I/O	I/O	I/O
96	I/O	I/O	WD, I/O
97	I/O	I/O	I/O
98	VCCA	VCCA	VCCA
99	GND	GND	GND
100	NC	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	NC	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	WD, I/O
107	I/O	I/O	WD, I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	NC	I/O	I/O
111	I/O	I/O	WD, I/O
112	I/O	I/O	WD, I/O
113	I/O	I/O	I/O
114	NC	VCCI	VCCI
115	I/O	I/O	WD, I/O
116	NC	I/O	WD, I/O
117	I/O	I/O	I/O
118	I/O	I/O	TDI, I/O
119	I/O	I/O	TMS, I/O
120	GND	GND	GND
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	NC	I/O	I/O
125	GND	GND	GND
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	NC	I/O	I/O
130	GND	GND	GND
131	I/O	I/O	I/O

Table 52 • **PQ160**

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	VCCA	VCCA
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	VCCA	VCCA
139	VCCI	VCCI	VCCI
140	GND	GND	GND
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	GND	GND	GND
146	NC	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	NC	VCCA	VCCA
151	NC	I/O	I/O
152	NC	I/O	I/O
153	NC	I/O	I/O
154	NC	I/O	I/O
155	GND	GND	GND
156	I/O	I/O	I/O
157	I/O	I/O	I/O
158	I/O	I/O	I/O
159	MODE	MODE	MODE
160	GND	GND	GND

Table 56 • **VQ100**

VQ100		
Pin Number	**A42MX09 Function**	**A42MX16 Function**
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	LP	LP
63	VCCA	VCCA
64	VCCI	VCCI
65	VCCA	VCCA
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	GND	GND
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	SDI, I/O	SDI, I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	GND	GND
83	I/O	I/O
84	I/O	I/O
85	PRA, I/O	PRA, I/O
86	I/O	I/O
87	CLKA, I/O	CLKA, I/O
88	VCCA	VCCA
89	I/O	I/O
90	CLKB, I/O	CLKB, I/O
91	I/O	I/O
92	PRB, I/O	PRB, I/O

Table 56 • **VQ100**

VQ100		
Pin Number	**A42MX09 Function**	**A42MX16 Function**
93	I/O	I/O
94	GND	GND
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	DCLK, I/O	DCLK, I/O

Figure 48 • **TQ176**

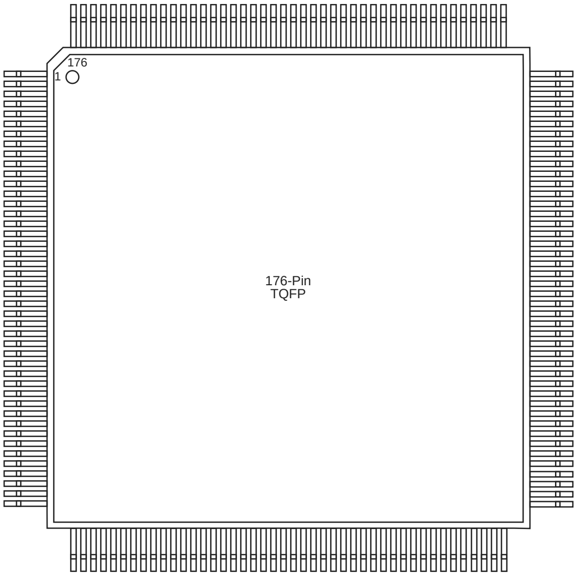


Table 57 • **TQ176**

TQ176			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
1	GND	GND	GND
2	MODE	MODE	MODE
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	NC	NC	I/O
9	I/O	I/O	I/O

Table 58 • **CQ208**

CQ208	
Pin Number	**A42MX36 Function**
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	GND
53	GND
54	TMS, I/O
55	TDI, I/O
56	I/O
57	WD, I/O
58	WD, I/O
59	I/O
60	VCCI
61	I/O
62	I/O
63	I/O
64	I/O
65	QCLKA, I/O
66	WD, I/O
67	WD, I/O
68	I/O
69	I/O
70	WD, I/O
71	WD, I/O
72	I/O
73	I/O

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
22	I/O
23	I/O
24	I/O
25	I/O
26	VCCA
27	I/O
28	I/O
29	VCCA
30	VCCI
31	GND
32	VCCA
33	LP
34	TCK, I/O
35	I/O
36	GND
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	GND
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
59	I/O
60	VCCA
61	GND
62	GND
63	NC
64	NC
65	NC
66	I/O
67	SDO, TDO, I/O
68	I/O
69	WD, I/O
70	WD, I/O
71	I/O
72	VCCI
73	I/O
74	I/O
75	I/O
76	WD, I/O
77	GND
78	WD, I/O
79	I/O
80	QCLKB, I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	WD, I/O
88	WD, I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	VCCI

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
244	WD, I/O
245	I/O
246	I/O
247	I/O
248	VCCI
249	I/O
250	WD, I/O
251	WD, I/O
252	I/O
253	SDI, I/O
254	I/O
255	GND
256	NC

Figure 51 • **BG272**

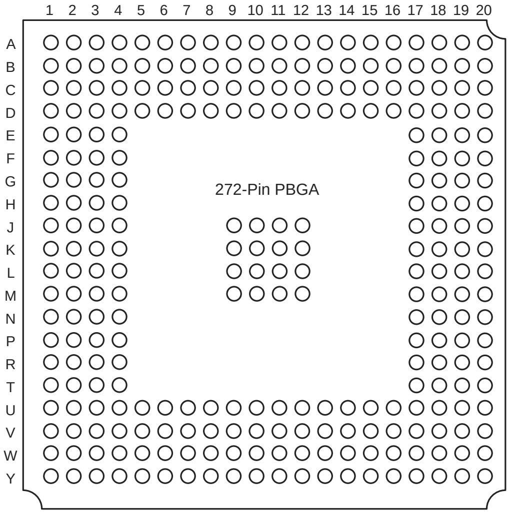


Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
A1	GND
A2	GND
A3	I/O
A4	WD, I/O
A5	I/O

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
M10	GND
M11	GND
M12	GND
M17	I/O
M18	I/O
M19	I/O
M20	I/O
N1	I/O
N2	I/O
N3	I/O
N4	VCCI
N17	VCCI
N18	I/O
N19	I/O
N20	I/O
P1	I/O
P2	I/O
P3	I/O
P4	VCCA
P17	I/O
P18	I/O
P19	I/O
P20	I/O
R1	I/O
R2	I/O
R3	I/O
R4	VCCI
R17	VCCI
R18	I/O
R19	I/O
R20	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T17	VCCA
T18	I/O