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**Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

**Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 72 |
| Number of Gates | 14000 |
| Voltage - Supply | 3V ~ 3.6V, 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -55°C ~ 125°C (TC) |
| Package / Case | 84-LCC (J-Lead) |
| Supplier Device Package | 84-PLCC (29.31x29.31) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a42mx09-pl84m |

# 3        40MX and 42MX FPGAs

## 3.1        General Description

Microsemi's 40MX and 42MX families offer a cost-effective design solution at 5V. The MX devices are single-chip solutions and provide high performance while shortening the system design and development cycle. MX devices can integrate and consolidate logic implemented in multiple PALs, CPLDs, and FPGAs. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

The MX device architecture is based on Microsemi's patented antifuse technology implemented in a 0.45µm triple-metal CMOS process. With capacities ranging from 3,000 to 54,000 system gates, the MX devices provide performance up to 250 MHz, are live on power-up and have one-fifth the standby power consumption of comparable FPGAs. MX FPGAs provide up to 202 user I/Os and are available in a wide variety of packages and speed grades.

A42MX24 and A42MX36 devices also feature multiPlex I/Os, which support mixed-voltage systems, enable programmable PCI, deliver high-performance operation at both 5.0V and 3.3V, and provide a low-power mode. The devices are fully compliant with the PCI local bus specification (version 2.1). They deliver 200 MHz on-chip operation and 6.1 ns clock-to-output performance.

The 42MX24 and 42MX36 devices include system-level features such as IEEE Standard 1149.1 (JTAG) Boundary Scan Testing and fast wide-decode modules. In addition, the A42MX36 device offers dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The storage elements can efficiently address applications requiring wide data path manipulation and can perform transformation functions such as those required for telecommunications, networking, and DSP.

All MX devices are fully tested over automotive and military temperature ranges. In addition, the largest member of the family, the A42MX36, is available in both CQ208 and CQ256 ceramic packages screened to MIL-STD-883 levels. For easy prototyping and conversion from plastic to ceramic, the CQ208 and PQ208 devices are pin-compatible.
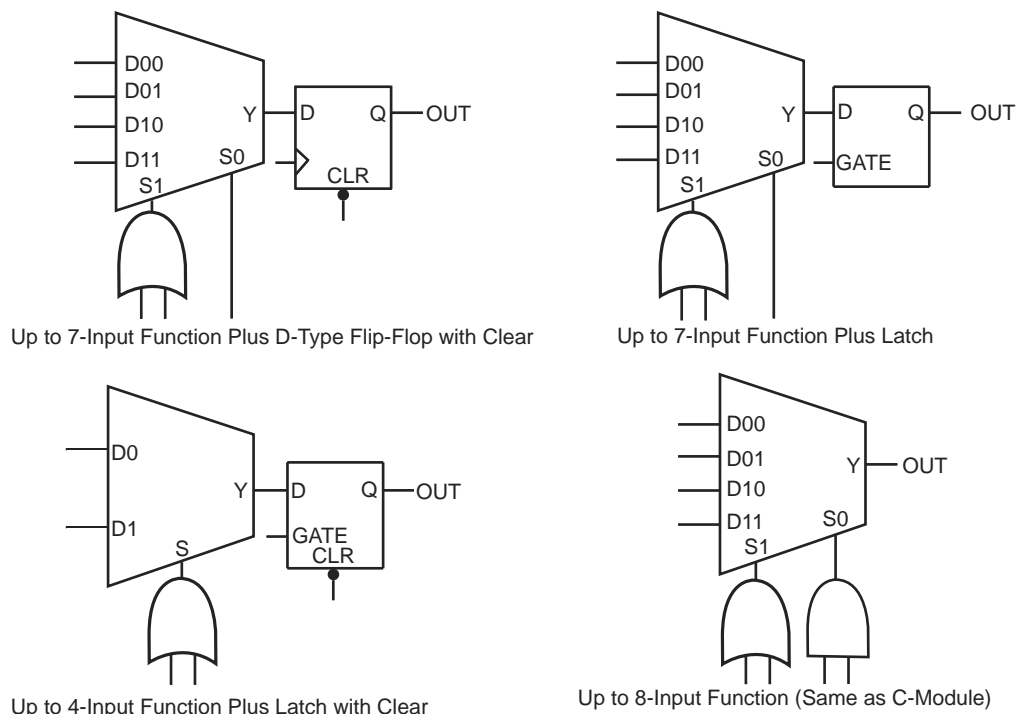
## 3.2        MX Architectural Overview

The MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within these families are composed of logic modules, I/O modules, routing resources and clock networks, which are the building blocks for fast logic designs. In addition, the A42MX36 device contains embedded dual-port SRAM modules, which are optimized for high-speed data path functions such as FIFOs, LIFOs and scratch pad memory. A42MX24 and A42MX36 also contain wide-decode modules.

### 3.2.1        Logic Modules

The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources.(see the following figure).

The logic module can implement the four basic logic functions (NAND, AND, OR and NOR) in gates of two, three, or four inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array; latches and flip-flops can be constructed from logic modules whenever required in the application.

*Figure 4 •*  **42MX S-Module Implementation**



Up to 7-Input Function Plus D-Type Flip-Flop with Clear

Up to 7-Input Function Plus Latch

Up to 4-Input Function Plus Latch with Clear

Up to 8-Input Function (Same as C-Module)

A42MX24 and A42MX36 devices contain D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry, providing a fast, wide-input AND function similar to that found in CPLD architectures (Figure 5, page 9). The D-module allows A42MX24 and A42MX36 devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin, and can also be fed back into the array to be incorporated into other logic.

## 3.2.2    **Dual-Port SRAM Modules**

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the A42MX36 dual-port SRAM block is shown in Figure 6, page 9.

The A42MX36 SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]), which are connected to segmented vertical routing tracks.

The A42MX36 dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring FIFO and LIFO queues. The ACTgen Macro Builder within Microsemi's designer software provides capability to quickly design memory functions with the SRAM blocks. Unused SRAM blocks can be used to implement registers for other user logic within the design.

*Figure 8 •*   **Clock Networks of 42MX Devices**
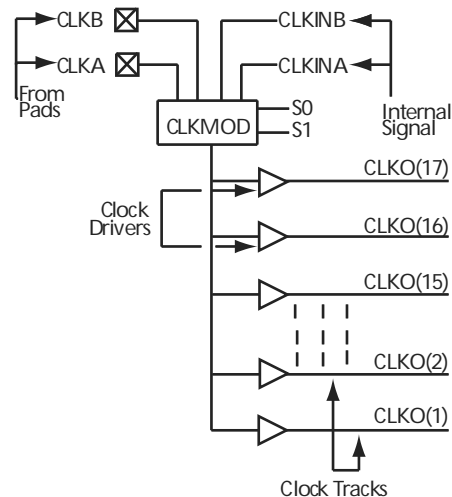


*Figure 9 •*   **Quadrant Clock Network of A42MX36 Devices**
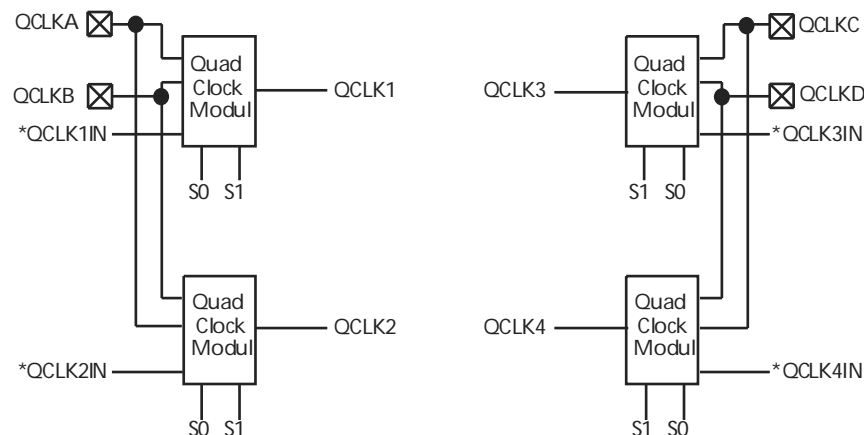


**Note:**  *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

## 3.2.5    MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 10, page 12 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (See the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 10, page 12). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. See the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 μA.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 11, page 12). When the PCI fuse is not programmed, the output drive is standard.

Silicon Sculptor programs devices independently to achieve the fastest programming times possible. After being programmed, each fuse is verified to insure that it has been programmed correctly. Furthermore, at the end of programming, there are integrity tests that are run to ensure no extra fuses have been programmed. Not only does it test fuses (both programmed and non-programmed), Silicon Sculptor also allows self-test to verify its own hardware extensively.

The procedure for programming an MX device using Silicon Sculptor is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via In-House Programming from the factory.

For more details on programming MX devices, see the *AC225: Programming Antifuse Devices* application note and the *Silicon Sculptor 3 Programmers User Guide*.

### 3.3.4 Power Supply

MX devices are designed to operate in both 5.0V and 3.3V environments. In particular, 42MX devices can operate in mixed 5.0 V/3.3 V systems. The following table describes the voltage support of MX devices.

*Table 6 •* **Voltage Support of MX Devices**

| Device | VCC | VCCA | VCCI | Maximum Input Tolerance | Nominal Output Voltage |
|--------|-------|-------|-------|-------------------------|------------------------|
| 40MX | 5.0 V | – | – | 5.5 V | 5.0 V |
| | 3.3 V | – | – | 3.6 V | 3.3 V |
| 42MX | – | 5.0 V | 5.0 V | 5.5 V | 5.0 V |
| | – | 3.3 V | 3.3 V | 3.6 V | 3.3 V |
| | – | 5.0 V | 3.3 V | 5.5 V | 3.3 V |

For A42MX24 and A42MX36 devices the VCCA supply has to be monotonic during power up in order for the POR to issue reset to the JTAG state machine correctly. For more information, see the *AC291: 42MX Family Devices Power-Up Behavior*.

### 3.3.5 Power-Up/Down in Mixed-Voltage Mode

When powering up 42MX in mixed voltage mode (VCCA = 5.0 V and VCCI = 3.3 V), VCCA must be greater than or equal to VCCI throughout the power-up sequence. If VCCI exceeds VCCA during power-up, one of two things will happen:

• The input protection diode on the I/Os will be forward biased
• The I/Os will be at logical High

In either case, ICC rises to high levels. For power-down, any sequence with VCCA and VCCI can be implemented.

### 3.3.6 Transient Current

Due to the simultaneous random logic switching activity during power-up, a transient current may appear on the core supply (VCC). Customers must use a regulator for the VCC supply that can source a minimum of 100 mA for transient current during power-up. Failure to provide enough power can prevent the system from powering up properly and result in functional failure. However, there are no reliability concerns, since transient current is distributed across the die instead of confined to a localized spot.

Since the transient current is not due to I/O switching, its value and duration are independent of the VCCI.

3. All outputs unloaded. All inputs = VCC/VCCI or GND

# 3.8    3.3 V Operating Conditions

The following table shows 3.3 V operating conditions.

*Table 16 •*    **Absolute Maximum Ratings for 40MX Devices\***

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCC | DC Supply Voltage | −0.5 to +7.0 | V |
| VI | Input Voltage | −0.5 to VCC + 0.5 | V |
| VO | Output Voltage | −0.5 to VCC + 0.5 | V |
| $t_{STG}$ | Storage Temperature | −65 to + 150 | °C |

**Note:**  \*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

*Table 17 •*    **Absolute Maximum Ratings for 42MX Devices\***

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCCI | DC Supply Voltage for I/Os | −0.5 to +7.0 | V |
| VCCA | DC Supply Voltage for Array | −0.5 to +7.0 | V |
| VI | Input Voltage | −0.5 to VCCI+0.5 | V |
| VO | Output Voltage | −0.5 to VCCI+0.5 | V |
| $t_{STG}$ | Storage Temperature | −65 to +150 | °C |

**Note:**  \*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

*Table 18 •*    **Recommended Operating Conditions**

| Parameter | Commercial | Industrial | Military | Units |
|---|---|---|---|---|
| Temperature Range\* | 0 to +70 | −40 to +85 | −55 to +125 | °C |
| VCC (40MX) | 3.0 to 3.6 | 3.0 to 3.6 | 3.0 to 3.6 | V |
| VCCA (42MX) | 3.0 to 3.6 | 3.0 to 3.6 | 3.0 to 3.6 | V |
| VCCI (42MX) | 3.0 to 3.6 | 3.0 to 3.6 | 3.0 to 3.6 | V |

**Note:**  \*Ambient temperature ($T_A$) is used for commercial and industrial grades; case temperature ($T_C$) is used for military grades.

All the following tables show various specifications and operating conditions of 40MX and 42MX FPGAs.

### 3.9.1 Mixed 5.0V/3.3V Electrical Specifications

*Table 22 •* **Mixed 5.0V/3.3V Electrical Specifications**

| Symbol | Parameter | Commercial Min. | Commercial Max. | Commercial –F Min. | Commercial –F Max. | Industrial Min. | Industrial Max. | Military Min. | Military Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| VOH[1] | IOH = −10 mA | 2.4 | | 2.4 | | | | | | V |
| | IOH = −4 mA | | | | | 2.4 | | 2.4 | | V |
| VOL[1] | IOL = 10 mA | | 0.5 | | 0.5 | | | | | V |
| | IOL = 6 mA | | | | | | 0.4 | | 0.4 | V |
| VIL | | −0.3 | 0.8 | −0.3 | 0.8 | −0.3 | 0.8 | −0.3 | 0.8 | V |
| VIH[2] | | 2.0 | VCCA + 0.3 | 2.0 | VCCA + 0.3 | 2.0 | VCCA + 0.3 | 2.0 | VCCA + 0.3 | V |
| IL | VIN = 0.5 V | | −10 | | −10 | | −10 | | −10 | µA |
| IH | VIN = 2.7 V | | −10 | | −10 | | −10 | | −10 | µA |
| Input Transition Time, $T_R$ and $T_F$ | | | 500 | | 500 | | 500 | | 500 | ns |
| $C_{IO}$ I/O Capacitance | | | 10 | | 10 | | 10 | | 10 | pF |
| Standby Current, ICC[3] | A42MX09 | 5 | 25 | | 25 | | 25 | | 25 | mA |
| | A42MX16 | 6 | 25 | | 25 | | 25 | | 25 | mA |
| | A42MX24, A42MX36 | 20 | 25 | | 25 | | 25 | | 25 | mA |
| Low Power Mode Standby Current | | | 0.5 | | ICC – 5.0 | | ICC – 5.0 | | ICC – 5.0 | mA |
| IIO I/O source sink current | Can be derived from the *IBIS model* (http://www.microsemi.com/soc/techdocs/models/ibis.html) | | | | | | | | | |

1. Only one output tested at a time. VCCI = min.
2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
3. All outputs unloaded. All inputs = VCCI or GND

### 3.9.2 Output Drive Characteristics for 5.0 V PCI Signaling

MX PCI device I/O drivers were designed specifically for high-performance PCI systems. Figure 16, page 28 shows the typical output drive characteristics of the MX devices. MX output drivers are compliant with the PCI Local Bus Specification.

*Table 23 •* **DC Specification (5.0 V PCI Signaling)[1]**

| Symbol | Parameter | Condition | PCI Min. | PCI Max. | MX Min. | MX Max. | Units |
|---|---|---|---|---|---|---|---|
| VCCI | Supply Voltage for I/Os | | 4.75 | 5.25 | 4.75 | 5.25[2] | V |
| VIH[3] | Input High Voltage | | 2.0 | VCC + 0.5 | 2.0 | VCCI + 0.3 | V |
| VIL | Input Low Voltage | | −0.5 | 0.8 | −0.3 | 0.8 | V |
| IIH | Input High Leakage Current | VIN = 2.7 V | | 70 | — | 10 | µA |
| IIL | Input Low Leakage Current | VIN=0.5 V | | −70 | — | −10 | µA |
| VOH | Output High Voltage | IOUT = −2 mA IOUT = −6 mA | 2.4 | | 3.84 | | V |
| VOL | Output Low Voltage | IOUT = 3 mA, 6 mA | 0.55 | — | 0.33 | | V |

*Figure 30 •* **42MX SRAM Write Operation**
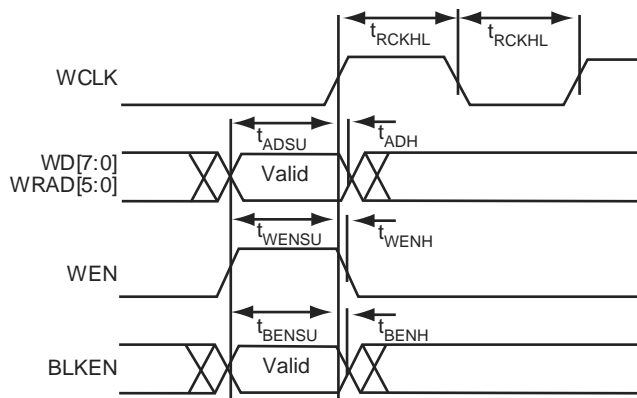


**Note:** Identical timing for falling edge clock

*Figure 31 •* **42MX SRAM Synchronous Read Operation**
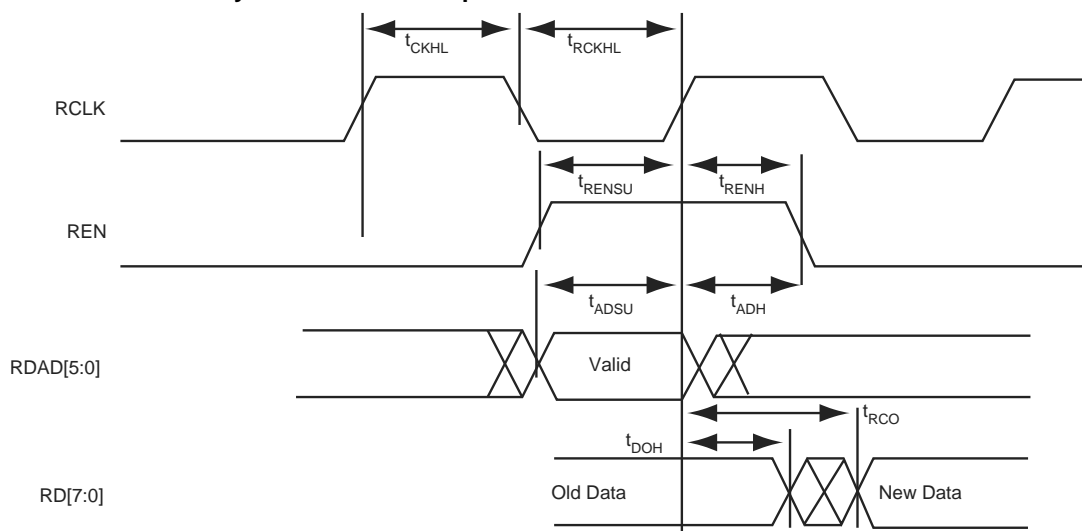


**Note:** Identical timing for falling edge clock

*Figure 32 •* **42MX SRAM Asynchronous Read Operation—Type 1 (Read Address Controlled)**

***Table 40 •*** **A42MX16 Timing Characteristics (Nominal 5.0 V Operation)** *(continued)***(Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)**

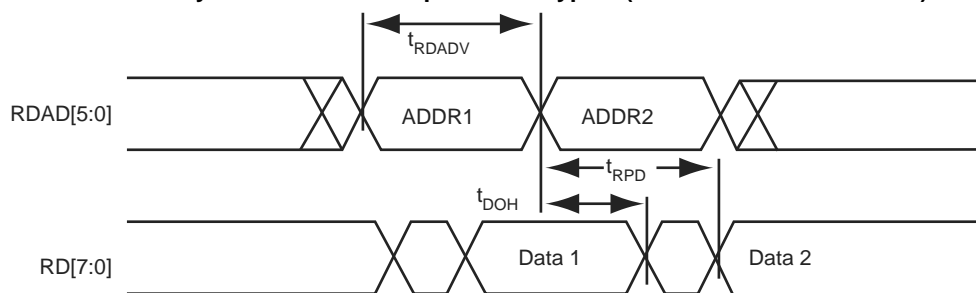| Parameter / Description | | –3 Speed Min. | Max. | –2 Speed Min. | Max. | –1 Speed Min. | Max. | Std Speed Min. | Max. | –F Speed Min. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| t$_{RD3}$ | FO = 3 Routing Delay | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| t$_{RD4}$ | FO = 4 Routing Delay | | 1.6 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | ns |
| t$_{RD8}$ | FO = 8 Routing Delay | | 2.6 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| **Logic Module Sequential Timing[3,4]** | | | | | | | | | | | | |
| t$_{SUD}$ | Flip-Flop (Latch) Data Input Set-Up | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| t$_{HD}$ | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t$_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| t$_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t$_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.1 | | ns |
| t$_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.5 | | 5.0 | | 5.6 | | 6.6 | | 9.2 | | ns |
| t$_A$ | Flip-Flop Clock Input Period | 6.8 | | 7.6 | | 8.6 | | 10.1 | | 14.1 | | ns |
| t$_{INH}$ | Input Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t$_{INSU}$ | Input Buffer Latch Set-Up | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | | ns |
| t$_{OUTH}$ | Output Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t$_{OUTSU}$ | Output Buffer Latch Set-Up | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | | ns |
| f$_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 215 | | 195 | | 179 | | 156 | | 94 | MHz |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| t$_{INYH}$ | Pad-to-Y HIGH | | 1.1 | | 1.2 | | 1.3 | | 1.6 | | 2.2 | ns |
| t$_{INYL}$ | Pad-to-Y LOW | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| t$_{INGH}$ | G to Y HIGH | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| t$_{INGL}$ | G to Y LOW | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| **Input Module Predicted Routing Delays[2]** | | | | | | | | | | | | |
| t$_{IRD1}$ | FO = 1 Routing Delay | | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 4.0 | ns |
| t$_{IRD2}$ | FO = 2 Routing Delay | | 2.1 | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| t$_{IRD3}$ | FO = 3 Routing Delay | | 2.3 | | 2.6 | | 3.0 | | 3.5 | | 4.9 | ns |
| t$_{IRD4}$ | FO = 4 Routing Delay | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.4 | ns |
| t$_{IRD8}$ | FO = 8 Routing Delay | | 3.6 | | 4.0 | | 4.6 | | 5.4 | | 7.5 | ns |
| **Global Clock Network** | | | | | | | | | | | | |
| t$_{CKH}$ | Input LOW to HIGH   FO = 32<br>FO = 384 | | 2.6<br>2.9 | | 2.9<br>3.2 | | 3.3<br>3.6 | | 3.9<br>4.3 | | 5.4<br>6.0 | ns<br>ns |
| t$_{CKL}$ | Input HIGH to LOW   FO = 32<br>FO = 384 | | 3.8<br>4.5 | | 4.2<br>5.0 | | 4.8<br>5.6 | | 5.6<br>6.6 | | 7.8<br>9.2 | ns<br>ns |
| t$_{PWH}$ | Minimum Pulse Width HIGH   FO = 32<br>FO = 384 | 3.2<br>3.7 | | 3.5<br>4.1 | | 4.0<br>4.6 | | 4.7<br>5.4 | | 6.6<br>7.6 | | ns<br>ns |

***Table 40 •*** **A42MX16 Timing Characteristics (Nominal 5.0 V Operation)** *(continued)*(**Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| t$_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 3.2 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | | ns |
| | | FO = 384 | 3.7 | | 4.1 | | 4.6 | | 5.4 | | 7.6 | | ns |
| t$_{CKSW}$ | Maximum Skew | FO = 32 | | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| | | FO = 384 | | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| t$_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 384 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t$_{HEXT}$ | Input Latch External Hold | FO = 32 | 2.8 | | 3.1 | | 5.5 | | 4.1 | | 5.7 | | ns |
| | | FO = 384 | 3.2 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | | ns |
| t$_P$ | Minimum Period | FO = 32 | 4.2 | | 4.67 | | 5.1 | | 5.8 | | 9.7 | | ns |
| | | FO = 384 | 4.6 | | 5.1 | | 5.6 | | 6.4 | | 10.7 | | ns |
| f$_{MAX}$ | Maximum Frequency | FO = 32 | | 237 | | 215 | | 198 | | 172 | | 103 | MHz |
| | | FO = 384 | | 215 | | 195 | | 179 | | 156 | | 94 | MHz |

**Table 43 •** **A42MX24 Timing Characteristics (Nominal 3.3 V Operation)** *(continued)***(Worst-Case Commercial Conditions, VCCA = 3.0 V,  T$_J$ = 70°C)**

| Parameter / Description | | –3 Speed Min. | –3 Speed Max. | –2 Speed Min. | –2 Speed Max. | –1 Speed Min. | –1 Speed Max. | Std Speed Min. | Std Speed Max. | –F Speed Min. | –F Speed Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Input Module Predicted Routing Delays[2]** | | | | | | | | | | | | |
| t$_{IRD1}$ | FO = 1 Routing Delay | | 2.6 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| t$_{IRD2}$ | FO = 2 Routing Delay | | 2.9 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| t$_{IRD3}$ | FO = 3 Routing Delay | | 3.2 | | 3.6 | | 4.0 | | 4.8 | | 6.6 | ns |
| t$_{IRD4}$ | FO = 4 Routing Delay | | 3.5 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| t$_{IRD8}$ | FO = 8 Routing Delay | | 4.8 | | 5.3 | | 6.1 | | 7.1 | | 10.0 | ns |
| **Global Clock Network** | | | | | | | | | | | | |
| t$_{CKH}$ | Input LOW to HIGH FO = 32 | | 4.4 | | 4.8 | | 5.5 | | 6.5 | | 9.1 | ns |
| | FO = 486 | | 4.8 | | 5.3 | | 6.0 | | 7.1 | | 10.0 | ns |
| t$_{CKL}$ | Input HIGH to LOW FO = 32 | | 5.1 | | 5.7 | | 6.4 | | 7.6 | | 10.6 | ns |
| | FO = 486 | | 6.0 | | 6.6 | | 7.5 | | 8.8 | | 12.4 | ns |
| t$_{PWH}$ | Minimum Pulse FO = 32 | 3.0 | | 3.3 | | 3.8 | | 4.5 | | 6.3 | | ns |
| | Width HIGH FO = 486 | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | | ns |
| t$_{PWL}$ | Minimum Pulse FO = 32 | 3.0 | | 3.4 | | 3.8 | | 4.5 | | 6.3 | | ns |
| | Width LOW FO = 486 | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | | ns |
| t$_{CKSW}$ | Maximum Skew FO = 32 | | 0.8 | | 0.8 | | 1.0 | | 1.1 | | 1.6 | ns |
| | FO = 486 | | 0.8 | | 0.8 | | 1.0 | | 1.1 | | 1.6 | ns |
| t$_{SUEXT}$ | Input Latch External FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | Set-Up FO = 486 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | |
| t$_{DLH}$ | Data-to-Pad HIGH | | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.1 | ns |
| t$_{DHL}$ | Data-to-Pad LOW | | 4.0 | | 4.4 | | 5.0 | | 5.9 | | 8.3 | ns |
| t$_{ENZH}$ | Enable Pad Z to HIGH | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.4 | ns |
| t$_{ENZL}$ | Enable Pad Z to LOW | | 3.9 | | 4.4 | | 5.0 | | 5.8 | | 8.2 | ns |
| t$_{ENHZ}$ | Enable Pad HIGH to Z | | 7.2 | | 8.0 | | 9.1 | | 10.7 | | 14.9 | ns |
| t$_{ENLZ}$ | Enable Pad LOW to Z | | 6.7 | | 7.5 | | 8.5 | | 9.9 | | 13.9 | ns |
| t$_{GLH}$ | G-to-Pad HIGH | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| t$_{GHL}$ | G-to-Pad LOW | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| t$_{LSU}$ | I/O Latch Output Set-Up | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |

Input, output, tristate or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/Os pins are configured by the Designer software as shown in Table 46, page 84.

*Table 46 •*    **Configuration of Unused I/Os**

| Device | Configuration |
|---|---|
| A40MX02, A40MX04 | Pulled LOW |
| A42MX09, A42MX16 | Pulled LOW |
| A42MX24, A42MX36 | Tristated |

In all cases, it is recommended to tie all unused MX I/O pins to LOW on the board. This applies to all dual-purpose pins when configured as I/Os as well.

**LP, Low Power Mode**

Controls the low power mode of all 42MX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation in 200 µs after the LP pin is driven to a logic LOW.

**MODE, Mode**

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). The MODE pin is held HIGH to provide verification capability. The MODE pin should be terminated to GND through a 10kΩ resistor so that the MODE pin can be pulled HIGH when required.

**NC, No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

**PRA, I/O**

**PRB, I/OProbe A/B**

The Probe pin is used to output data from any user-defined design node within the device. Each diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. The Probe pin is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**QCLKA/B/C/D, I/O Quadrant Clock**

Quadrant clock inputs for A42MX36 devices. When not used as a register control signal, these pins can function as user I/Os.

**SDI, I/OSerial Data Input**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**SDO, I/OSerial Data Output**

Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. SDO is available for 42MX devices only.

When Silicon Explorer II is being used, SDO will act as an output while the "checksum" command is run. It will return to user I/O when "checksum" is complete.

**TCK, I/O Test Clock**

Clock signal to shift the Boundary Scan Test (BST) data into the device. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

**TDI, I/OTest Data In**

Serial data input for BST instructions and data. Data is shifted in on the rising edge of TCK. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

**TDO, I/OTest Data Out**

Serial data output for BST instructions and test data. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

**TMS, I/OTest Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI and TDO pins are boundary scan pins. Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications. IEEE JTAG specification recommends a 10kΩ pull-up resistor on the pin. BST pins are only available in A42MX24 and A42MX36 devices.

**VCC, Supply Voltage**

Input supply voltage for 40MX devices

**VCCA, Supply Voltage**

Supply voltage for array in 42MX devices

**VCCI, Supply Voltage**

Supply voltage for I/Os in 42MX devices

**WD, I/OWide Decode Output**

When a wide decode module is used in a 42MX device this pin can be used as a dedicated output from the wide decode module. This direct connection eliminates additional interconnect delays associated with regular logic modules. To implement the direct I/O connection, connect an output buffer of any type to the output of the wide decode macro and place this output on one of the reserved WD pins.

*Table 48 •* **PL68**

| PL68 | | |
|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** |
| 24 | I/O | I/O |
| 25 | VCC | VCC |
| 26 | I/O | I/O |
| 27 | I/O | I/O |
| 28 | I/O | I/O |
| 29 | I/O | I/O |
| 30 | I/O | I/O |
| 31 | I/O | I/O |
| 32 | GND | GND |
| 33 | I/O | I/O |
| 34 | I/O | I/O |
| 35 | I/O | I/O |
| 36 | I/O | I/O |
| 37 | I/O | I/O |
| 38 | VCC | VCC |
| 39 | I/O | I/O |
| 40 | I/O | I/O |
| 41 | I/O | I/O |
| 42 | I/O | I/O |
| 43 | I/O | I/O |
| 44 | I/O | I/O |
| 45 | I/O | I/O |
| 46 | I/O | I/O |
| 47 | I/O | I/O |
| 48 | I/O | I/O |
| 49 | GND | GND |
| 50 | I/O | I/O |
| 51 | I/O | I/O |
| 52 | CLK, I/O | CLK, I/O |
| 53 | I/O | I/O |
| 54 | MODE | MODE |
| 55 | VCC | VCC |
| 56 | SDI, I/O | SDI, I/O |
| 57 | DCLK, I/O | DCLK, I/O |
| 58 | PRA, I/O | PRA, I/O |
| 59 | PRB, I/O | PRB, I/O |
| 60 | I/O | I/O |

*Table 52 •* **PQ160**

| PQ160 | | | |
| --- | --- | --- | --- |
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 21 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 22 | I/O | I/O | I/O |
| 23 | PRA, I/O | PRA, I/O | PRA, I/O |
| 24 | NC | I/O | WD, I/O |
| 25 | I/O | I/O | WD, I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | NC | I/O | I/O |
| 29 | I/O | I/O | WD, I/O |
| 30 | GND | GND | GND |
| 31 | NC | I/O | WD, I/O |
| 32 | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O |
| 35 | NC | VCCI | VCCI |
| 36 | I/O | I/O | WD, I/O |
| 37 | I/O | I/O | WD, I/O |
| 38 | SDI, I/O | SDI, I/O | SDI, I/O |
| 39 | I/O | I/O | I/O |
| 40 | GND | GND | GND |
| 41 | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | GND | GND | GND |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | GND | GND | GND |
| 50 | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O |
| 52 | NC | I/O | I/O |
| 53 | I/O | I/O | I/O |
| 54 | NC | VCCA | VCCA |
| 55 | I/O | I/O | I/O |
| 56 | I/O | I/O | I/O |
| 57 | VCCA | VCCA | VCCA |

*Table 52 •* **PQ160**

**PQ160**

| Pin Number | A42MX09 Function | A42MX16 Function | A42MX24 Function |
|---|---|---|---|
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | WD, I/O |
| 97 | I/O | I/O | I/O |
| 98 | VCCA | VCCA | VCCA |
| 99 | GND | GND | GND |
| 100 | NC | I/O | I/O |
| 101 | I/O | I/O | I/O |
| 102 | I/O | I/O | I/O |
| 103 | NC | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | I/O | I/O | WD, I/O |
| 107 | I/O | I/O | WD, I/O |
| 108 | I/O | I/O | I/O |
| 109 | GND | GND | GND |
| 110 | NC | I/O | I/O |
| 111 | I/O | I/O | WD, I/O |
| 112 | I/O | I/O | WD, I/O |
| 113 | I/O | I/O | I/O |
| 114 | NC | VCCI | VCCI |
| 115 | I/O | I/O | WD, I/O |
| 116 | NC | I/O | WD, I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | TDI, I/O |
| 119 | I/O | I/O | TMS, I/O |
| 120 | GND | GND | GND |
| 121 | I/O | I/O | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | NC | I/O | I/O |
| 125 | GND | GND | GND |
| 126 | I/O | I/O | I/O |
| 127 | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O |
| 129 | NC | I/O | I/O |
| 130 | GND | GND | GND |
| 131 | I/O | I/O | I/O |

*Table 57 •* **TQ176**

**TQ176**

| Pin Number | A42MX09 Function | A42MX16 Function | A42MX24 Function |
| --- | --- | --- | --- |
| 121 | NC | NC | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | NC | I/O | I/O |
| 125 | NC | I/O | I/O |
| 126 | NC | NC | I/O |
| 127 | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O |
| 129 | I/O | I/O | I/O |
| 130 | I/O | I/O | I/O |
| 131 | I/O | I/O | I/O |
| 132 | I/O | I/O | I/O |
| 133 | GND | GND | GND |
| 134 | I/O | I/O | I/O |
| 135 | SDI, I/O | SDI, I/O | SDI, I/O |
| 136 | NC | I/O | I/O |
| 137 | I/O | I/O | WD, I/O |
| 138 | I/O | I/O | WD, I/O |
| 139 | I/O | I/O | I/O |
| 140 | NC | VCCI | VCCI |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | NC | I/O | I/O |
| 144 | NC | I/O | WD, I/O |
| 145 | NC | NC | WD, I/O |
| 146 | I/O | I/O | I/O |
| 147 | NC | I/O | I/O |
| 148 | I/O | I/O | I/O |
| 149 | I/O | I/O | I/O |
| 150 | I/O | I/O | WD, I/O |
| 151 | NC | I/O | WD, I/O |
| 152 | PRA, I/O | PRA, I/O | PRA, I/O |
| 153 | I/O | I/O | I/O |
| 154 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 155 | VCCA | VCCA | VCCA |
| 156 | GND | GND | GND |
| 157 | I/O | I/O | I/O |

***Table 58 •*** **CQ208**

| CQ208 | |
| --- | --- |
| **Pin Number** | **A42MX36 Function** |
| 111 | I/O |
| 112 | I/O |
| 113 | I/O |
| 114 | I/O |
| 115 | I/O |
| 116 | I/O |
| 117 | I/O |
| 118 | I/O |
| 119 | I/O |
| 120 | I/O |
| 121 | I/O |
| 122 | I/O |
| 123 | I/O |
| 124 | I/O |
| 125 | I/O |
| 126 | GND |
| 127 | I/O |
| 128 | TCK, I/O |
| 129 | LP |
| 130 | VCCA |
| 131 | GND |
| 132 | VCCI |
| 133 | VCCA |
| 134 | I/O |
| 135 | I/O |
| 136 | VCCA |
| 137 | I/O |
| 138 | I/O |
| 139 | I/O |
| 140 | I/O |
| 141 | I/O |
| 142 | I/O |
| 143 | I/O |
| 144 | I/O |
| 145 | I/O |
| 146 | I/O |
| 147 | I/O |

*Table 60 •* **BG272**

| BG272 | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M17 | I/O |
| M18 | I/O |
| M19 | I/O |
| M20 | I/O |
| N1 | I/O |
| N2 | I/O |
| N3 | I/O |
| N4 | VCCI |
| N17 | VCCI |
| N18 | I/O |
| N19 | I/O |
| N20 | I/O |
| P1 | I/O |
| P2 | I/O |
| P3 | I/O |
| P4 | VCCA |
| P17 | I/O |
| P18 | I/O |
| P19 | I/O |
| P20 | I/O |
| R1 | I/O |
| R2 | I/O |
| R3 | I/O |
| R4 | VCCI |
| R17 | VCCI |
| R18 | I/O |
| R19 | I/O |
| R20 | I/O |
| T1 | I/O |
| T2 | I/O |
| T3 | I/O |
| T4 | I/O |
| T17 | VCCA |
| T18 | I/O |

*Table 61 •*   **PG132**

| PG132 | |
| --- | --- |
| **Pin Number** | **A42MX09 Function** |
| B3 | I/O |
| A2 | I/O |
| C3 | DCLK |
| B5 | GNDA |
| E12 | GNDA |
| J2 | GNDA |
| M9 | GNDA |
| B9 | GNDI |
| C5 | GNDI |
| E11 | GNDI |
| F4 | GNDI |
| J3 | GNDI |
| J11 | GNDI |
| L5 | GNDI |
| L9 | GNDI |
| C9 | GNDQ |
| E3 | GNDQ |
| K12 | GNDQ |
| D7 | VCCA |
| G3 | VCCA |
| G10 | VCCA |
| L7 | VCCA |
| C7 | VCCI |
| G2 | VCCI |
| G11 | VCCI |
| K7 | VCCI |

*Table 62 •*   **CQ172**

| | |
|---|---|
| 99 | I/O |
| 100 | I/O |
| 101 | I/O |
| 102 | I/O |
| 103 | GND |
| 104 | I/O |
| 105 | I/O |
| 106 | VKS |
| 107 | VPP |
| 108 | GND |
| 109 | VCCI |
| 110 | VSV |
| 111 | I/O |
| 112 | I/O |
| 113 | VCC |
| 114 | I/O |
| 115 | I/O |
| 116 | I/O |
| 117 | I/O |
| 118 | GND |
| 119 | I/O |
| 120 | I/O |
| 121 | I/O |
| 122 | I/O |
| 123 | GNDI |
| 124 | I/O |
| 125 | I/O |
| 126 | I/O |
| 127 | I/O |
| 128 | I/O |
| 129 | I/O |
| 130 | I/O |
| 131 | SDI |
| 132 | I/O |
| 133 | I/O |
| 134 | I/O |
| 135 | I/O |
| 136 | VCCI |
| 137 | I/O |