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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

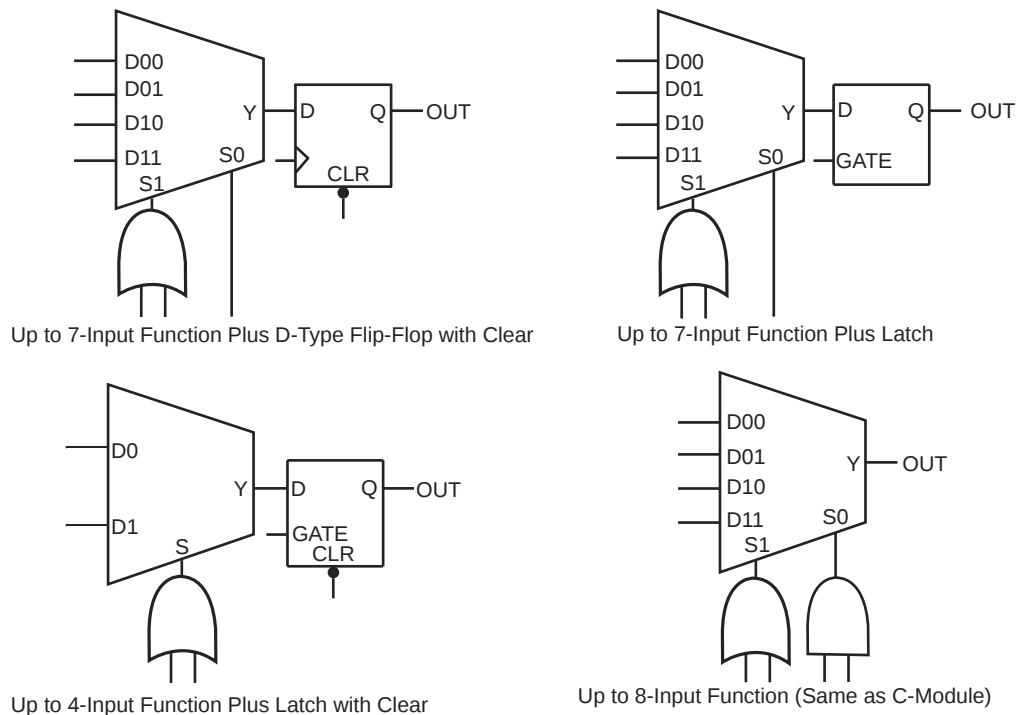
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	72
Number of Gates	14000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx09-plg84a

Figure 4 • 42MX S-Module Implementation

A42MX24 and A42MX36 devices contain D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry, providing a fast, wide-input AND function similar to that found in CPLD architectures (Figure 5, page 9). The D-module allows A42MX24 and A42MX36 devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin, and can also be fed back into the array to be incorporated into other logic.

3.2.2 Dual-Port SRAM Modules

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the A42MX36 dual-port SRAM block is shown in Figure 6, page 9.

The A42MX36 SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]), which are connected to segmented vertical routing tracks.

The A42MX36 dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring FIFO and LIFO queues. The ACTgen Macro Builder within Microsemi's designer software provides capability to quickly design memory functions with the SRAM blocks. Unused SRAM blocks can be used to implement registers for other user logic within the design.

3. All outputs unloaded. All inputs = VCC/VCCI or GND

3.8 3.3 V Operating Conditions

The following table shows 3.3 V operating conditions.

Table 16 • Absolute Maximum Ratings for 40MX Devices*

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCC + 0.5	V
VO	Output Voltage	–0.5 to VCC + 0.5	V
t _{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 17 • Absolute Maximum Ratings for 42MX Devices*

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCCI+0.5	V
VO	Output Voltage	–0.5 to VCCI+0.5	V
t _{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 18 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCA (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCI (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

All the following tables show various specifications and operating conditions of 40MX and 42MX FPGAs.

3.8.1 3.3 V LVTTTL Electrical Specifications

Table 19 • 3.3V LVTTTL Electrical Specifications

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	IOH = -4 mA	2.15		2.15		2.4		2.4		V
VOL ¹	IOL = 6 mA		0.4		0.4		0.48		0.48	V
VIL		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX)		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL			-10		-10		-10		-10	μA
IIH			-10		-10		-10		-10	μA
Input Transition Time, T _R and T _F			500		500		500		500	ns
C _{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC ²	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		15		25		25		25	mA
Low-Power Mode Standby Current	42MX devices only		0.5		ICC - 5.0		ICC - 5.0		ICC - 5.0	mA
I/O, I/O source sink current	Can be derived from the <i>IBIS model</i> (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCC/VCCI = min.
2. All outputs unloaded. All inputs = VCC/VCCI or GND.

3.9 Mixed 5.0 V / 3.3 V Operating Conditions (for 42MX Devices Only)

Table 20 • Absolute Maximum Ratings*

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	-0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	-0.5 to +7.0	V
VI	Input Voltage	-0.5 to VCCA + 0.5	V
VO	Output Voltage	-0.5 to VCCI + 0.5	V
t _{STG}	Storage Temperature	-65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device

3.9.1 Mixed 5.0V/3.3V Electrical Specifications

Table 22 • Mixed 5.0V/3.3V Electrical Specifications

Symbol	Parameter	Commercial		Commercial –F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	IOH = –10 mA	2.4		2.4						V
	IOH = –4 mA					2.4		2.4		V
VOL ¹	IOL = 10 mA	0.5		0.5						V
	IOL = 6 mA					0.4		0.4		V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH ²		2.0	VCCA + 0.3	2.0	VCCA + 0.3	2.0	VCCA + 0.3	2.0	VCCA + 0.3	V
IL	VIN = 0.5 V	–10		–10		–10		–10		μA
IH	VIN = 2.7 V	–10		–10		–10		–10		μA
Input Transition Time, TR and TF		500		500		500		500		ns
C _{IO} I/O Capacitance		10		10		10		10		pF
Standby Current, ICC ³	A42MX09	5		25		25		25		mA
	A42MX16	6		25		25		25		mA
	A42MX24, A42MX36	20		25		25		25		mA
Low Power Mode Standby Current		0.5		ICC – 5.0		ICC – 5.0		ICC – 5.0		mA
I/O I/O source sink current Can be derived from the <i>IBIS model</i> (http://www.microsemi.com/soc/techdocs/models/ibis.html)										

1. Only one output tested at a time. VCCI = min.

2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

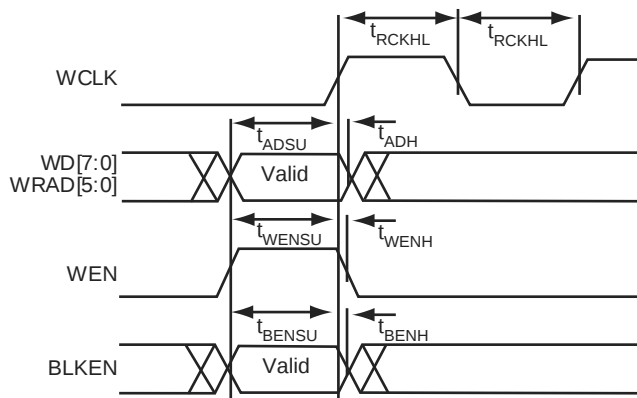
3. All outputs unloaded. All inputs = VCCI or GND

3.9.2 Output Drive Characteristics for 5.0 V PCI Signaling

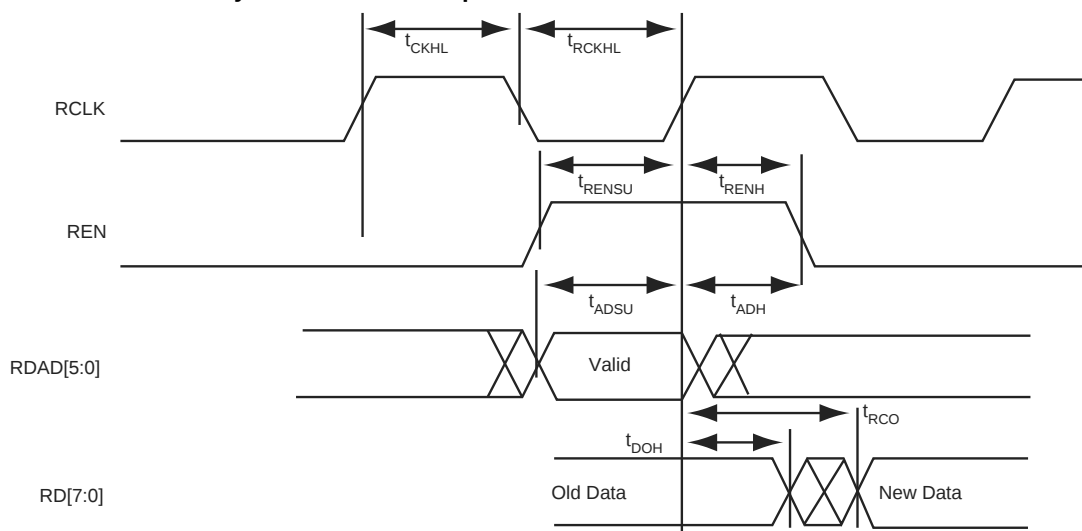
MX PCI device I/O drivers were designed specifically for high-performance PCI systems. Figure 16, page 28 shows the typical output drive characteristics of the MX devices. MX output drivers are compliant with the PCI Local Bus Specification.

Table 23 • DC Specification (5.0 V PCI Signaling)¹

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
VCCI	Supply Voltage for I/Os		4.75	5.25	4.75	5.25 ²	V
VIH ³	Input High Voltage		2.0	VCC + 0.5	2.0	VCCI + 0.3	V
VIL	Input Low Voltage		–0.5	0.8	–0.3	0.8	V
IIH	Input High Leakage Current	VIN = 2.7 V		70	—	10	μA
IIL	Input Low Leakage Current	VIN=0.5 V		–70	—	–10	μA
VOH	Output High Voltage	IOUT = –2 mA IOUT = –6 mA	2.4		3.84		V
VOL	Output Low Voltage	IOUT = 3 mA, 6 mA		0.55	—	0.33	V

Figure 30 • 42MX SRAM Write Operation

Note: Identical timing for falling edge clock

Figure 31 • 42MX SRAM Synchronous Read Operation

Note: Identical timing for falling edge clock

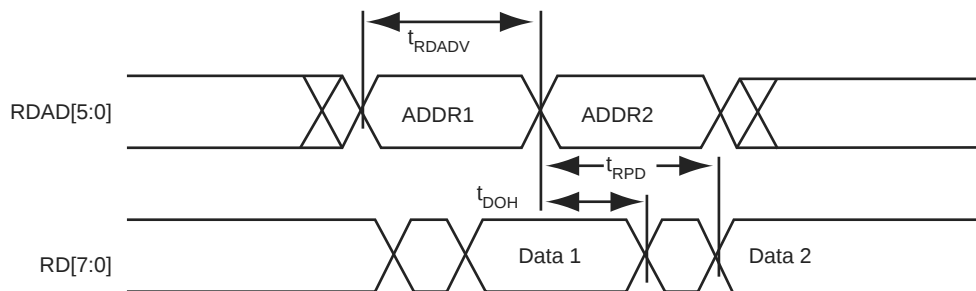
Figure 32 • 42MX SRAM Asynchronous Read Operation—Type 1 (Read Address Controlled)

Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH		3.3		3.8		4.3		5.1		7.2	ns
t _{DHL}	Data-to-Pad LOW		4.0		4.6		5.2		6.1		8.6	ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.3		4.9		5.8		8.0	ns
t _{ENZL}	Enable Pad Z to LOW		4.7		5.4		6.1		7.2		10.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.1	ns
t _{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{THL}	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t _{DHL}	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t _{ENZH}	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t _{ENZL}	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t _{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t _{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d _{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35pF loading

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t _{PD2}	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t _{CO}	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t _{GO}	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays ¹												

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RD1}	FO = 1 Routing Delay		2.0		2.2		2.5		3.0		4.2	ns
t _{RD2}	FO = 2 Routing Delay		2.7		3.1		3.5		4.1		5.7	ns
t _{RD3}	FO = 3 Routing Delay		3.4		3.9		4.4		5.2		7.3	ns
t _{RD4}	FO = 4 Routing Delay		4.2		4.8		5.4		6.3		8.9	ns
t _{RD8}	FO = 8 Routing Delay		7.1		8.2		9.2		10.9		15.2	ns
Logic Module Sequential Timing²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		4.3		4.9		5.6		6.6		9.2	ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		4.3		4.9		5.6		6.6		9.2	ns
t _{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		4.6		5.3		6.0		7.0		9.8	ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		4.6		5.3		6.0		7.0		9.8	ns
t _A	Flip-Flop Clock Input Period		6.8		7.8		8.9		10.4		14.6	ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		109		101		92		80		48	MHz
Input Module Propagation Delays												
t _{INYH}	Pad-to-Y HIGH		1.0		1.1		1.3		1.5		2.1	ns
t _{INYL}	Pad-to-Y LOW		0.9		1.0		1.1		1.3		1.9	ns
Input Module Predicted Routing Delays¹												
t _{IRD1}	FO = 1 Routing Delay		2.9		3.4		3.8		4.5		6.3	ns
t _{IRD2}	FO = 2 Routing Delay		3.6		4.2		4.8		5.6		7.8	ns
t _{IRD3}	FO = 3 Routing Delay		4.4		5.0		5.7		6.7		9.4	ns
t _{IRD4}	FO = 4 Routing Delay		5.1		5.9		6.7		7.8		11.0	ns
t _{IRD8}	FO = 8 Routing Delay		8.0		9.26		10.5		12.6		17.3	ns
Global Clock Network												
t _{CKH}	Input LOW to HIGH	FO = 16	6.4		7.4		8.3		9.8		13.7	ns
		FO = 128	6.4		7.4		8.3		9.8		13.7	
t _{CKL}	Input HIGH to LOW	FO = 16	6.7		7.8		8.8		10.4		14.5	ns
		FO = 128	6.7		7.8		8.8		10.4		14.5	
t _{PWH}	Minimum Pulse Width HIGH	FO = 16	3.1		3.6		4.1		4.8		6.7	ns
		FO = 128	3.3		3.8		4.3		5.1		7.1	
t _{PWL}	Minimum Pulse Width LOW	FO = 16	3.1		3.6		4.1		4.8		6.7	ns
		FO = 128	3.3		3.8		4.3		5.1		7.1	
t _{CKSW}	Maximum Skew	FO = 16	0.6		0.6		0.7		0.8		1.2	ns
		FO = 128	0.8		0.9		1.0		1.2		1.6	

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RD4}	FO = 4 Routing Delay	1.9		2.1		2.4		2.9		4.0		ns
t _{RD8}	FO = 8 Routing Delay	3.2		3.6		4.1		4.8		6.7		ns
Logic Module Sequential Timing ^{3, 4}												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.5		0.5		0.6		0.7		0.9		ns
t _{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.7		5.3		6.0		7.0		9.8		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.2		6.9		7.8		9.2		12.9		ns
t _A	Flip-Flop Clock Input Period	5.0		5.6		6.2		7.1		9.9		ns
t _{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
t _{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{OUTSU}	Output Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency	161		146		135		117		70		MHz

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		3.4		3.8		4.3		5.1		7.1	ns
t _{DHL}	Data-to-Pad LOW		4.0		4.5		5.1		6.1		8.3	ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t _{ENZL}	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t _{ENHZ}	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t _{ENLZ}	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t _{GLH}	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t _{GHL}	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t _{LSU}	I/O Latch Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad),64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d _{TLH}	Capacity Loading, LOW to HIGH	0.00		0.00		0.00		0.10		0.01		ns/pF
d _{THL}	Capacity Loading, HIGH to LOW	0.09		0.10		0.10		0.10		0.10		ns/pF

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		2.4		2.7		3.1		3.6		5.1	ns
t _{DHL}	Data-to-Pad LOW		2.8		3.2		3.6		4.2		5.9	ns
t _{ENZH}	Enable Pad Z to HIGH		2.5		2.8		3.2		3.8		5.3	ns
t _{ENZL}	Enable Pad Z to LOW		2.8		3.1		3.5		4.2		5.9	ns
t _{ENHZ}	Enable Pad HIGH to Z		5.2		5.7		6.5		7.6		10.7	ns
t _{ENLZ}	Enable Pad LOW to Z		4.8		5.3		6.0		7.1		9.9	ns
t _{GLH}	G-to-Pad HIGH		2.9		3.2		3.6		4.3		6.0	ns
t _{GHL}	G-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t _{LSU}	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.6		6.1		6.9		8.1		11.4	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.6		11.8		13.4		15.7		22.0	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵ (continued)													
t _{LH}	I/O Latch Output Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d _{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH			4.8		5.3		5.5		6.4		9.0	ns
t _{DHL}	Data-to-Pad LOW			3.5		3.9		4.1		4.9		6.8	ns
t _{ENZH}	Enable Pad Z to HIGH			3.6		4.0		4.5		5.3		7.4	ns
t _{ENZL}	Enable Pad Z to LOW			3.4		4.0		5.0		5.8		8.2	ns
t _{ENHZ}	Enable Pad HIGH to Z			7.2		8.0		9.0		10.7		14.9	ns
t _{ENLZ}	Enable Pad LOW to Z			6.7		7.5		8.5		9.9		13.9	ns
t _{GLH}	G-to-Pad HIGH			6.8		7.6		8.6		10.1		14.2	ns
t _{GHL}	G-to-Pad LOW			6.8		7.6		8.6		10.1		14.2	ns
t _{LSU}	I/O Latch Set-Up		0.7		0.7		0.8		1.0		1.4		ns
t _{LH}	I/O Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d _{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
t _{HEXT}	Input Latch External Hold	FO = 32	3.9		4.3		4.9		5.7		8.1		ns
		FO = 486	4.6		5.2		5.8		6.9		9.6		ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	7.8		8.7		9.5		10.8		18.2		ns
		FO = 486	8.6		9.5		10.4		11.9		19.9		ns

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

4 Package Pin Assignments

The following figures and tables give the details of the package pin assignments.

Figure 38 • PL44

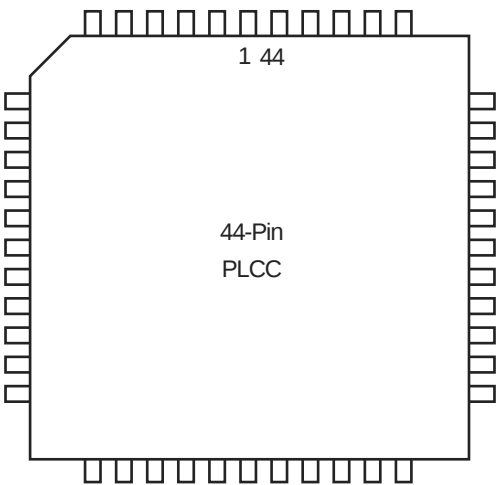


Table 47 • PL44

PL44		
Pin Number	A40MX02 Function	A40MX04 Function
1	I/O	I/O
2	I/O	I/O
3	VCC	VCC
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	GND	GND
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	VCC	VCC
15	I/O	I/O
16	VCC	VCC
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O

Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
58	VCCI	VCCI	VCCI
59	GND	GND	GND
60	VCCA	VCCA	VCCA
61	LP	LP	LP
62	I/O	I/O	TCK, I/O
63	I/O	I/O	I/O
64	GND	GND	GND
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	I/O	I/O	I/O
69	GND	GND	GND
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	I/O	I/O	I/O
77	NC	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	GND	GND	GND
81	I/O	I/O	I/O
82	SDO, I/O	SDO, I/O	SDO, TDO, I/O
83	I/O	I/O	WD, I/O
84	I/O	I/O	WD, I/O
85	I/O	I/O	I/O
86	NC	VCCI	VCCI
87	I/O	I/O	I/O
88	I/O	I/O	WD, I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O

Figure 44 • PQ208

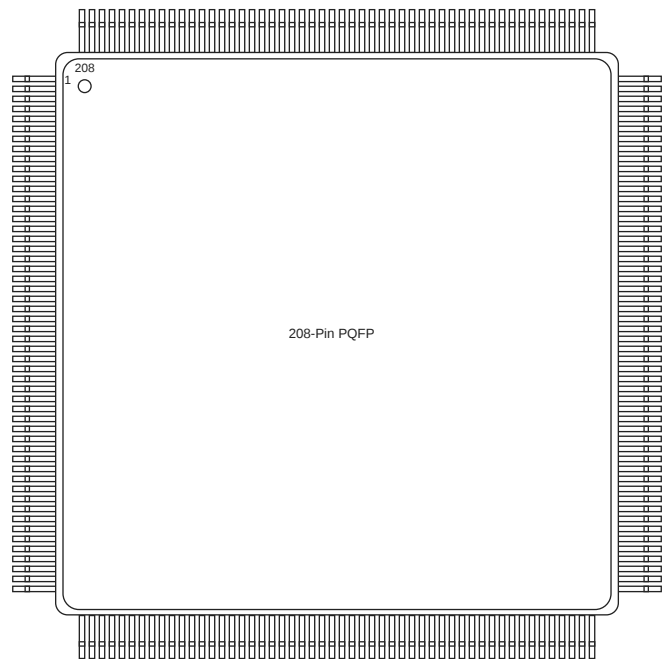


Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
1	GND	GND	GND
2	NC	VCCA	VCCA
3	MODE	MODE	MODE
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	NC	I/O	I/O
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	NC	I/O	I/O
17	VCCA	VCCA	VCCA
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
163	WD, I/O
164	WD, I/O
165	I/O
166	QCLKA, I/O
167	I/O
168	I/O
169	I/O
170	I/O
171	I/O
172	VCCI
173	I/O
174	WD, I/O
175	WD, I/O
176	I/O
177	I/O
178	TDI, I/O
179	TMS, I/O
180	GND
181	VCCA
182	GND
183	I/O
184	I/O
185	I/O
186	I/O
187	I/O
188	I/O
189	I/O
190	I/O
191	I/O
192	VCCI
193	I/O
194	I/O
195	I/O
196	I/O
197	I/O
198	I/O
199	I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
200	I/O
201	I/O
202	I/O
203	I/O
204	I/O
205	I/O
206	VCCA
207	I/O
208	I/O
209	VCCA
210	VCCI
211	I/O
212	I/O
213	I/O
214	I/O
215	I/O
216	I/O
217	I/O
218	I/O
219	VCCA
220	I/O
221	I/O
222	I/O
223	I/O
224	I/O
225	I/O
226	I/O
227	VCCI
228	I/O
229	I/O
230	I/O
231	I/O
232	I/O
233	I/O
234	I/O
235	I/O
236	I/O

Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
121	NC	NC	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	NC	I/O	I/O
125	NC	I/O	I/O
126	NC	NC	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	I/O	I/O	I/O
130	I/O	I/O	I/O
131	I/O	I/O	I/O
132	I/O	I/O	I/O
133	GND	GND	GND
134	I/O	I/O	I/O
135	SDI, I/O	SDI, I/O	SDI, I/O
136	NC	I/O	I/O
137	I/O	I/O	WD, I/O
138	I/O	I/O	WD, I/O
139	I/O	I/O	I/O
140	NC	VCCI	VCCI
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	NC	I/O	WD, I/O
145	NC	NC	WD, I/O
146	I/O	I/O	I/O
147	NC	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	I/O	I/O	WD, I/O
151	NC	I/O	WD, I/O
152	PRA, I/O	PRA, I/O	PRA, I/O
153	I/O	I/O	I/O
154	CLKA, I/O	CLKA, I/O	CLKA, I/O
155	VCCA	VCCA	VCCA
156	GND	GND	GND
157	I/O	I/O	I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
1	GND
2	VCCA
3	MODE
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	VCCA
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	VCCI
29	VCCA
30	I/O
31	I/O
32	VCCA
33	I/O
34	I/O
35	I/O
36	I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	I/O
125	I/O
126	GND
127	I/O
128	TCK, I/O
129	LP
130	VCCA
131	GND
132	VCCI
133	VCCA
134	I/O
135	I/O
136	VCCA
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
J9	GND
J10	GND
J11	GND
J12	GND
J17	VCCA
J18	I/O
J19	I/O
J20	I/O
K1	I/O
K2	I/O
K3	I/O
K4	VCCI
K9	GND
K10	GND
K11	GND
K12	GND
K17	I/O
K18	VCCA
K19	VCCA
K20	LP
L1	I/O
L2	I/O
L3	VCCA
L4	VCCA
L9	GND
L10	GND
L11	GND
L12	GND
L17	VCCI
L18	I/O
L19	I/O
L20	TCK, I/O
M1	I/O
M2	I/O
M3	I/O
M4	VCCI
M9	GND