Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	101
Number of Gates	14000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx09-pq160

Figures

- The Transient Current, page 13 is new (SAR 36930).
- Package names were revised according to standards established in *Package Mechanical Drawings* (SAR 34774)

1.7 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document

- In Table 20, page 23, the limits in VI were changed from -0.5 to VCCI + 0.5 to -0.5 to VCCA + 0.5

In Table 22, page 25, V_{OH} was changed from 3.7 to 2.4 for the min in industrial and military. V_{IH} had V_{CCI} and that was changed to VCCA

1.8 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- The Ease of Integration, page 1 was updated
- The Temperature Grade Offerings, page 5 is new
- The Speed Grade Offerings, page 5 is new
- The General Description, page 6 was updated
- The MultiPlex I/O Modules, page 11 was updated
- The User Security, page 12 was updated
- Table 6, page 13 was updated
- The Power Dissipation, page 14 was updated.
- The Static Power Component, page 14 was updated
- The Equivalent Capacitance, page 15 was updated
- Figure 13, page 17 was updated
- Table 10, page 18 was updated.
- Figure 14, page 18 was updated.
- Table 11, page 19 was updated.

Figure 13 • **Silicon Explorer II Setup with 42MX**

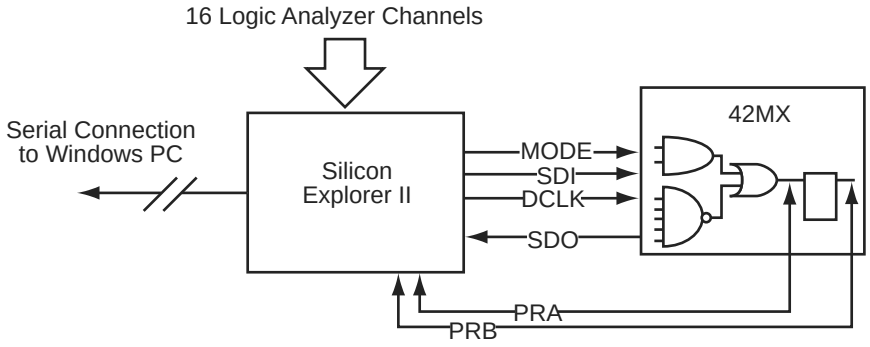


Table 8 • **Device Configuration Options for Probe Capability**

Security Fuse(s) Programmed	Mode	PRA, PRB[1]	SDI, SDO, DCLK[1]
No	LOW	User I/Os[2]	User I/Os[2]
No	HIGH	Probe Circuit Outputs	Probe Circuit Inputs
Yes	–	Probe Circuit Secured	Probe Circuit Secured

1. *Avoid using SDI, SDO, DCLK, PRA and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
2. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. See the Pin Descriptions,* page 83 *for information on unused I/O pins*

3.4.7 Design Consideration

It is recommended to use a series 70Ω termination resistor on every probe connector (SDI, SDO, MODE, DCLK, PRA and PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

3.4.8 IEEE Standard 1149.1 Boundary Scan Test (BST) Circuitry

42MX24 and 42MX36 devices are compatible with IEEE Standard 1149.1 (informally known as Joint Testing Action Group Standard or JTAG), which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic MX boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers and instruction register (Figure 14, page 18). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and some optional instructions. Table 9, page 18 describes the ports that control JTAG testing, while Table 10, page 18 describes the test instructions supported by these MX devices.

Each test section is accessed through the TAP, which has four associated pins: TCK (test clock input), TDI and TDO (test data input and output), and TMS (test mode selector).

The TAP controller is a four-bit state machine. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles.

42MX24 and 42MX36 devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary-scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

Figure 14 • **42MX IEEE 1149.1 Boundary Scan Circuitry**

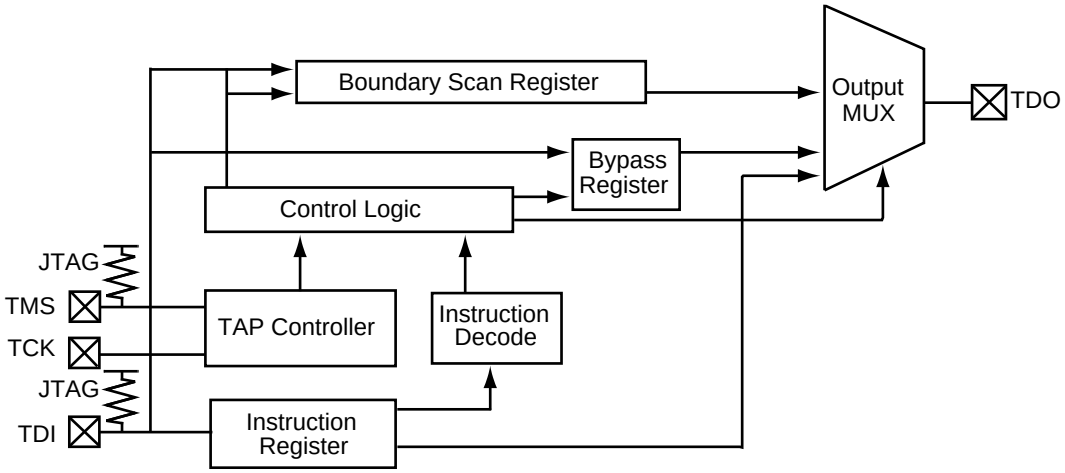


Table 9 • **Test Access Port Descriptions**

Port	Description
TMS (Test Mode Select)	Serial input for the test logic control bits. Data is captured on the rising edge of the test logic clock (TCK).
TCK (Test Clock Input)	Dedicated test logic clock used serially to shift test instruction, test data, and control inputs on the rising edge of the clock, and serially to shift the output data on the falling edge of the clock. The maximum clock frequency for TCK is 20 MHz.
TDI (Test Data Input)	Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock.
TDO (Test Data Output)	Serial output for test instruction and data from the test logic. TDO is set to an Inactive Drive state (high impedance) when data scanning is not in progress.

Table 10 • **Supported BST Public Instructions**

Instruction	IR Code (IR2.IR0)	Instruction Type	Description
EXTEST	000	Mandatory	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
SAMPLE/PRELOAD	001	Mandatory	Allows a snapshot of the signals at the device pins to be captured and examined during operation
HIGH Z	101	Optional	Tristates all I/Os to allow external signals to drive pins. See the IEEE Standard 1149.1 specification.
CLAMP	110	Optional	Allows state of signals driven from component pins to be determined from the Boundary-Scan Register. See the IEEE Standard 1149.1 specification for details.
BYPASS	111	Mandatory	Enables the bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the test chain.

3. All outputs unloaded. All inputs = VCC/VCCI or GND

3.8 3.3 V Operating Conditions

The following table shows 3.3 V operating conditions.

Table 16 • **Absolute Maximum Ratings for 40MX Devices***

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCC + 0.5	V
VO	Output Voltage	–0.5 to VCC + 0.5	V
t_{STG}	Storage Temperature	–65 to + 150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 17 • **Absolute Maximum Ratings for 42MX Devices***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCCI+0.5	V
VO	Output Voltage	–0.5 to VCCI+0.5	V
t_{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

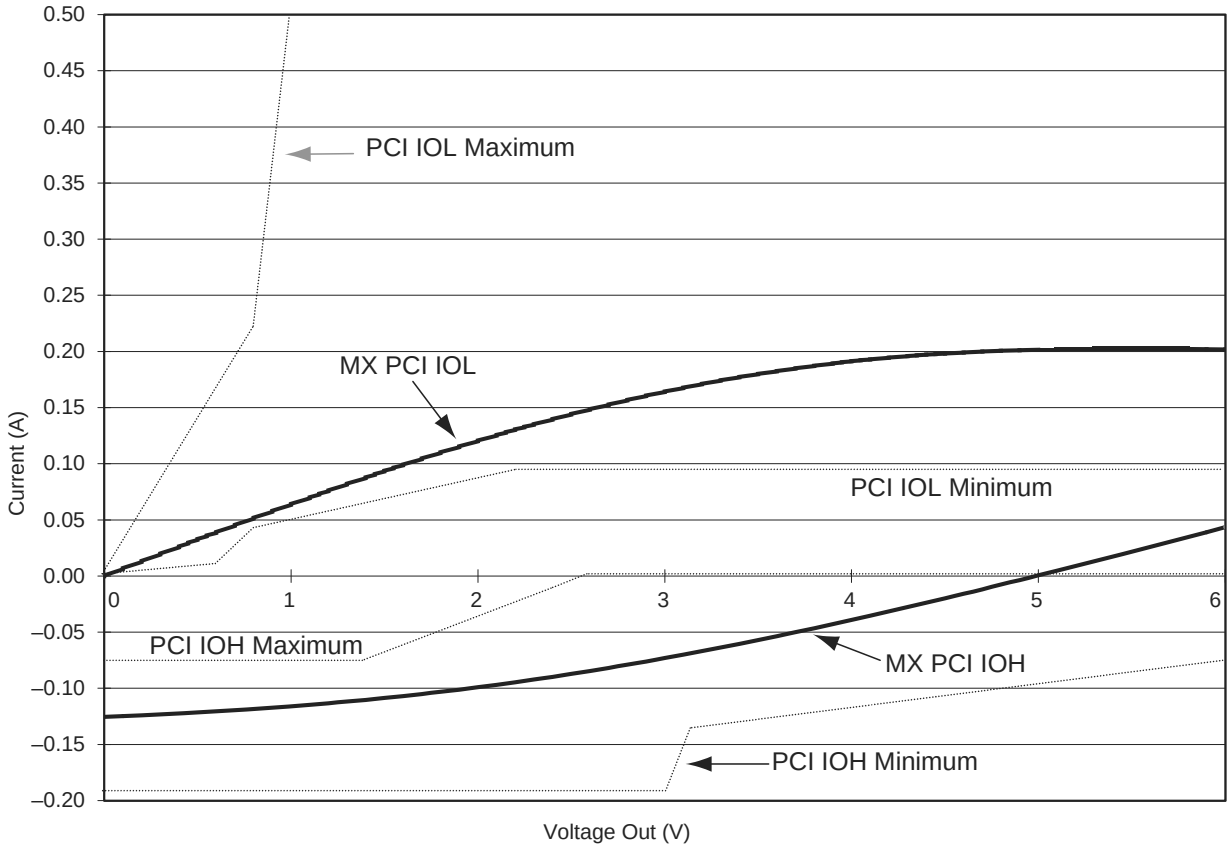
Table 18 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCA (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCI (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

All the following tables show various specifications and operating conditions of 40MX and 42MX FPGAs.

Figure 16 • **Typical Output Drive Characteristics (Based Upon Measured Data)**



3.9.4 Junction Temperature (T_J)

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a \quad (1)$$

EQ 4

where:

- T_a = Ambient Temperature
- ΔT = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$ (2)
- P = Power
- θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in Table 27, page 29.

3.9.5 Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc}, and the junction-to-ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of θ_{ja}.

approximately a 3 ns to a 6 ns delay, which is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section, shown in Table 34, page 41.

3.11.3 Timing Derating

MX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature and worst-case processing.

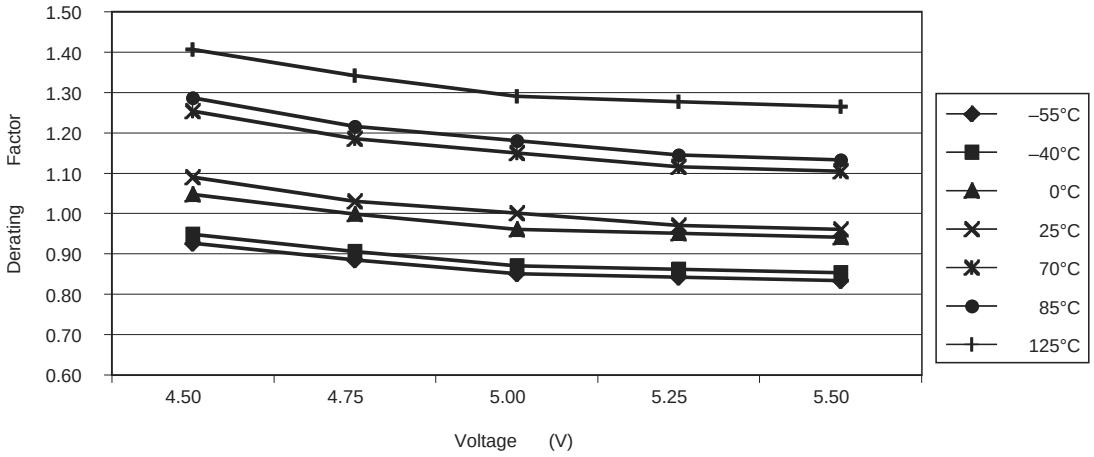
3.11.4 Temperature and Voltage Derating Factors

The following tables and figures show temperature and voltage derating factors for 40MX and 42MX FPGAs.

Table 28 • **42MX Temperature and Voltage Derating Factors (Normalized to T_J = 25°C, VCCA = 5.0 V)**

	Temperature						
42MX Voltage	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
4.50	0.93	0.95	1.05	1.09	1.25	1.29	1.41
4.75	0.88	0.90	1.00	1.03	1.18	1.22	1.34
5.00	0.85	0.87	0.96	1.00	1.15	1.18	1.29
5.25	0.84	0.86	0.95	0.97	1.12	1.14	1.28
5.50	0.83	0.85	0.94	0.96	1.10	1.13	1.26

Figure 34 • **42MX Junction Temperature and Voltage Derating Curves (Normalized to TJ = 25°C, VCCA = 5.0 V)**



Note: This derating factor applies to all routing and propagation delays

Table 29 • **40MX Temperature and Voltage Derating Factors(Normalized to TJ = 25°C, VCC = 5.0 V)**

	Temperature						
40MX Voltage	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
4.50	0.89	0.93	1.02	1.09	1.25	1.31	1.45
4.75	0.84	0.88	0.97	1.03	1.18	1.24	1.37
5.00	0.82	0.85	0.94	1.00	1.15	1.20	1.33
5.25	0.80	0.82	0.91	0.97	1.12	1.16	1.29
5.50	0.79	0.82	0.90	0.96	1.10	1.15	1.28

Table 35 • **A40MX02 Timing Characteristics (Nominal 3.3 V Operation) *(continued)***
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[4]												
t_{DLH}	Data-to-Pad HIGH		5.5		6.4		7.2		8.5		11.9	ns
t_{DHL}	Data-to-Pad LOW		4.8		5.5		6.2		7.3		10.2	ns
t_{ENZH}	Enable Pad Z to HIGH		4.7		5.5		6.2		7.3		10.2	ns
t_{ENZL}	Enable Pad Z to LOW		6.8		7.9		8.9		10.5		14.7	ns
t_{ENHZ}	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9	ns
t_{ENLZ}	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7	ns
d_{TLH}	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro
4. Delays based on 35 pF loading

Table 36 • **A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t_{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t_{PD2}	Dual-Module Macros		2.3		3.1		3.5		4.1		5.7	ns
t_{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays[1]												
t_{RD1}	FO = 1 Routing Delay		1.2		1.6		1.8		2.1		3.0	ns
t_{RD2}	FO = 2 Routing Delay		1.9		2.2		2.5		2.9		4.1	ns
t_{RD3}	FO = 3 Routing Delay		2.4		2.8		3.2		3.7		5.2	ns
t_{RD4}	FO = 4 Routing Delay		2.9		3.4		3.9		4.5		6.3	ns
t_{RD8}	FO = 8 Routing Delay		5.0		5.8		6.6		7.8		10.9	ns
Logic Module Sequential Timing[2]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	3.1		3.5		4.0		4.7		6.6		ns

Table 36 • **A40MX04 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

Table 40 • **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RD3}	FO = 3 Routing Delay			1.3		1.4		1.6		1.9		2.7	ns
t_{RD4}	FO = 4 Routing Delay			1.6		1.7		2.0		2.3		3.2	ns
t_{RD8}	FO = 8 Routing Delay			2.6		2.9		3.2		3.8		5.3	ns
Logic Module Sequential Timing[3,4]													
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up		0.3		0.4		0.4		0.5		0.7		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up		0.7		0.8		0.9		1.0		1.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		3.4		3.8		4.3		5.0		7.1		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		4.5		5.0		5.6		6.6		9.2		ns
t_A	Flip-Flop Clock Input Period		6.8		7.6		8.6		10.1		14.1		ns
t_{INH}	Input Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Set-Up		0.5		0.5		0.6		0.7		1.0		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up		0.5		0.5		0.6		0.7		1.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency			215		195		179		156		94	MHz
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			1.1		1.2		1.3		1.6		2.2	ns
t_{INYL}	Pad-to-Y LOW			0.8		0.9		1.0		1.2		1.7	ns
t_{INGH}	G to Y HIGH			1.4		1.6		1.8		2.1		2.9	ns
t_{INGL}	G to Y LOW			1.4		1.6		1.8		2.1		2.9	ns
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			1.8		2.0		2.3		2.7		4.0	ns
t_{IRD2}	FO = 2 Routing Delay			2.1		2.3		2.6		3.1		4.3	ns
t_{IRD3}	FO = 3 Routing Delay			2.3		2.6		3.0		3.5		4.9	ns
t_{IRD4}	FO = 4 Routing Delay			2.6		3.0		3.3		3.9		5.4	ns
t_{IRD8}	FO = 8 Routing Delay			3.6		4.0		4.6		5.4		7.5	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		2.6		2.9		3.3		3.9		5.4	ns
		FO = 384		2.9		3.2		3.6		4.3		6.0	ns
t_{CKL}	Input HIGH to LOW	FO = 32		3.8		4.2		4.8		5.6		7.8	ns
		FO = 384		4.5		5.0		5.6		6.6		9.2	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	3.2		3.5		4.0		4.7		6.6		ns
		FO = 384	3.7		4.1		4.6		5.4		7.6		ns

Table 42 • **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		2.4		2.7		3.1		3.6		5.1	ns
t_{DHL}	Data-to-Pad LOW		2.8		3.2		3.6		4.2		5.9	ns
t_{ENZH}	Enable Pad Z to HIGH		2.5		2.8		3.2		3.8		5.3	ns
t_{ENZL}	Enable Pad Z to LOW		2.8		3.1		3.5		4.2		5.9	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.2		5.7		6.5		7.6		10.7	ns
t_{ENLZ}	Enable Pad LOW to Z		4.8		5.3		6.0		7.1		9.9	ns
t_{GLH}	G-to-Pad HIGH		2.9		3.2		3.6		4.3		6.0	ns
t_{GHL}	G-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t_{LSU}	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.6		6.1		6.9		8.1		11.4	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.6		11.8		13.4		15.7		22.0	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

Table 44 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[5] (Continued)												
t_{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t_{GLH}	G-to-Pad HIGH		2.9		3.3		3.7		4.4		6.1	ns
t_{GHL}	G-to-Pad LOW		2.9		3.3		3.7		4.4		6.1	ns
t_{LSU}	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

Table 45 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations (continued)												
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Set-Up	0.9		1.0		1.1		1.3		1.8		ns
t_{RENH}	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t_{WENSU}	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Set-Up	3.9		4.3		4.9		5.7		8.0		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations												
t_{RPD}	Asynchronous Access Time		11.3		12.6		14.3		16.8		23.5	ns
t_{RDADV}	Read Address Valid	12.3		13.7		15.5		18.2		25.5		ns
t_{ADSU}	Address/Data Set-Up Time	2.3		2.5		2.8		3.4		4.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RENSUA}	Read Enable Set-Up to Address Valid	0.9		1.0		1.1		1.3		1.8		ns
t_{RENHA}	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t_{WENSU}	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.8		2.0		2.1		2.5		3.5	ns
Input Module Propagation Delays												
t_{INPY}	Input Data Pad-to-Y		1.4		1.6		1.8		2.1		3.0	ns
t_{INGO}	Input Latch Gate-to-Output		2.0		2.2		2.5		2.9		4.1	ns
t_{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t_{ILA}	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

Table 45 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			2.8		3.1		3.5		4.1		5.7	ns
t_{IRD2}	FO = 2 Routing Delay			3.2		3.5		4.1		4.8		6.7	ns
t_{IRD3}	FO = 3 Routing Delay			3.7		4.1		4.7		5.5		7.7	ns
t_{IRD4}	FO = 4 Routing Delay			4.2		4.6		5.3		6.2		8.7	ns
t_{IRD8}	FO = 8 Routing Delay			6.1		6.8		7.7		9.0		12.6	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		4.6		5.1		5.7		6.7		9.3	ns
		FO = 635		5.0		5.6		6.3		7.4		10.3	ns
t_{CKL}	Input HIGH to LOW	FO = 32		5.3		5.9		6.7		7.8		11.0	ns
		FO = 635		6.8		7.6		8.6		10.1		14.1	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	2.5		2.7		3.1		3.6		5.1		ns
		FO = 635	2.8		3.1		3.5		4.1		5.7		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	2.5		2.7		3.1		3.6		5.1		ns
		FO = 635	2.8		3.1		3.5		4.1		5.7		ns
t_{CKSW}	Maximum Skew	FO = 32		1.0		1.2		1.3		1.5		2.2	ns
		FO = 635		1.0		1.2		1.3		1.5		2.2	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 635	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	4.0		4.4		5.0		5.9		8.2		ns
		FO = 635	4.6		5.2		5.9		6.9		9.6		ns
t_P	Minimum Period ($1/f_{MAX}$)	FO = 32	9.2		10.2		11.1		12.7		21.2		ns
		FO = 635	9.9		11.0		12.0		13.8		23.0		ns
f_{MAX}	Maximum Datapath Frequency	FO = 32		108		98		90		79		47	MHz
		FO = 635		100		91		83		73		44	MHz
TTL Output Module Timing[5]													
t_{DLH}	Data-to-Pad HIGH			3.6		4.0		4.5		5.3		7.4	ns
t_{DHL}	Data-to-Pad LOW			4.2		4.6		5.2		6.2		8.6	ns
t_{ENZH}	Enable Pad Z to HIGH			3.7		4.2		4.7		5.5		7.7	ns
t_{ENZL}	Enable Pad Z to LOW			4.1		4.6		5.2		6.1		8.5	ns
t_{ENHZ}	Enable Pad HIGH to Z			7.34		8.2		9.3		10.9		15.3	ns
TTL Output Module Timing[5]													
t_{ENLZ}	Enable Pad LOW to Z			6.9		7.6		8.7		10.2		14.3	ns
t_{GLH}	G-to-Pad HIGH			4.9		5.5		6.2		7.3		10.2	ns
t_{GHL}	G-to-Pad LOW			4.9		5.5		6.2		7.3		10.2	ns
t_{LSU}	I/O Latch Output Set-Up		0.7		0.7		0.8		1.0		1.4		ns
t_{LH}	I/O Latch Output Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.9		8.8		10.0		11.8		16.5	ns

Table 45 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.9		12.1		13.7		16.1		22.5	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.10		0.11		0.12		0.14		0.20	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.10		0.11		0.12		0.14		0.20	ns/pF
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		4.9		5.5		6.2		7.3		10.3	ns
t_{DHL}	Data-to-Pad LOW		3.4		3.8		4.3		5.1		7.1	ns
t_{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.7		5.5		7.7	ns
t_{ENZL}	Enable Pad Z to LOW		4.1		4.6		5.2		6.1		8.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.4		8.2		9.3		10.9		15.3	ns
t_{ENLZ}	Enable Pad LOW to Z		6.9		7.6		8.7		10.2		14.3	ns
t_{GLH}	G-to-Pad HIGH		7.0		7.8		8.9		10.4		14.6	ns
t_{GHL}	G-to-Pad LOW		7.0		7.8		8.9		10.4		14.6	ns
t_{LSU}	I/O Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.9		8.8		10.0		11.8		16.5	ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. Delays based on 35 pF loading.

3.12 Pin Descriptions

This section lists the pin descriptions for 40MX and 42MX series FPGAs.

CLK/A/B, I/O Global Clock

Clock inputs for clock distribution networks. CLK is for 40MX while CLKA and CLKB are for 42MX devices. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK, I/ODiagnostic Clock

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND, Ground

Input LOW supply voltage.

I/O, Input/Output

Input, output, tristate or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/Os pins are configured by the Designer software as shown in Table 46, page 84.

Table 46 • **Configuration of Unused I/Os**

Device	Configuration
A40MX02, A40MX04	Pulled LOW
A42MX09, A42MX16	Pulled LOW
A42MX24, A42MX36	Tristated

In all cases, it is recommended to tie all unused MX I/O pins to LOW on the board. This applies to all dual-purpose pins when configured as I/Os as well.

LP, Low Power Mode

Controls the low power mode of all 42MX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation in 200 µs after the LP pin is driven to a logic LOW.

MODE, Mode

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). The MODE pin is held HIGH to provide verification capability. The MODE pin should be terminated to GND through a 10kΩ resistor so that the MODE pin can be pulled HIGH when required.

NC, No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O

PRB, I/OProbe A/B

The Probe pin is used to output data from any user-defined design node within the device. Each diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. The Probe pin is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

QCLKA/B/C/D, I/O Quadrant Clock

Quadrant clock inputs for A42MX36 devices. When not used as a register control signal, these pins can function as user I/Os.

SDI, I/OSerial Data Input

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDO, I/OSerial Data Output

Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. SDO is available for 42MX devices only.

When Silicon Explorer II is being used, SDO will act as an output while the "checksum" command is run. It will return to user I/O when "checksum" is complete.

TCK, I/O Test Clock

Table 49 • **PL84**

PL84				
Pin Number	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
47	I/O	I/O	I/O	WD, I/O
48	I/O	I/O	I/O	I/O
49	I/O	GND	GND	GND
50	I/O	I/O	I/O	WD, I/O
51	I/O	I/O	I/O	WD, I/O
52	I/O	SDO, I/O	SDO, I/O	SDO, TDO, I/O
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	GND	I/O	I/O	I/O
61	GND	I/O	I/O	I/O
62	I/O	I/O	I/O	TCK, I/O
63	I/O	LP	LP	LP
64	CLK, I/O	VCCA	VCCA	VCCA
65	I/O	VCCI	VCCI	VCCI
66	MODE	I/O	I/O	I/O
67	VCC	I/O	I/O	I/O
68	VCC	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	GND	GND	GND
71	I/O	I/O	I/O	I/O
72	SDI, I/O	I/O	I/O	I/O
73	DCLK, I/O	I/O	I/O	I/O
74	PRA, I/O	I/O	I/O	I/O
75	PRB, I/O	I/O	I/O	I/O
76	I/O	SDI, I/O	SDI, I/O	SDI, I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	WD, I/O
79	I/O	I/O	I/O	WD, I/O
80	I/O	I/O	I/O	WD, I/O
81	I/O	PRA, I/O	PRA, I/O	PRA, I/O
82	GND	I/O	I/O	I/O
83	I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O

Table 53 • **PQ208**

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
58	I/O	WD, I/O	WD, I/O
59	I/O	I/O	I/O
60	VCCI	VCCI	VCCI
61	NC	I/O	I/O
62	NC	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	QCLKA, I/O
66	I/O	WD, I/O	WD, I/O
67	NC	WD, I/O	WD, I/O
68	NC	I/O	I/O
69	I/O	I/O	I/O
70	I/O	WD, I/O	WD, I/O
71	I/O	WD, I/O	WD, I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	GND	GND	GND
79	VCCA	VCCA	VCCA
80	NC	VCCI	VCCI
81	I/O	I/O	I/O
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	WD, I/O	WD, I/O
86	I/O	WD, I/O	WD, I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	NC	I/O	I/O
90	NC	I/O	I/O
91	I/O	I/O	QCLKB, I/O
92	I/O	I/O	I/O
93	I/O	WD, I/O	WD, I/O
94	I/O	WD, I/O	WD, I/O

Table 58 • **CQ208**

CQ208	
Pin Number	**A42MX36 Function**
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	GND
53	GND
54	TMS, I/O
55	TDI, I/O
56	I/O
57	WD, I/O
58	WD, I/O
59	I/O
60	VCCI
61	I/O
62	I/O
63	I/O
64	I/O
65	QCLKA, I/O
66	WD, I/O
67	WD, I/O
68	I/O
69	I/O
70	WD, I/O
71	WD, I/O
72	I/O
73	I/O

Table 61 • **PG132**

PG132	
Pin Number	**A42MX09 Function**
N10	I/O
M10	I/O
N11	I/O
L10	I/O
M11	I/O
N12	SDO
M12	I/O
L11	I/O
N13	I/O
M13	I/O
K11	I/O
L12	I/O
L13	I/O
K13	I/O
H10	I/O
J12	I/O
J13	I/O
H11	I/O
H12	I/O
H13	VKS
G13	VPP