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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	72
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-1pl84

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3.4.9 JTAG Mode Activation

The JTAG test logic circuit is activated in the Designer software by selecting **Tools > Device Selection**. This brings up the Device Selection dialog box as shown in the following figure. The JTAG test logic circuit can be enabled by clicking the “Reserve JTAG Pins” check box. The following table explains the pins' behavior in either mode.

Figure 15 • Device Selection Wizard

Table 11 • Boundary Scan Pin Configuration and Functionality

Reserve JTAG	Checked	Unchecked
TCK	BST input; must be terminated to logical HIGH or LOW to avoid floating	User I/O
TDI, TMS	BST input; may float or be tied to HIGH	User I/O
TDO	BST output; may float or be connected to TDI of another device	User I/O

3.4.10 TRST Pin and TAP Controller Reset

An active reset (TRST) pin is not supported; however, MX devices contain power-on circuitry that resets the boundary scan circuitry upon power-up. Also, the TMS pin is equipped with an internal pull-up resistor. This allows the TAP controller to remain in or return to the Test-Logic-Reset state when there is no input or when a logical 1 is on the TMS pin. To reset the controller, TMS must be HIGH for at least five TCK cycles.

3.4.11 Boundary Scan Description Language (BSDL) File

Conforming to the IEEE Standard 1149.1 requires that the operation of the various JTAG components be documented. The BSDL file provides the standard format to describe the JTAG components that can be used by automatic test equipment software. The file includes the instructions that are supported, instruction bit pattern, and the boundary-scan chain order. For an in-depth discussion on BSDL files, see the *BSDL Files Format Description* application note.

BSDL files are grouped into two categories - generic and device-specific. The generic files assign all user I/Os as inouts. Device-specific files assign user I/Os as inputs, outputs or inouts.

Generic files for MX devices are available on the Microsemi SoC Product Group's website:

<http://www.microsemi.com/soc/techdocs/models/bsdl.html>.

3.5 Development Tool Support

The MX family of FPGAs is fully supported by Libero® Integrated Design Environment (IDE). Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes SynplifyPro from Synopsys, ModelSim® HDL Simulator from Mentor Graphics® and Viewdraw.

Libero IDE includes place-and-route and provides a comprehensive suite of backend support tools for FPGA development, including timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor.

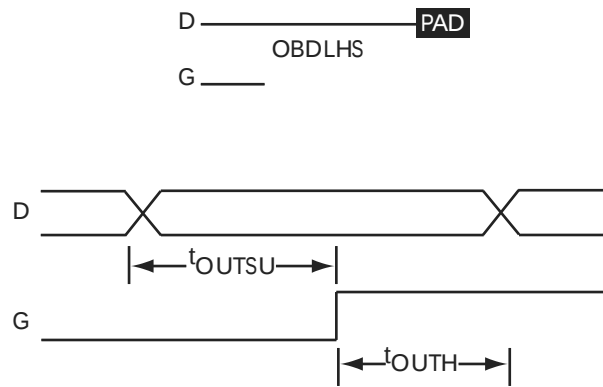
reliability. Devices should not be operated outside the recommended operating conditions.

Table 21 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCCA	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI	3.14 to 3.47	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

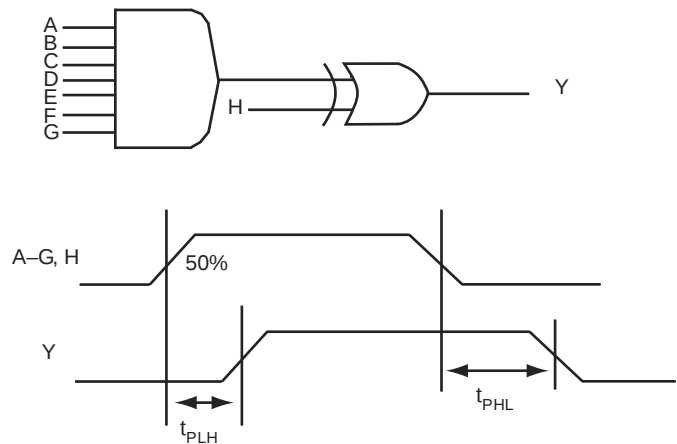
Figure 27 • Output Buffer Latches



3.10.4 Decode Module Timing

The following figure shows decode module timing.

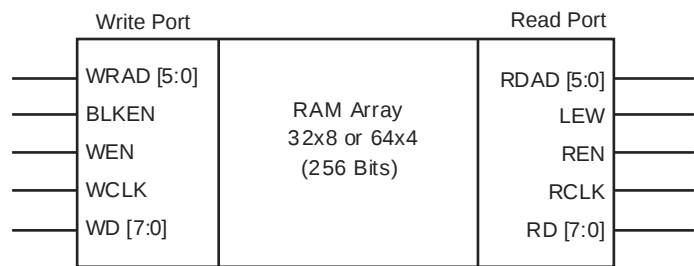
Figure 28 • Decode Module Timing



3.10.5 SRAM Timing Characteristics

The following figure shows SRAM timing characteristics.

Figure 29 • SRAM Timing Characteristics



3.10.6 Dual-Port SRAM Timing Waveforms

The following figures show dual-port SRAM timing waveforms.

approximately a 3 ns to a 6 ns delay, which is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section, shown in Table 34, page 41.

3.11.3 Timing Derating

MX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature and worst-case processing.

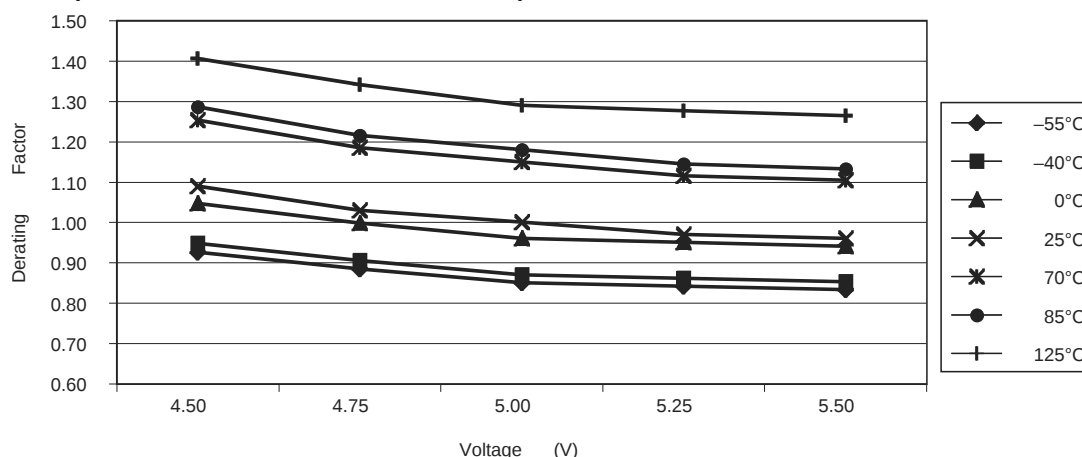
3.11.4 Temperature and Voltage Derating Factors

The following tables and figures show temperature and voltage derating factors for 40MX and 42MX FPGAs.

Table 28 • 42MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 5.0\text{ V}$)

42MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.93	0.95	1.05	1.09	1.25	1.29	1.41
4.75	0.88	0.90	1.00	1.03	1.18	1.22	1.34
5.00	0.85	0.87	0.96	1.00	1.15	1.18	1.29
5.25	0.84	0.86	0.95	0.97	1.12	1.14	1.28
5.50	0.83	0.85	0.94	0.96	1.10	1.13	1.26

Figure 34 • 42MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 5.0\text{ V}$)



Note: This derating factor applies to all routing and propagation delays

Table 29 • 40MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.89	0.93	1.02	1.09	1.25	1.31	1.45
4.75	0.84	0.88	0.97	1.03	1.18	1.24	1.37
5.00	0.82	0.85	0.94	1.00	1.15	1.20	1.33
5.25	0.80	0.82	0.91	0.97	1.12	1.16	1.29
5.50	0.79	0.82	0.90	0.96	1.10	1.15	1.28

Table 33 • Timing Parameters for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{SU(PTP)}$	Input Set-Up Time to CLK—Point-to-Point	10, 12 ²	—	1.5	—	1.5	—	ns
t_H	Input Hold to CLK	0	—	0	—	0	—	ns

1. TOFF is system dependent. MX PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.
2. REQ# and GNT# are point-to-point signals and have different output valid delay and input setup times than do bussed signals. GNT# has a setup of 10; REW# has a setup of 12.

3.11.6.1 Timing Characteristics

The following tables list the timing characteristics.

Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation)
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t _{PD2}	Dual-Module Macros		2.7		3.1		3.5		4.1		5.7	ns
t _{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays ¹												
t _{RD1}	FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.8	ns
t _{RD2}	FO = 2 Routing Delay		1.8		2.1		2.4		2.8		3.9	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.7		3.0		3.6		5.0	ns
t _{RD4}	FO = 4 Routing Delay		2.9		3.3		3.7		4.4		6.1	ns
t _{RD8}	FO = 8 Routing Delay		4.9		5.7		6.5		7.6		10.6	ns
Logic Module Sequential Timing ²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t _A	Flip-Flop Clock Input Period	4.8		5.6		6.3		7.5		10.4		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		181		168		154		134		80	MHz

Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t _{INYH}	Pad-to-Y HIGH		0.7		0.8		0.9		1.1		1.5		ns
t _{INYL}	Pad-to-Y LOW		0.6		0.7		0.8		1.0		1.3		ns
Input Module Predicted Routing Delays ¹													
t _{IRD1}	FO = 1 Routing Delay		2.1		2.4		2.2		3.2		4.5		ns
t _{IRD2}	FO = 2 Routing Delay		2.6		3.0		3.4		4.0		5.6		ns
t _{IRD3}	FO = 3 Routing Delay		3.1		3.6		4.1		4.8		6.7		ns
t _{IRD4}	FO = 4 Routing Delay		3.6		4.2		4.8		5.6		7.8		ns
t _{IRD8}	FO = 8 Routing Delay		5.7		6.6		7.5		8.8		12.4		ns
Global Clock Network													
t _{CKH}	Input Low to HIGH	FO = 16 FO = 128	4.6 4.6		5.3 5.3		6.0 6.0		7.0 7.0		9.8 9.8		ns
t _{CKL}	Input High to LOW	FO = 16 FO = 128	4.8 4.8		5.6 5.6		6.3 6.3		7.4 7.4		10.4 10.4		ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 16 FO = 128	2.2 2.4	2.6 2.7		2.9 3.1		3.4 3.6		4.8 5.1		ns	
t _{PWL}	Minimum Pulse Width LOW	FO = 16 FO = 128	2.2 2.4	2.6 2.7		2.9 3.01		3.4 3.6		4.8 5.1		ns	
t _{CKSW}	Maximum Skew	FO = 16 FO = 128	0.4 0.5		0.5 0.6		0.5 0.7		0.6 0.8		0.8 1.2		ns
t _P	Minimum Period	FO = 16 FO = 128	4.7 4.8	5.4 5.6		6.1 6.3		7.2 7.5		10.0 10.4		ns	
f _{MAX}	Maximum Frequency	FO = 16 FO = 128	188 181		175 168		160 154		139 134		83 80		MHz

Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays ¹													
t _{IRD1}	FO = 1 Routing Delay		2.9		3.3		3.8		4.5		6.3		ns
t _{IRD2}	FO = 2 Routing Delay		3.6		4.2		4.8		5.6		7.8		ns
t _{IRD3}	FO = 3 Routing Delay		4.4		5.0		5.7		6.7		9.4		ns
t _{IRD4}	FO = 4 Routing Delay		5.1		5.9		6.7		7.8		11.0		ns
t _{IRD8}	FO = 8 Routing Delay		8.0		9.3		10.5		12.4		17.2		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 16 FO = 128	6.4 6.4		7.4 7.4		8.4 8.4		9.9 9.9		13.8 13.8		ns
t _{CKL}	Input HIGH to LOW	FO = 16 FO = 128	6.8 6.8		7.8 7.8		8.9 8.9		10.4 10.4		14.6 14.6		ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 16 FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t _{PWL}	Minimum Pulse Width LOW	FO = 16 FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t _{CKSW}	Maximum Skew	FO = 16 FO = 128	0.6 0.8		0.6 0.9		0.7 1.0		0.8 1.2		1.2 1.6		ns
t _P	Minimum Period	FO = 16 FO = 128	6.5 6.8		7.5 7.8		8.5 8.9		10.1 10.4		14.1 14.6		ns
f _{MAX}	Maximum Frequency	FO = 16 FO = 128	113 109		105 101		96 92		83 80		50 48		MHz
TTL Output Module Timing ⁴													
t _{DLH}	Data-to-Pad HIGH		4.7		5.4		6.1		7.2		10.0		ns
t _{DHL}	Data-to-Pad LOW		5.6		6.4		7.3		8.6		12.0		ns
t _{ENZH}	Enable Pad Z to HIGH		5.2		6.0		6.9		8.1		11.3		ns
t _{ENZL}	Enable Pad Z to LOW		6.6		7.6		8.6		10.1		14.1		ns
t _{ENHZ}	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9		ns
t _{ENLZ}	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7		ns
d _{TLH}	Delta LOW to HIGH		0.03		0.03		0.04		0.04		0.06		ns/pF
d _{THL}	Delta HIGH to LOW		0.04		0.04		0.05		0.06		0.08		ns/pF

Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		2.4		2.7		3.1		3.6		5.1	ns
t _{DHL}	Data-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t _{ENZH}	Enable Pad Z to HIGH		2.7		2.9		3.3		3.9		5.5	ns
t _{ENZL}	Enable Pad Z to LOW		2.9		3.2		3.7		4.3		6.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		4.9		5.4		6.2		7.3		10.2	ns
t _{ENLZ}	Enable Pad LOW to Z		5.3		5.9		6.7		7.9		11.1	ns
t _{GLH}	G-to-Pad HIGH		4.2		4.6		5.2		6.1		8.6	ns
t _{GHL}	G-to-Pad LOW		4.2		4.6		5.2		6.1		8.6	ns
t _{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.2		5.8		6.6		7.7		10.8	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.4		8.2		9.3		10.9		15.3	ns
d _{TLH}	Capacity Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF
d _{THL}	Capacity Loading, HIGH to LOW		0.04		0.04		0.04		0.05		0.07	ns/pF

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays ¹												
t _{PD1}	Single Module		1.6		1.8		2.1		2.5		3.5	ns
t _{CO}	Sequential Clock-to-Q		1.8		2.0		2.3		2.7		3.8	ns
t _{GO}	Latch G-to-Q		1.7		1.9		2.1		2.5		3.5	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		2.0		2.2		2.5		2.9		4.1	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		1.0		1.1		1.2		1.4		2.0	ns
t _{RD2}	FO = 2 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t _{RD3}	FO = 3 Routing Delay		1.6		1.8		2.0		2.4		3.3	ns

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Sequential Timing ^{3, 4}												
t _{CO}	Flip-Flop Clock-to-Output		2.1		2.0		2.3		2.7		3.7	ns
t _{GO}	Latch Gate-to-Output		3.4		1.9		2.1		2.5		3.4	ns
t _{SUD}	Flip-Flop (Latch) Set-Up Time	0.4		0.5		0.6		0.7		0.9		ns
t _{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RO}	Flip-Flop (Latch) Reset-to-Output		2.0		2.2		2.5		2.9		4.1	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.2		5.8		6.9		9.6		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.1		6.8		7.7		9.0		12.6		ns
Input Module Propagation Delays												
t _{INPY}	Input Data Pad-to-Y		1.4		1.6		1.8		2.2		3.0	ns
t _{INGO}	Input Latch Gate-to-Output		1.8		1.9		2.2		2.6		3.6	ns
t _{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t _{ILA}	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

Table 47 • PL44

PL44		
Pin Number	A40MX02 Function	A40MX04 Function
21	GND	GND
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	VCC	VCC
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	CLK, I/O	CLK, I/O
34	MODE	MODE
35	VCC	VCC
36	SDI, I/O	SDI, I/O
37	DCLK, I/O	DCLK, I/O
38	PRA, I/O	PRA, I/O
39	PRB, I/O	PRB, I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	GND	GND
44	I/O	I/O

Table 50 • PQ 100

PQ100				
Pin Number	A40MX02 Function	A40MX04 Function	A42MX09 Function	A42MX16 Function
56	VCC	VCC	I/O	I/O
57	I/O	I/O	GND	GND
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	I/O	I/O	I/O	I/O
61	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	GND	GND	I/O	I/O
64	I/O	I/O	LP	LP
65	I/O	I/O	VCCA	VCCA
66	I/O	I/O	VCCI	VCCI
67	I/O	I/O	VCCA	VCCA
68	I/O	I/O	I/O	I/O
69	VCC	VCC	I/O	I/O
70	I/O	I/O	I/O	I/O
71	I/O	I/O	I/O	I/O
72	I/O	I/O	GND	GND
73	I/O	I/O	I/O	I/O
74	I/O	I/O	I/O	I/O
75	I/O	I/O	I/O	I/O
76	I/O	I/O	I/O	I/O
77	NC	NC	I/O	I/O
78	NC	NC	I/O	I/O
79	NC	NC	SDI, I/O	SDI, I/O
80	NC	I/O	I/O	I/O
81	NC	I/O	I/O	I/O
82	NC	I/O	I/O	I/O
83	I/O	I/O	I/O	I/O
84	I/O	I/O	GND	GND
85	I/O	I/O	I/O	I/O
86	GND	GND	I/O	I/O
87	GND	GND	PRA, I/O	PRA, I/O
88	I/O	I/O	I/O	I/O
89	I/O	I/O	CLKA, I/O	CLKA, I/O
90	CLK, I/O	CLK, I/O	VCCA	VCCA
91	I/O	I/O	I/O	I/O
92	MODE	MODE	CLKB, I/O	CLKB, I/O

Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
117	GNDI
118	NC
119	I/O
120	I/O
121	I/O
122	I/O
123	PROBA
124	I/O
125	CLKA
126	VCC
127	VCCI
128	NC
129	I/O
130	CLKB
131	I/O
132	PROBB
133	I/O
134	I/O
135	I/O
136	GND
137	GNDI
138	NC
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	DCLK

Figure 43 • PQ160

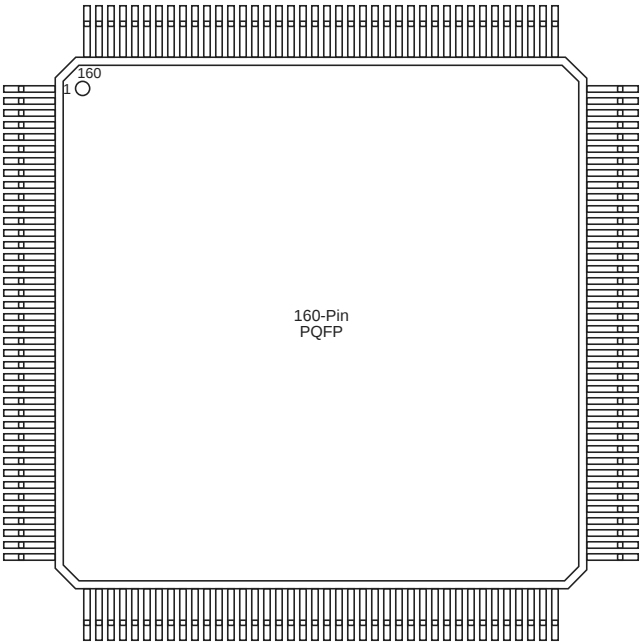


Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	I/O	I/O	I/O
2	DCLK, I/O	DCLK, I/O	DCLK, I/O
3	NC	I/O	I/O
4	I/O	I/O	WD, I/O
5	I/O	I/O	WD, I/O
6	NC	VCCI	VCCI
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	NC	I/O	I/O
11	GND	GND	GND
12	NC	I/O	I/O
13	I/O	I/O	WD, I/O
14	I/O	I/O	WD, I/O
15	I/O	I/O	I/O
16	PRB, I/O	PRB, I/O	PRB, I/O
17	I/O	I/O	I/O
18	CLKB, I/O	CLKB, I/O	CLKB, I/O
19	I/O	I/O	I/O
20	VCCA	VCCA	VCCA

Figure 44 • PQ208

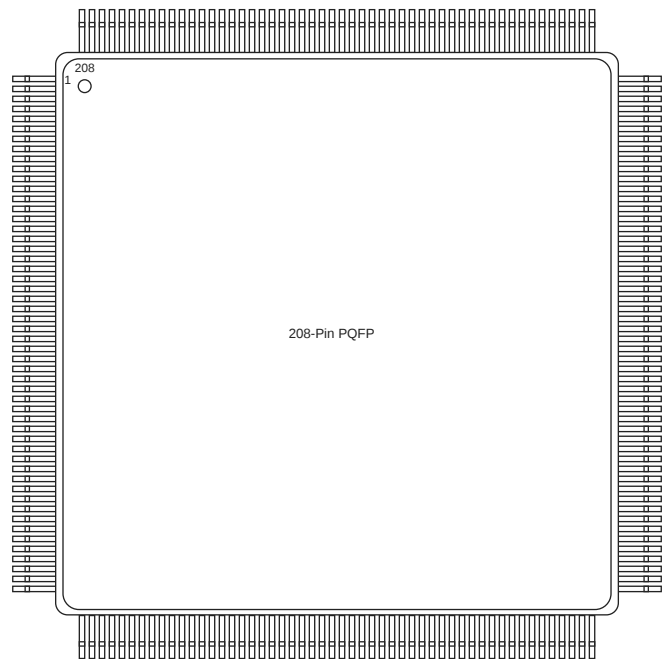


Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
1	GND	GND	GND
2	NC	VCCA	VCCA
3	MODE	MODE	MODE
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	NC	I/O	I/O
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	NC	I/O	I/O
17	VCCA	VCCA	VCCA
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
132	VCCI	VCCI	VCCI
133	VCCA	VCCA	VCCA
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	VCCA	VCCA	VCCA
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	I/O	I/O	I/O
146	NC	I/O	I/O
147	NC	I/O	I/O
148	NC	I/O	I/O
149	NC	I/O	I/O
150	GND	GND	GND
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	I/O	I/O	I/O
156	I/O	I/O	I/O
157	GND	GND	GND
158	I/O	I/O	I/O
159	SDI, I/O	SDI, I/O	SDI, I/O
160	I/O	I/O	I/O
161	I/O	WD, I/O	WD, I/O
162	I/O	WD, I/O	WD, I/O
163	I/O	I/O	I/O
164	VCCI	VCCI	VCCI
165	NC	I/O	I/O
166	NC	I/O	I/O
167	I/O	I/O	I/O
168	I/O	WD, I/O	WD, I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
133	I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	GND
140	I/O
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	I/O
153	I/O
154	I/O
155	VCCA
156	I/O
157	I/O
158	VCCA
159	VCCI
160	GND
161	I/O
162	I/O
163	I/O
164	I/O
165	GND
166	I/O
167	I/O
168	I/O
169	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
207	I/O
208	I/O
209	QCLKC, I/O
210	I/O
211	WD, I/O
212	WD, I/O
213	I/O
214	I/O
215	WD, I/O
216	WD, I/O
217	I/O
218	PRB, I/O
219	I/O
220	CLKB, I/O
221	I/O
222	GND
223	GND
224	VCCA
225	VCCI
226	I/O
227	CLKA, I/O
228	I/O
229	PRA, I/O
230	I/O
231	I/O
232	WD, I/O
233	WD, I/O
234	I/O
235	I/O
236	I/O
237	I/O
238	I/O
239	I/O
240	QCLKD, I/O
241	I/O
242	WD, I/O
243	GND

Table 61 • PG132

PG132	
Pin Number	A42MX09 Function
N10	I/O
M10	I/O
N11	I/O
L10	I/O
M11	I/O
N12	SDO
M12	I/O
L11	I/O
N13	I/O
M13	I/O
K11	I/O
L12	I/O
L13	I/O
K13	I/O
H10	I/O
J12	I/O
J13	I/O
H11	I/O
H12	I/O
H13	VKS
G13	VPP

Table 61 • PG132

PG132	
Pin Number	A42MX09 Function
G12	VSV
F13	I/O
F12	I/O
F11	I/O
F10	I/O
E13	I/O
D13	I/O
D12	I/O
C13	I/O
B13	I/O
D11	I/O
C12	I/O
A13	I/O
C11	I/O
B12	SDI
B11	I/O
C10	I/O
A12	I/O
A11	I/O
B10	I/O
D8	I/O
A10	I/O
C8	I/O
A9	I/O
B8	PRBA
A8	I/O
B7	CLKA
A7	I/O
B6	CLKB
A6	I/O
C6	PRBB
A5	I/O
D6	I/O
A4	I/O
B4	I/O
A3	I/O
C4	I/O