

Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

E·XFI

Product Status	Obsolete
Number of LABs/CLBs	· ·
Number of Logic Elements/Cells	·
Total RAM Bits	
Number of I/O	72
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-1pl84m

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 1 • Product profile

Device	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
Maximum Flip-Flops	147	273	516	928	1,410	1,822
Clocks	1	1	2	2	2	6
User I/O (maximum)	57	69	104	140	176	202
PCI	-	-	_	-	Yes	Yes
Boundary Scan Test (BST)	-	-	_	-	Yes	Yes
Packages (by pin count)						
PLCC	44, 68	44, 68, 84	84	84	84	-
PQFP	100	100	100, 144, 160	100, 160, 208	160, 208	208, 240
VQFP	80	80	100	100	_	_
TQFP	_	_	176	176	176	_
CQFP	_	_	_	172	_	208, 256
PBGA	_	_	_	_	_	272
CPGA	_	_	132	_	-	_

2.4 Plastic Device Resources

Table 2 • Plastic Device Resources

	User I/	Os										
Device	PLCC 44-Pin	PLCC 68-Pin	PLCC 84-Pin	PQFP 100-Pin	PQFP 144- Pin	PQFP 160-Pin	PQFP 208- Pin	PQFP 240-Pin	VQFP 80-Pin	VQFP 100- Pin	TQFP 176- Pin	PBGA 272- Pin
A40MX02	34	57	-	57	_	_	_	_	57	-	-	_
A40MX04	34	57	69	69	-	_	-	_	69	-	-	_
A42MX09	-	-	72	83	95	101	-	_	-	83	104	_
A42MX16	-	-	72	83	-	125	140	_	-	83	140	_
A42MX24	-	-	72	_	-	125	176	_	-	-	150	_
A42MX36	-	_	_	_	_	-	176	202	_	-	-	202

Note: Package Definitions: PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array

2.5 Ceramic Device Resources

Table 3 • Ceramic Device Resources

	User I/Os										
Device	CPGA 132-Pin	CQFP 172-Pin	CQFP 208-Pin	CQFP 256-Pin							
A42MX09	95										
A42MX16		131									
A42MX36			176	202							

Note: Package Definitions: CQFP = Ceramic Quad Flat Pack

2.6 Temperature Grade Offerings

Table 4 • Temperature Grade Offerings

Package	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PLCC 44	C, I, M	C, I, M				
PLCC 68	C, I, A, M	C, I, M				
PLCC 84		C, I, A, M	C, I, A, M	C, I, M	C, I, M	
PQFP 100	C, I, A, M	C, I, A, M	C, I, A, M	C, I, M		
PQFP 144			С			
PQFP 160			C, I, A, M	C, I, M	C, I, A, M	
PQFP 208				C, I, A, M	C, I, A, M	C, I, A, M
PQFP 240						C, I, A, M
VQFP 80	C, I, A, M	C, I, A, M				
VQFP 100			C, I, A, M	C, I, A, M		
TQFP 176			C, I, A, M	C, I, A, M	C, I, A, M	
PBGA 272						C, I, M
CQFP 172				С, М, В		
CQFP 208						C, M, B
CQFP 256						C, M, B
CPGA 132			С, М, В			

Note: C = Commercial

- I = Industrial
 - A = Automotive
 - M = Military

B = MIL-STD-883 Class B

2.7 Speed Grade Offerings

Table 5 •Speed Grade Offerings

	– F	Std	-1	-2	-3
С	Р	Р	Р	Р	Р
I		Р	Р	Р	Р
А		Р			
М		Ρ	Р		
В		Ρ	Р		

Note: See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local Microsemi Sales representative for device availability.

Figure 2 • 42MX C-Module Implementation



The 42MX devices contain three types of logic modules: combinatorial (C-modules), sequential (S-modules) and decode (D-modules). The following figure illustrates the combinatorial logic module. The S-module, shown in Figure 4, page 8, implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D-flip-flop or a transparent latch. The S-module register can be bypassed so that it implements purely combinatorial logic.





Figure 8 • Clock Networks of 42MX Devices



Figure 9 • Quadrant Clock Network of A42MX36 Devices



Note: *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

3.2.5 MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 10, page 12 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (See the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 10, page 12). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. See the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 μ A.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 11, page 12). When the PCI fuse is not programmed, the output drive is standard.

Figure 13 • Silicon Explorer II Setup with 42MX



Table 8 • Device Configuration Options for Probe Capability

Security Fuse(s) Programmed	Mode	PRA, PRB ¹	SDI, SDO, DCLK ¹			
No	LOW	User I/Os ²	User I/Os ²			
No	HIGH	Probe Circuit Outputs	Probe Circuit Inputs			
Yes	_	Probe Circuit Secured	Probe Circuit Secured			

1. Avoid using SDI, SDO, DCLK, PRA and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.

2. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. See the Pin Descriptions, page 83 for information on unused I/O pins

3.4.7 Design Consideration

It is recommended to use a series 70Ω termination resistor on every probe connector (SDI, SDO, MODE, DCLK, PRA and PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

3.4.8 IEEE Standard 1149.1 Boundary Scan Test (BST) Circuitry

42MX24 and 42MX36 devices are compatible with IEEE Standard 1149.1 (informally known as Joint Testing Action Group Standard or JTAG), which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic MX boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers and instruction register (Figure 14, page 18). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and some optional instructions. Table 9, page 18 describes the ports that control JTAG testing, while Table 10, page 18 describes the test instructions supported by these MX devices.

Each test section is accessed through the TAP, which has four associated pins: TCK (test clock input), TDI and TDO (test data input and output), and TMS (test mode selector).

The TAP controller is a four-bit state machine. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles.

42MX24 and 42MX36 devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

3. All outputs unloaded. All inputs = VCC/VCCI or GND

3.8 3.3 V Operating Conditions

The following table shows 3.3 V operating conditions.

Table 16 • Absolute Maximum Ratings for 40MX Devices*

Symbol	Parameter	Limits	Units		
VCC	DC Supply Voltage	–0.5 to +7.0	V		
VI	Input Voltage	-0.5 to VCC + 0.5	V		
VO	Output Voltage	-0.5 to VCC + 0.5	V		
t _{STG}	Storage Temperature	-65 to + 150	°C		

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 17 • Absolute Maximum Ratings for 42MX Devices*

Symbol	Parameter	Limits	Units	
VCCI	DC Supply Voltage for I/Os	-0.5 to +7.0	V	
VCCA	DC Supply Voltage for Array	-0.5 to +7.0	V	
VI	Input Voltage	-0.5 to VCCI+0.5	V	
VO	Output Voltage	-0.5 to VCCI+0.5	V	
t _{STG}	Storage Temperature	-65 to +150	°C	

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 18 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	-40 to +85	-55 to +125	°C
VCC (40MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCA (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCI (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

All the following tables show various specifications and operating conditions of 40MX and 42MX FPGAs.

Figure 30 • 42MX SRAM Write Operation



Note: Identical timing for falling edge clock











		–3 Speed		-2 Speed -1 Speed		Std Speed		-F Speed				
Param	eter / Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{THL}	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

Table 36 •A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued) (Worst-Case Commercial
Conditions, VCC = 4.75 V, T_J = 70°C)

		−3 Speed −2 Speed −1 S		–1 Sp	-1 Speed Std Speed		–F Speed						
Parameter	/ Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Input Mod	ule Predicted Routing	Delays ²											
t _{IRD1}	FO = 1 Routing Delay			1.8		2.0		2.3		2.7		3.8	ns
t _{IRD2}	FO = 2 Routing Delay			2.1		2.3		2.6		3.1		4.3	ns
t _{IRD3}	FO = 3 Routing Delay			2.3		2.5		2.9		3.4		4.8	ns
t _{IRD4}	FO = 4 Routing Delay			2.5		2.8		3.2		3.7		5.2	ns
t _{IRD8}	FO = 8 Routing Delay			3.4		3.8		4.3		5.1		7.1	ns
Global Clo	ock Network												
t _{СКН}	Input LOW to HIGH	FO = 32 FO = 486		2.6 2.9		2.9 3.2		3.3 3.6		3.9 4.3		5.4 5.9	ns ns
t _{CKL}	Input HIGH to LOW	FO = 32 FO = 486		3.7 4.3		4.1 4.7		4.6 5.4		5.4 6.3		7.6 8.8	ns ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32 FO = 486	2.2 2.4		2.4 2.6		2.7 3.0		3.2 3.5		4.5 4.9		ns ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32 FO = 486	2.2 2.4		2.4 2.6		2.7 3.0		3.2 3.5		4.5 4.9		ns ns
t _{CKSW}	Maximum Skew	FO = 32 FO = 486		0.5 0.5		0.6 0.6		0.7 0.7		0.8 0.8		1.1 1.1	ns ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 486	0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		ns ns
t _{HEXT}	Input Latch External Hold	FO = 32 FO = 486	2.8 3.3		3.1 3.7		3.5 4.2		4.1 4.9		5.7 6.9		ns ns
t _P	Minimum Period (1/f _{MAX})	FO = 32 FO = 486	4.7 5.1		5.2 5.7		5.7 6.2		6.5 7.1		10.9 11.9		ns ns

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

		–3 S	peed	–2 S	peed	–1 Sp	beed	Std S	peed	–F Sp	beed	
Parame	ter / Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
TTL Out	tput Module Timing ⁵ (Continued)											
t _{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t _{GLH}	G-to-Pad HIGH		2.9		3.3		3.7		4.4		6.1	ns
t _{GHL}	G-to-Pad LOW		2.9		3.3		3.7		4.4		6.1	ns
t _{LSU}	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

Table 44 •A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions,
VCCA = 4.75 V, T_J = 70°C)

Input, output, tristate or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/Os pins are configured by the Designer software as shown in Table 46, page 84.

Device	Configuration
A40MX02, A40MX04	Pulled LOW
A42MX09, A42MX16	Pulled LOW
A42MX24, A42MX36	Tristated

Table 46 • Configuration of Unused I/Os

In all cases, it is recommended to tie all unused MX I/O pins to LOW on the board. This applies to all dual-purpose pins when configured as I/Os as well.

LP, Low Power Mode

Controls the low power mode of all 42MX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation in 200 µs after the LP pin is driven to a logic LOW.

MODE, Mode

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). The MODE pin is held HIGH to provide verification capability. The MODE pin should be terminated to GND through a $10k\Omega$ resistor so that the MODE pin can be pulled HIGH when required.

NC, No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O

PRB, I/OProbe A/B

The Probe pin is used to output data from any user-defined design node within the device. Each diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. The Probe pin is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

QCLKA/B/C/D, I/O Quadrant Clock

Quadrant clock inputs for A42MX36 devices. When not used as a register control signal, these pins can function as user I/Os.

SDI, I/OSerial Data Input

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDO, I/OSerial Data Output

Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. SDO is available for 42MX devices only.

When Silicon Explorer II is being used, SDO will act as an output while the "checksum" command is run. It will return to user I/O when "checksum" is complete.

TCK, I/O Test Clock

4 Package Pin Assignments

The following figures and tables give the details of the package pin assignments.

Figure 38 • PL44



Table 47 • PL44

PL44		
Pin Number	A40MX02 Function	A40MX04 Function
1	I/O	I/O
2	I/O	I/O
3	VCC	VCC
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	GND	GND
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	VCC	VCC
15	I/O	I/O
16	VCC	VCC
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O

Table 49 • PL84



Table 50 • PQ 100

PQ100				
Pin Number	A40MX02 Function	A40MX04 Function	A42MX09 Function	A42MX16 Function
1	NC	NC	I/O	I/O
2	NC	NC	DCLK, I/O	DCLK, I/O
3	NC	NC	I/O	I/O
4	NC	NC	MODE	MODE
5	NC	NC	I/O	I/O
6	PRB, I/O	PRB, I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	GND	GND
10	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O
13	GND	GND	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	VCCA	VCCA
17	I/O	I/O	VCCI	VCCA
18	I/O	I/O	I/O	I/O

PQ144	
Pin Number	A42MX09 Function
6	I/O
7	I/O
8	I/O
9	GNDQ
10	GNDI
11	NC
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	VSV
19	VCC
20	VCCI
21	NC
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	GND
29	GNDI
30	NC
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	BININ
38	BINOUT
39	I/O
40	I/O
41	I/O
42	I/O

Table 51 • PQ144

Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
58	VCCI	VCCI	VCCI
59	GND	GND	GND
60	VCCA	VCCA	VCCA
61	LP	LP	LP
62	I/O	I/O	TCK, I/O
63	I/O	I/O	I/O
64	GND	GND	GND
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	I/O	I/O	I/O
69	GND	GND	GND
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	I/O	I/O	I/O
77	NC	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	GND	GND	GND
81	I/O	I/O	I/O
82	SDO, I/O	SDO, I/O	SDO, TDO, I/O
83	I/O	I/O	WD, I/O
84	I/O	I/O	WD, I/O
85	I/O	I/O	I/O
86	NC	VCCI	VCCI
87	I/O	I/O	I/O
88	I/O	I/O	WD, I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
206	I/O	I/O	I/O
207	DCLK, I/O	DCLK, I/O	DCLK, I/O
208	I/O	I/O	I/O

Figure 45 • PQ240



Note: This figure shows the 240-Pin PQFP Package top view.

Table 54 • PQ240

PQ240		
Pin Number	A42MX36 Function	
1	I/O	
2	DCLK, I/O	
3	I/O	
4	I/O	
5	I/O	
6	WD, I/O	
7	WD, I/O	
8	VCCI	
9	I/O	
10	I/O	
11	I/O	
12	I/O	
13	I/O	
14	I/O	

Table 60 • BG	272
BG272	
Pin Number	A42MX36 Function
C3	GND
C4	I/O
C5	WD, I/O
C6	I/O
C7	QCLKC, I/O
C8	I/O
C9	I/O
C10	CLKB
C11	PRA, I/O
C12	WD, I/O
C13	I/O
C14	QCLKD, I/O
C15	I/O
C16	WD, I/O
C17	SDI, I/O
C18	I/O
C19	I/O
C20	I/O
D1	I/O
D2	I/O
D3	I/O
D4	I/O
D5	VCCI
D6	I/O
D7	I/O
D8	VCCA
D9	WD, I/O
D10	VCCI
D11	I/O
D12	VCCI
D13	I/O
D14	VCCI
D15	I/O
D16	VCCA
D17	GND
D18	I/O
D19	I/O

PG132	
Pin Number	A42MX09 Function
N10	I/O
M10	I/O
N11	I/O
L10	I/O
M11	I/O
N12	SDO
M12	I/O
L11	I/O
N13	I/O
M13	I/O
K11	I/O
L12	I/O
L13	I/O
K13	I/O
H10	I/O
J12	I/O
J13	I/O
H11	I/O
H12	I/O
H13	VKS
G13	VPP

Figure 53 • CQ172

Table 62 • CQ172

CQ172		
Pin Number	A42MX16 Function	
1	MODE	
2	I/O	
3	I/O	
4	I/O	
5	I/O	
6	I/O	
7	GND	
8	I/O	
9	I/O	
10	I/O	
11	I/O	
12	VCC	
13	I/O	
14	I/O	
15	I/O	
16	I/O	
17	GND	
18	I/O	
19	I/O	
20	I/O	