Microchip Technology - A42MX16-1PLG84I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	72
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-1plg84i

Contents

Table 1 • **Product profile**

Device	**A40MX02**	**A40MX04**	**A42MX09**	**A42MX16**	**A42MX24**	**A42MX36**
Maximum Flip-Flops	147	273	516	928	1,410	1,822
Clocks	1	1	2	2	2	6
User I/O (maximum)	57	69	104	140	176	202
PCI	–	–	–	–	Yes	Yes
Boundary Scan Test (BST)	–	–	–	–	Yes	Yes
Packages (by pin count)						
PLCC	44, 68	44, 68, 84	84	84	84	–
PQFP	100	100	100, 144, 160	100, 160, 208	160, 208	208, 240
VQFP	80	80	100	100	–	–
TQFP	–	–	176	176	176	–
CQFP	–	–	–	172	–	208, 256
PBGA	–	–	–	–	–	272
CPGA	–	–	132	–	–	–

3 40MX and 42MX FPGAs

3.1 General Description

Microsemi's 40MX and 42MX families offer a cost-effective design solution at 5V. The MX devices are single-chip solutions and provide high performance while shortening the system design and development cycle. MX devices can integrate and consolidate logic implemented in multiple PALs, CPLDs, and FPGAs. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

The MX device architecture is based on Microsemi's patented antifuse technology implemented in a 0.45µm triple-metal CMOS process. With capacities ranging from 3,000 to 54,000 system gates, the MX devices provide performance up to 250 MHz, are live on power-up and have one-fifth the standby power consumption of comparable FPGAs. MX FPGAs provide up to 202 user I/Os and are available in a wide variety of packages and speed grades.

A42MX24 and A42MX36 devices also feature multiPlex I/Os, which support mixed-voltage systems, enable programmable PCI, deliver high-performance operation at both 5.0V and 3.3V, and provide a low-power mode. The devices are fully compliant with the PCI local bus specification (version 2.1). They deliver 200 MHz on-chip operation and 6.1 ns clock-to-output performance.

The 42MX24 and 42MX36 devices include system-level features such as IEEE Standard 1149.1 (JTAG) Boundary Scan Testing and fast wide-decode modules. In addition, the A42MX36 device offers dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The storage elements can efficiently address applications requiring wide data path manipulation and can perform transformation functions such as those required for telecommunications, networking, and DSP.

All MX devices are fully tested over automotive and military temperature ranges. In addition, the largest member of the family, the A42MX36, is available in both CQ208 and CQ256 ceramic packages screened to MIL-STD-883 levels. For easy prototyping and conversion from plastic to ceramic, the CQ208 and PQ208 devices are pin-compatible.

3.2 MX Architectural Overview

The MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within these families are composed of logic modules, I/O modules, routing resources and clock networks, which are the building blocks for fast logic designs. In addition, the A42MX36 device contains embedded dual-port SRAM modules, which are optimized for high-speed data path functions such as FIFOs, LIFOs and scratch pad memory. A42MX24 and A42MX36 also contain wide-decode modules.

3.2.1 Logic Modules

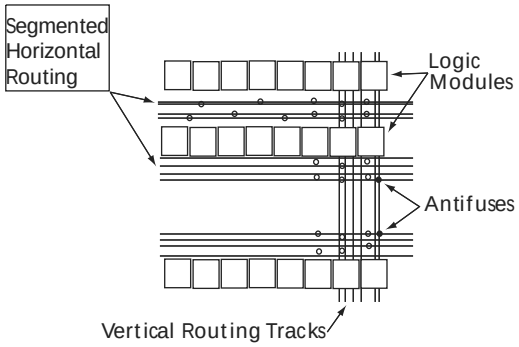
The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources.(see the following figure).

The logic module can implement the four basic logic functions (NAND, AND, OR and NOR) in gates of two, three, or four inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array; latches and flip-flops can be constructed from logic modules whenever required in the application.

3.2.3.3 Antifuse Structures

An antifuse is a “normally open” structure. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient programming algorithms. There are no pre-existing connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For instance, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Figure 7 • **MX Routing Structure**



3.2.4 Clock Networks

The 40MX devices have one global clock distribution network (CLK). A signal can be put on the CLK network by being routed through the CLKBUF buffer.

In 42MX devices, there are two low-skew, high-fanout clock distribution networks, referred to as CLKA and CLKB. Each network has a clock module (CLKMOD) that can select the source of the clock signal from any of the following (Figure 8, page 11):

- Externally from the CLKA pad, using CLKBUF buffer
- Externally from the CLKB pad, using CLKBUF buffer
- Internally from the CLKINTA input, using CLKINT buffer
- Internally from the CLKINTB input, using CLKINT buffer

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

Clock input pads in both 40MX and 42MX devices can also be used as normal I/Os, bypassing the clock networks.

The A42MX36 device has four additional register control resources, called quadrant clock networks (Figure 9, page 11). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

reliability. Devices should not be operated outside the recommended operating conditions.

Table 21 • **Recommended Operating Conditions**

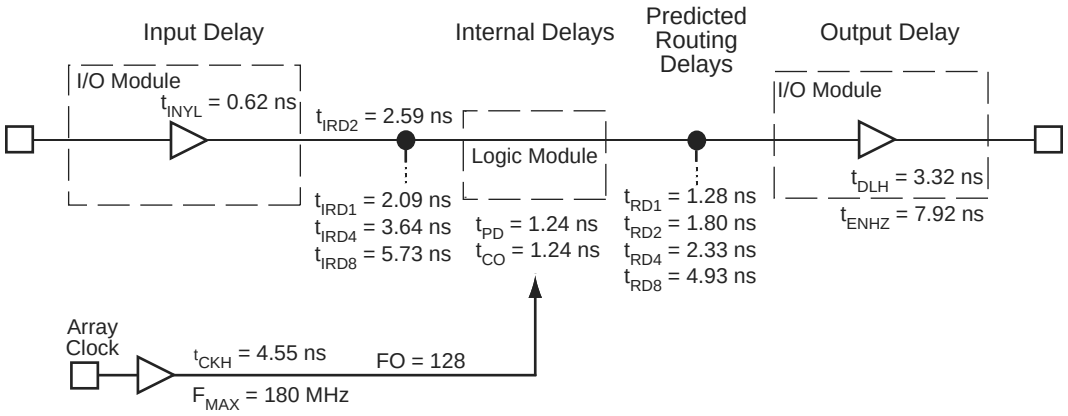
Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCCA	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI	3.14 to 3.47	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

3.10 Timing Models

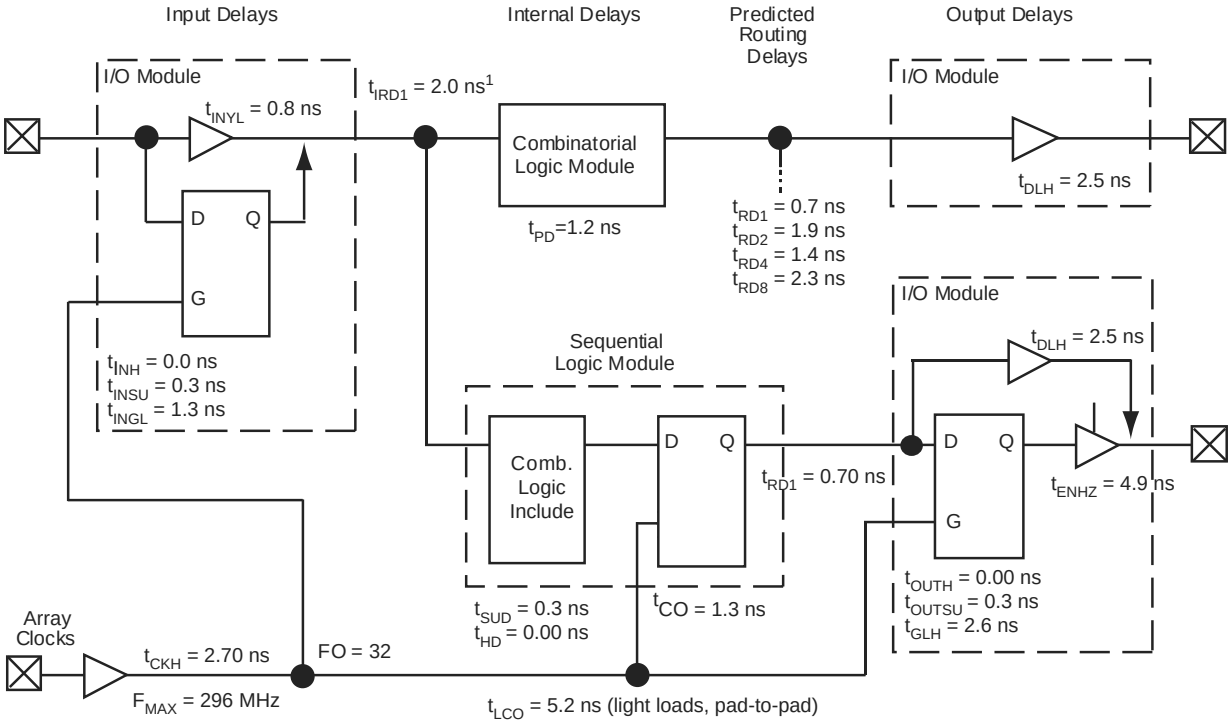
The following figures show various timing models.

Figure 17 • **40MX Timing Model***



Note: Values are shown for 40MX –3 speed devices at 5.0 V worst-case commercial conditions.

Figure 18 • **42MX Timing Model**



Note: 1. Input module predicted routing delay

Note: 2. Values are shown for A42MX09 –3 at 5.0 V worst-case commercial conditions.

Figure 22 • **AC Test Loads**

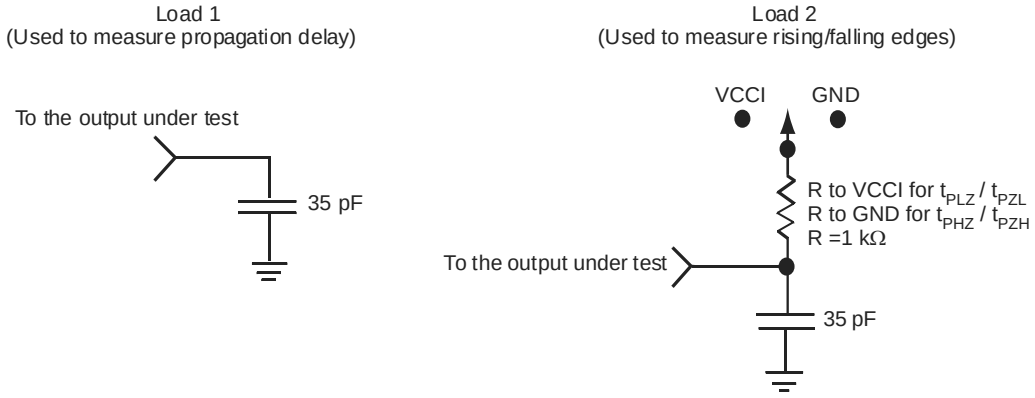


Figure 23 • **Input Buffer Delays**

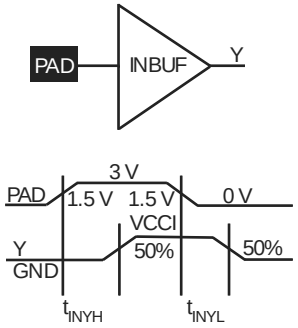


Figure 24 • **Module Delays**

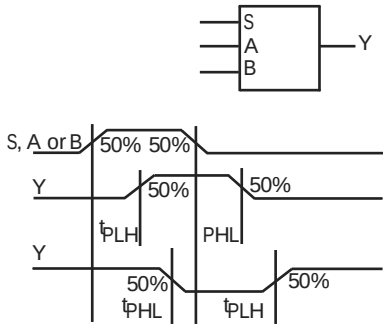
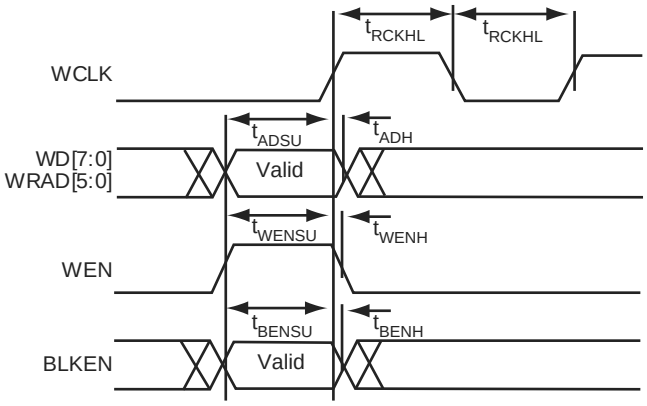
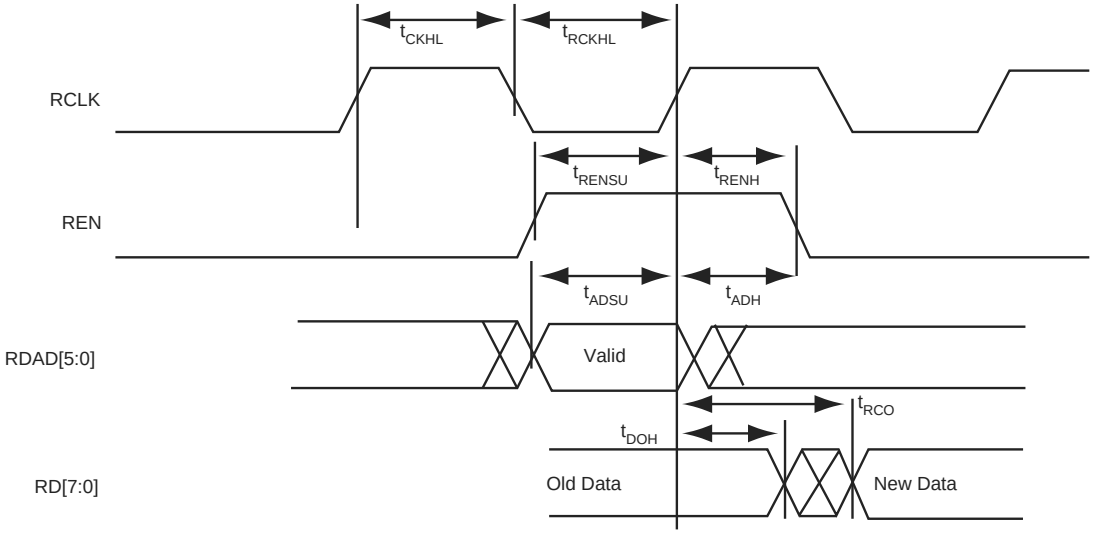


Figure 30 • **42MX SRAM Write Operation**



Note: Identical timing for falling edge clock

Figure 31 • **42MX SRAM Synchronous Read Operation**



Note: Identical timing for falling edge clock

Figure 32 • **42MX SRAM Asynchronous Read Operation—Type 1 (Read Address Controlled)**

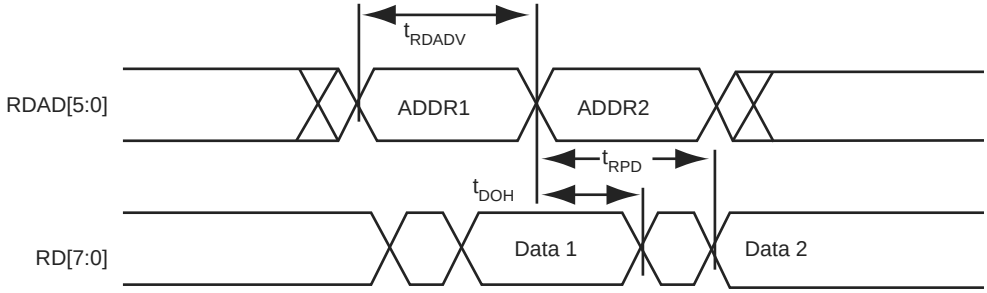


Table 36 • **A40MX04 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

Table 39 • **A42MX09 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RD4}	FO = 4 Routing Delay		1.9		2.1		2.4		2.9		4.0	ns
t_{RD8}	FO = 8 Routing Delay		3.2		3.6		4.1		4.8		6.7	ns
Logic Module Sequential Timing [3, 4]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.5		0.5		0.6		0.7		0.9		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.7		5.3		6.0		7.0		9.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.2		6.9		7.8		9.2		12.9		ns
t_A	Flip-Flop Clock Input Period	5.0		5.6		6.2		7.1		9.9		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		161		146		135		117		70	MHz

Table 43 • **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			2.6		2.9		3.2		3.8		5.3	ns
t_{IRD2}	FO = 2 Routing Delay			2.9		3.2		3.6		4.3		6.0	ns
t_{IRD3}	FO = 3 Routing Delay			3.2		3.6		4.0		4.8		6.6	ns
t_{IRD4}	FO = 4 Routing Delay			3.5		3.9		4.4		5.2		7.3	ns
t_{IRD8}	FO = 8 Routing Delay			4.8		5.3		6.1		7.1		10.0	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		4.4		4.8		5.5		6.5		9.1	ns
		FO = 486		4.8		5.3		6.0		7.1		10.0	ns
t_{CKL}	Input HIGH to LOW	FO = 32		5.1		5.7		6.4		7.6		10.6	ns
		FO = 486		6.0		6.6		7.5		8.8		12.4	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	3.0		3.3		3.8		4.5		6.3		ns
		FO = 486	3.3		3.7		4.2		4.9		6.9		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	3.0		3.4		3.8		4.5		6.3		ns
		FO = 486	3.3		3.7		4.2		4.9		6.9		ns
t_{CKSW}	Maximum Skew	FO = 32		0.8		0.8		1.0		1.1		1.6	ns
		FO = 486		0.8		0.8		1.0		1.1		1.6	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 486	0.0		0.0		0.0		0.0		0.0		ns
TTL Output Module Timing[5]													
t_{DLH}	Data-to-Pad HIGH			3.4		3.8		4.3		5.0		7.1	ns
t_{DHL}	Data-to-Pad LOW			4.0		4.4		5.0		5.9		8.3	ns
t_{ENZH}	Enable Pad Z to HIGH			3.6		4.0		4.5		5.3		7.4	ns
t_{ENZL}	Enable Pad Z to LOW			3.9		4.4		5.0		5.8		8.2	ns
t_{ENHZ}	Enable Pad HIGH to Z			7.2		8.0		9.1		10.7		14.9	ns
t_{ENLZ}	Enable Pad LOW to Z			6.7		7.5		8.5		9.9		13.9	ns
t_{GLH}	G-to-Pad HIGH			4.8		5.3		6.0		7.2		10.0	ns
t_{GHL}	G-to-Pad LOW			4.8		5.3		6.0		7.2		10.0	ns
t_{LSU}	I/O Latch Output Set-Up		0.7		0.7		0.8		1.0		1.4		ns

Figure 42 • **PQ144**

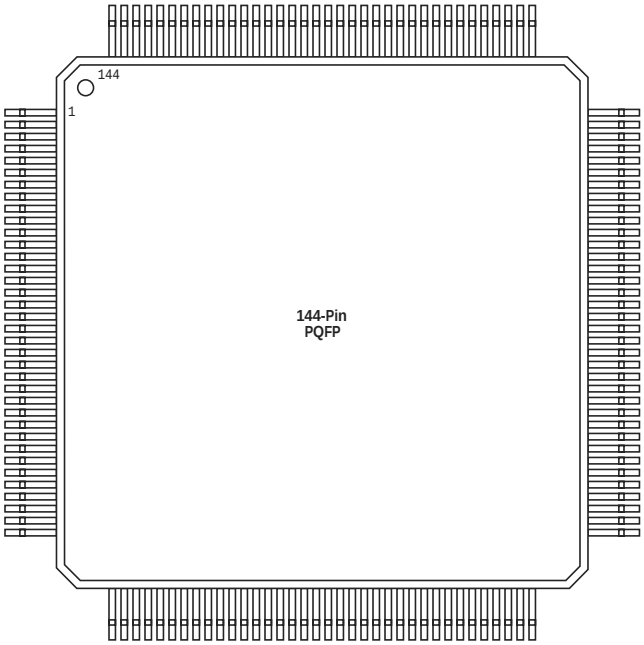


Table 51 • **PQ144**

PQ144	
Pin Number	**A42MX09 Function**
1	I/O
2	MODE
3	I/O
4	I/O
5	I/O

Table 51 • **PQ144**

PQ144	
Pin Number	**A42MX09 Function**
43	I/O
44	GNDQ
45	GNDI
46	NC
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	VCC
55	VCCI
56	NC
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	GND
65	GNDI
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	SDO
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	GNDQ

Table 53 • **PQ208**

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
95	NC	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	VCCI	VCCI	VCCI
99	I/O	I/O	I/O
100	I/O	WD, I/O	WD, I/O
101	I/O	WD, I/O	WD, I/O
102	I/O	I/O	I/O
103	SDO, I/O	SDO, TDO, I/O	SDO, TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	VCCA	VCCA
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	NC	I/O	I/O
113	NC	I/O	I/O
114	NC	I/O	I/O
115	NC	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	I/O	I/O	I/O
126	GND	GND	GND
127	I/O	I/O	I/O
128	I/O	TCK, I/O	TCK, I/O
129	LP	LP	LP
130	VCCA	VCCA	VCCA
131	GND	GND	GND

Table 54 • **PQ240**

PQ240	
Pin Number	**A42MX36 Function**
52	VCCI
53	I/O
54	WD, I/O
55	WD, I/O
56	I/O
57	SDI, I/O
58	I/O
59	VCCA
60	GND
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	VCCI
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	VCCA
86	I/O
87	I/O
88	VCCA

Table 54 • **PQ240**

PQ240	
Pin Number	**A42MX36 Function**
237	GND
238	MODE
239	VCCA
240	GND

Figure 46 • **VQ80**

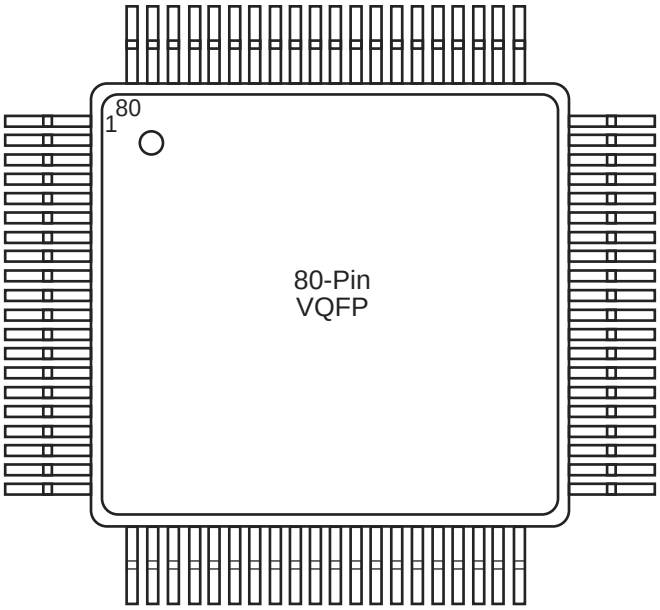


Table 55 • **VQ80**

VQ80		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
1	I/O	I/O
2	NC	I/O
3	NC	I/O
4	NC	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	GND
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O

Table 55 • **VQ80**

VQ80		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
49	I/O	I/O
50	CLK, I/O	CLK, I/O
51	I/O	I/O
52	MODE	MODE
53	VCC	VCC
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	GND	GND
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	VCC	**VCC**
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
59	I/O
60	VCCA
61	GND
62	GND
63	NC
64	NC
65	NC
66	I/O
67	SDO, TDO, I/O
68	I/O
69	WD, I/O
70	WD, I/O
71	I/O
72	VCCI
73	I/O
74	I/O
75	I/O
76	WD, I/O
77	GND
78	WD, I/O
79	I/O
80	QCLKB, I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	WD, I/O
88	WD, I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	VCCI

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
96	VCCA
97	GND
98	GND
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	WD, I/O
106	WD, I/O
107	I/O
108	I/O
109	WD, I/O
110	WD, I/O
111	I/O
112	QCLKA, I/O
113	I/O
114	GND
115	I/O
116	I/O
117	I/O
118	I/O
119	VCCI
120	I/O
121	WD, I/O
122	WD, I/O
123	I/O
124	I/O
125	I/O
126	I/O
127	GND
128	NC
129	NC
130	NC
131	GND
132	I/O