



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                                                 |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                                                        |
| Number of LABs/CLBs            | -                                                                                                                                                               |
| Number of Logic Elements/Cells | -                                                                                                                                                               |
| Total RAM Bits                 | -                                                                                                                                                               |
| Number of I/O                  | 83                                                                                                                                                              |
| Number of Gates                | 24000                                                                                                                                                           |
| Voltage - Supply               | 3V ~ 3.6V, 4.75V ~ 5.25V                                                                                                                                        |
| Mounting Type                  | Surface Mount                                                                                                                                                   |
| Operating Temperature          | 0°C ~ 70°C (TA)                                                                                                                                                 |
| Package / Case                 | 100-BQFP                                                                                                                                                        |
| Supplier Device Package        | 100-PQFP (20x14)                                                                                                                                                |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-1pq100">https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-1pq100</a> |

Figure 51 BG272 ..... 145

Figure 52 PG132 ..... 153

Figure 53 CQ172 ..... 158

## 2.6 Temperature Grade Offerings

**Table 4 • Temperature Grade Offerings**

| Package  | A40MX02    | A40MX04    | A42MX09    | A42MX16    | A42MX24    | A42MX36    |
|----------|------------|------------|------------|------------|------------|------------|
| PLCC 44  | C, I, M    | C, I, M    |            |            |            |            |
| PLCC 68  | C, I, A, M | C, I, M    |            |            |            |            |
| PLCC 84  |            | C, I, A, M | C, I, A, M | C, I, M    | C, I, M    |            |
| PQFP 100 | C, I, A, M | C, I, A, M | C, I, A, M | C, I, M    |            |            |
| PQFP 144 |            |            | C          |            |            |            |
| PQFP 160 |            |            | C, I, A, M | C, I, M    | C, I, A, M |            |
| PQFP 208 |            |            |            | C, I, A, M | C, I, A, M | C, I, A, M |
| PQFP 240 |            |            |            |            |            | C, I, A, M |
| VQFP 80  | C, I, A, M | C, I, A, M |            |            |            |            |
| VQFP 100 |            |            | C, I, A, M | C, I, A, M |            |            |
| TQFP 176 |            |            | C, I, A, M | C, I, A, M | C, I, A, M |            |
| PBGA 272 |            |            |            |            |            | C, I, M    |
| CQFP 172 |            |            |            | C, M, B    |            |            |
| CQFP 208 |            |            |            |            |            | C, M, B    |
| CQFP 256 |            |            |            |            |            | C, M, B    |
| CPGA 132 |            |            | C, M, B    |            |            |            |

**Note:** C = Commercial  
 I = Industrial  
 A = Automotive  
 M = Military  
 B = MIL-STD-883 Class B

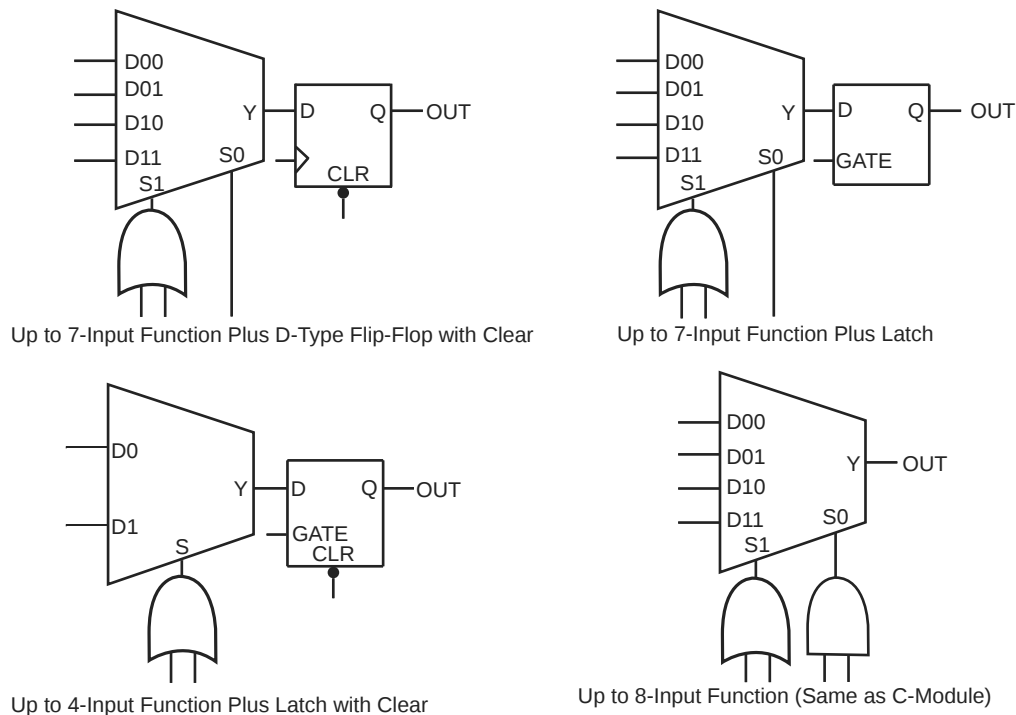
## 2.7 Speed Grade Offerings

**Table 5 • Speed Grade Offerings**

|   | – F | Std | –1 | –2 | –3 |
|---|-----|-----|----|----|----|
| C | P   | P   | P  | P  | P  |
| I |     | P   | P  | P  | P  |
| A |     | P   |    |    |    |
| M |     | P   | P  |    |    |
| B |     | P   | P  |    |    |

**Note:** See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local *Microsemi Sales representative* for device availability.

**Figure 4 • 42MX S-Module Implementation**

A42MX24 and A42MX36 devices contain D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry, providing a fast, wide-input AND function similar to that found in CPLD architectures (Figure 5, page 9). The D-module allows A42MX24 and A42MX36 devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin, and can also be fed back into the array to be incorporated into other logic.

### 3.2.2 Dual-Port SRAM Modules

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the A42MX36 dual-port SRAM block is shown in Figure 6, page 9.

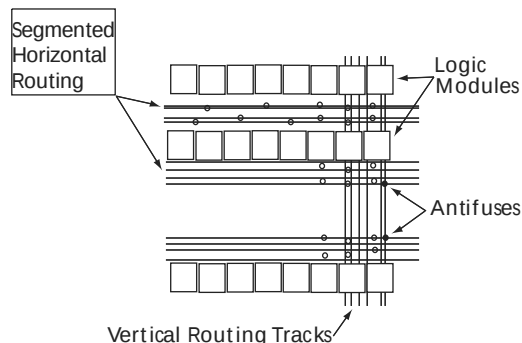
The A42MX36 SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]), which are connected to segmented vertical routing tracks.

The A42MX36 dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring FIFO and LIFO queues. The ACTgen Macro Builder within Microsemi's designer software provides capability to quickly design memory functions with the SRAM blocks. Unused SRAM blocks can be used to implement registers for other user logic within the design.

### 3.2.3.3 Antifuse Structures

An antifuse is a “normally open” structure. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient programming algorithms. There are no pre-existing connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For instance, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

**Figure 7 • MX Routing Structure**



### 3.2.4 Clock Networks

The 40MX devices have one global clock distribution network (CLK). A signal can be put on the CLK network by being routed through the CLKBUF buffer.

In 42MX devices, there are two low-skew, high-fanout clock distribution networks, referred to as CLKA and CLKB. Each network has a clock module (CLKMOD) that can select the source of the clock signal from any of the following (Figure 8, page 11):

- Externally from the CLKA pad, using CLKBUF buffer
- Externally from the CLKB pad, using CLKBUF buffer
- Internally from the CLKINTA input, using CLKINT buffer
- Internally from the CLKINTB input, using CLKINT buffer

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

Clock input pads in both 40MX and 42MX devices can also be used as normal I/Os, bypassing the clock networks.

The A42MX36 device has four additional register control resources, called quadrant clock networks (Figure 9, page 11). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

### 3.8.1 3.3 V LVTTTL Electrical Specifications

**Table 19 • 3.3V LVTTTL Electrical Specifications**

| Symbol                                                   | Parameter                                                                                                                                                                 | Commercial |            | Commercial -F |            | Industrial |            | Military |            | Units |
|----------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------------|---------------|------------|------------|------------|----------|------------|-------|
|                                                          |                                                                                                                                                                           | Min.       | Max.       | Min.          | Max.       | Min.       | Max.       | Min.     | Max.       |       |
| VOH <sup>1</sup>                                         | IOH = -4 mA                                                                                                                                                               | 2.15       |            | 2.15          |            | 2.4        |            | 2.4      |            | V     |
| VOL <sup>1</sup>                                         | IOL = 6 mA                                                                                                                                                                |            | 0.4        |               | 0.4        |            | 0.48       |          | 0.48       | V     |
| VIL                                                      |                                                                                                                                                                           | -0.3       | 0.8        | -0.3          | 0.8        | -0.3       | 0.8        | -0.3     | 0.8        | V     |
| VIH (40MX)                                               |                                                                                                                                                                           | 2.0        | VCC + 0.3  | 2.0           | VCC + 0.3  | 2.0        | VCC + 0.3  | 2.0      | VCC + 0.3  | V     |
| VIH (42MX)                                               |                                                                                                                                                                           | 2.0        | VCCI + 0.3 | 2.0           | VCCI + 0.3 | 2.0        | VCCI + 0.3 | 2.0      | VCCI + 0.3 | V     |
| IIL                                                      |                                                                                                                                                                           |            | -10        |               | -10        |            | -10        |          | -10        | μA    |
| IIH                                                      |                                                                                                                                                                           |            | -10        |               | -10        |            | -10        |          | -10        | μA    |
| Input Transition Time, T <sub>R</sub> and T <sub>F</sub> |                                                                                                                                                                           |            | 500        |               | 500        |            | 500        |          | 500        | ns    |
| C <sub>IO</sub> I/O Capacitance                          |                                                                                                                                                                           |            | 10         |               | 10         |            | 10         |          | 10         | pF    |
| Standby Current, ICC <sup>2</sup>                        | A40MX02, A40MX04                                                                                                                                                          |            | 3          |               | 25         |            | 10         |          | 25         | mA    |
|                                                          | A42MX09                                                                                                                                                                   |            | 5          |               | 25         |            | 25         |          | 25         | mA    |
|                                                          | A42MX16                                                                                                                                                                   |            | 6          |               | 25         |            | 25         |          | 25         | mA    |
|                                                          | A42MX24, A42MX36                                                                                                                                                          |            | 15         |               | 25         |            | 25         |          | 25         | mA    |
| Low-Power Mode Standby Current                           | 42MX devices only                                                                                                                                                         |            | 0.5        |               | ICC - 5.0  |            | ICC - 5.0  |          | ICC - 5.0  | mA    |
| I/O, I/O source sink current                             | Can be derived from the <i>IBIS model</i> ( <a href="http://www.microsemi.com/soc/techdocs/models/ibis.html">http://www.microsemi.com/soc/techdocs/models/ibis.html</a> ) |            |            |               |            |            |            |          |            |       |

1. Only one output tested at a time. VCC/VCCI = min.

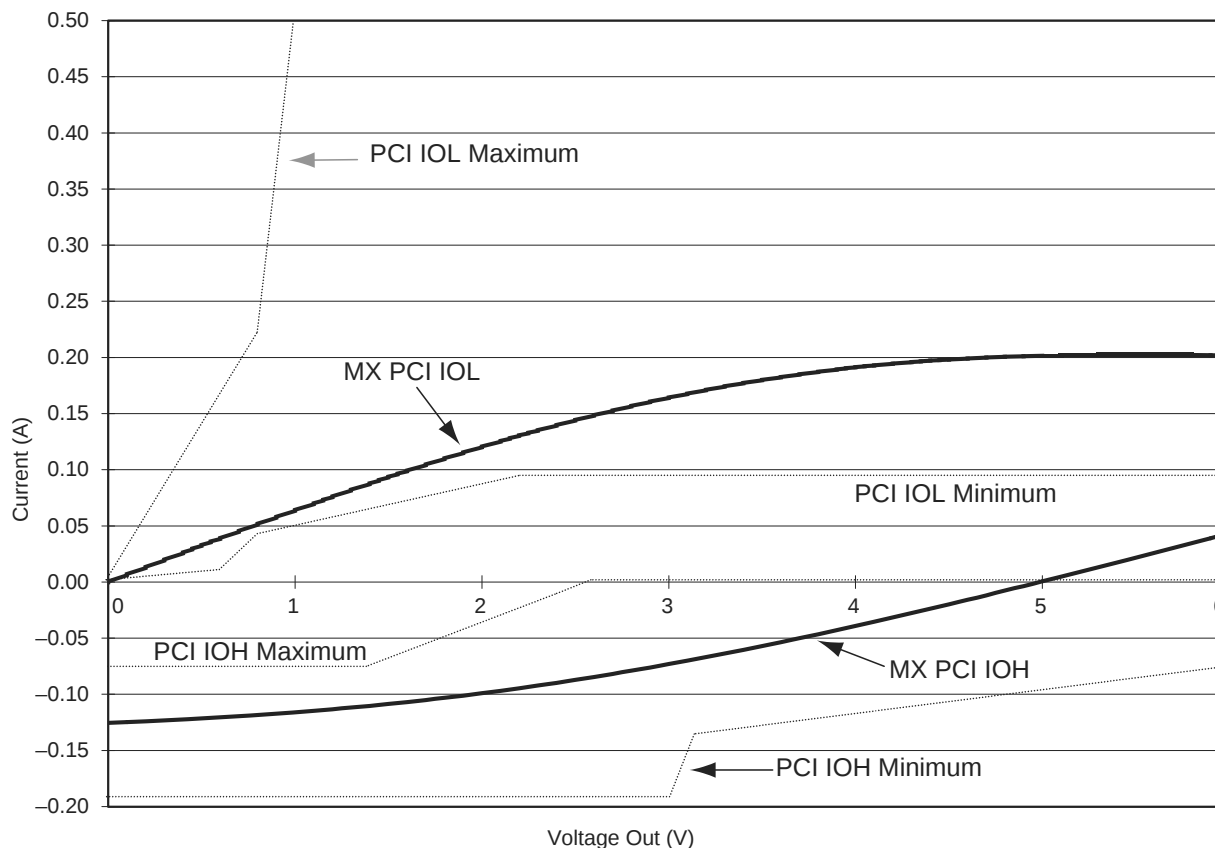
2. All outputs unloaded. All inputs = VCC/VCCI or GND.

## 3.9 Mixed 5.0 V / 3.3 V Operating Conditions (for 42MX Devices Only)

**Table 20 • Absolute Maximum Ratings\***

| Symbol           | Parameter                   | Limits             | Units |
|------------------|-----------------------------|--------------------|-------|
| VCCI             | DC Supply Voltage for I/Os  | -0.5 to +7.0       | V     |
| VCCA             | DC Supply Voltage for Array | -0.5 to +7.0       | V     |
| VI               | Input Voltage               | -0.5 to VCCA + 0.5 | V     |
| VO               | Output Voltage              | -0.5 to VCCI + 0.5 | V     |
| t <sub>STG</sub> | Storage Temperature         | -65 to +150        | °C    |

**Note:** \*Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device

**Figure 16 • Typical Output Drive Characteristics (Based Upon Measured Data)**

### 3.9.4 Junction Temperature ( $T_J$ )

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a(1)$$

EQ 4

where:

- $T_a$  = Ambient Temperature
- $\Delta T$  = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$  (2)
- $P$  = Power
- $\theta_{ja}$  = Junction to ambient of package.  $\theta_{ja}$  numbers are located in Table 27, page 29.

### 3.9.5 Package Thermal Characteristics

The device junction-to-case thermal characteristic is  $\theta_{jc}$ , and the junction-to-ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates.

The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of  $\theta_{ja}$ .

**Table 33 • Timing Parameters for 33 MHz PCI**

| Symbol        | Parameter                               | PCI                 |      | A42MX24 |      | A42MX36 |      | Units |
|---------------|-----------------------------------------|---------------------|------|---------|------|---------|------|-------|
|               |                                         | Min.                | Max. | Min.    | Max. | Min.    | Max. |       |
| $t_{SU(PTP)}$ | Input Set-Up Time to CLK—Point-to-Point | 10, 12 <sup>2</sup> | —    | 1.5     | —    | 1.5     | —    | ns    |
| $t_H$         | Input Hold to CLK                       | 0                   | —    | 0       | —    | 0       | —    | ns    |

1. TOFF is system dependent. MX PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.
2. REQ# and GNT# are point-to-point signals and have different output valid delay and input setup times than do bussed signals. GNT# has a setup of 10; REW# has a setup of 12.

### 3.11.6.1 Timing Characteristics

The following tables list the timing characteristics.

**Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation)**  
**(Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C)**

| Parameter / Description                            |                                                 | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|----------------------------------------------------|-------------------------------------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                                    |                                                 | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| Logic Module Propagation Delays                    |                                                 |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>PD1</sub>                                   | Single Module                                   |          | 1.2  |          | 1.4  |          | 1.6  |           | 1.9  |          | 2.7  | ns    |
| t <sub>PD2</sub>                                   | Dual-Module Macros                              |          | 2.7  |          | 3.1  |          | 3.5  |           | 4.1  |          | 5.7  | ns    |
| t <sub>CO</sub>                                    | Sequential Clock-to-Q                           |          | 1.2  |          | 1.4  |          | 1.6  |           | 1.9  |          | 2.7  | ns    |
| t <sub>GO</sub>                                    | Latch G-to-Q                                    |          | 1.2  |          | 1.4  |          | 1.6  |           | 1.9  |          | 2.7  | ns    |
| t <sub>RS</sub>                                    | Flip-Flop (Latch) Reset-to-Q                    |          | 1.2  |          | 1.4  |          | 1.6  |           | 1.9  |          | 2.7  | ns    |
| Logic Module Predicted Routing Delays <sup>1</sup> |                                                 |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>RD1</sub>                                   | FO = 1 Routing Delay                            |          | 1.3  |          | 1.5  |          | 1.7  |           | 2.0  |          | 2.8  | ns    |
| t <sub>RD2</sub>                                   | FO = 2 Routing Delay                            |          | 1.8  |          | 2.1  |          | 2.4  |           | 2.8  |          | 3.9  | ns    |
| t <sub>RD3</sub>                                   | FO = 3 Routing Delay                            |          | 2.3  |          | 2.7  |          | 3.0  |           | 3.6  |          | 5.0  | ns    |
| t <sub>RD4</sub>                                   | FO = 4 Routing Delay                            |          | 2.9  |          | 3.3  |          | 3.7  |           | 4.4  |          | 6.1  | ns    |
| t <sub>RD8</sub>                                   | FO = 8 Routing Delay                            |          | 4.9  |          | 5.7  |          | 6.5  |           | 7.6  |          | 10.6 | ns    |
| Logic Module Sequential Timing <sup>2</sup>        |                                                 |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>SUD</sub>                                   | Flip-Flop (Latch)<br>Data Input Set-Up          | 3.1      |      | 3.5      |      | 4.0      |      | 4.7       |      | 6.6      |      | ns    |
| t <sub>HD</sub> <sup>3</sup>                       | Flip-Flop (Latch)<br>Data Input Hold            | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>SUENA</sub>                                 | Flip-Flop (Latch)<br>Enable Set-Up              | 3.1      |      | 3.5      |      | 4.0      |      | 4.7       |      | 6.6      |      | ns    |
| t <sub>HENA</sub>                                  | Flip-Flop (Latch) Enable Hold                   | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>WCLKA</sub>                                 | Flip-Flop (Latch)<br>Clock Active Pulse Width   | 3.3      |      | 3.8      |      | 4.3      |      | 5.0       |      | 7.0      |      | ns    |
| t <sub>WASYN</sub>                                 | Flip-Flop (Latch)<br>Asynchronous Pulse Width   | 3.3      |      | 3.8      |      | 4.3      |      | 5.0       |      | 7.0      |      | ns    |
| t <sub>A</sub>                                     | Flip-Flop Clock Input Period                    | 4.8      |      | 5.6      |      | 6.3      |      | 7.5       |      | 10.4     |      | ns    |
| f <sub>MAX</sub>                                   | Flip-Flop (Latch) Clock<br>Frequency (FO = 128) |          | 181  |          | 168  |          | 154  |           | 134  |          | 80   | MHz   |

**Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 3.0 V, T<sub>J</sub> = 70°C)**

| Parameter / Description                |                      | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|----------------------------------------|----------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                        |                      | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| CMOS Output Module Timing <sup>4</sup> |                      |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>DLH</sub>                       | Data-to-Pad HIGH     |          | 5.5  |          | 6.4  |          | 7.2  |           | 8.5  |          | 11.9 | ns    |
| t <sub>DHL</sub>                       | Data-to-Pad LOW      |          | 4.8  |          | 5.5  |          | 6.2  |           | 7.3  |          | 10.2 | ns    |
| t <sub>ENZH</sub>                      | Enable Pad Z to HIGH |          | 4.7  |          | 5.5  |          | 6.2  |           | 7.3  |          | 10.2 | ns    |
| t <sub>ENZL</sub>                      | Enable Pad Z to LOW  |          | 6.8  |          | 7.9  |          | 8.9  |           | 10.5 |          | 14.7 | ns    |
| t <sub>ENHZ</sub>                      | Enable Pad HIGH to Z |          | 11.1 |          | 12.8 |          | 14.5 |           | 17.1 |          | 23.9 | ns    |
| t <sub>ENLZ</sub>                      | Enable Pad LOW to Z  |          | 8.2  |          | 9.5  |          | 10.7 |           | 12.6 |          | 17.7 | ns    |
| d <sub>TLH</sub>                       | Delta LOW to HIGH    |          | 0.05 |          | 0.05 |          | 0.06 |           | 0.07 |          | 0.10 | ns/pF |
| d <sub>THL</sub>                       | Delta HIGH to LOW    |          | 0.03 |          | 0.03 |          | 0.04 |           | 0.04 |          | 0.06 | ns/pF |

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading.

**Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T<sub>J</sub> = 70°C)**

| Parameter / Description                            |                                               | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|----------------------------------------------------|-----------------------------------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                                    |                                               | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| Logic Module Propagation Delays <sup>1</sup>       |                                               |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>PD1</sub>                                   | Single Module                                 |          | 1.2  |          | 1.3  |          | 1.5  |           | 1.8  |          | 2.5  | ns    |
| t <sub>CO</sub>                                    | Sequential Clock-to-Q                         |          | 1.3  |          | 1.4  |          | 1.6  |           | 1.9  |          | 2.7  | ns    |
| t <sub>GO</sub>                                    | Latch G-to-Q                                  |          | 1.2  |          | 1.4  |          | 1.6  |           | 1.8  |          | 2.6  | ns    |
| t <sub>RS</sub>                                    | Flip-Flop (Latch) Reset-to-Q                  |          | 1.2  |          | 1.6  |          | 1.8  |           | 2.1  |          | 2.9  | ns    |
| Logic Module Predicted Routing Delays <sup>2</sup> |                                               |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>RD1</sub>                                   | FO = 1 Routing Delay                          |          | 0.7  |          | 0.8  |          | 0.9  |           | 1.0  |          | 1.4  | ns    |
| t <sub>RD2</sub>                                   | FO = 2 Routing Delay                          |          | 0.9  |          | 1.0  |          | 1.2  |           | 1.4  |          | 1.9  | ns    |
| t <sub>RD3</sub>                                   | FO = 3 Routing Delay                          |          | 1.2  |          | 1.3  |          | 1.5  |           | 1.7  |          | 2.4  | ns    |
| t <sub>RD4</sub>                                   | FO = 4 Routing Delay                          |          | 1.4  |          | 1.5  |          | 1.7  |           | 2.0  |          | 2.9  | ns    |
| t <sub>RD8</sub>                                   | FO = 8 Routing Delay                          |          | 2.3  |          | 2.6  |          | 2.9  |           | 3.4  |          | 4.8  | ns    |
| Logic Module Sequential Timing <sup>3, 4</sup>     |                                               |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>SUD</sub>                                   | Flip-Flop (Latch)<br>Data Input Set-Up        | 0.3      |      | 0.4      |      | 0.4      |      | 0.5       |      | 0.7      |      | ns    |
| t <sub>HD</sub>                                    | Flip-Flop (Latch) Data Input Hold             | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>SUENA</sub>                                 | Flip-Flop (Latch) Enable Set-Up               | 0.4      |      | 0.5      |      | 0.5      |      | 0.6       |      | 0.8      |      | ns    |
| t <sub>HENA</sub>                                  | Flip-Flop (Latch) Enable Hold                 | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>WCLKA</sub>                                 | Flip-Flop (Latch) Clock Active<br>Pulse Width | 3.4      |      | 3.8      |      | 4.3      |      | 5.0       |      | 7.0      |      | ns    |

**Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T<sub>J</sub> = 70°C)**

| Parameter / Description                |                                              | -3 Speed |      | -2 Speed |      | -1 Speed |      | Std Speed |      | -F Speed |      | Units |
|----------------------------------------|----------------------------------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                        |                                              | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| CMOS Output Module Timing <sup>5</sup> |                                              |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>DLH</sub>                       | Data-to-Pad HIGH                             |          | 3.1  |          | 3.5  |          | 3.9  |           | 4.6  |          | 6.4  | ns    |
| t <sub>DHL</sub>                       | Data-to-Pad LOW                              |          | 2.4  |          | 2.6  |          | 3.0  |           | 3.5  |          | 4.9  | ns    |
| t <sub>ENZH</sub>                      | Enable Pad Z to HIGH                         |          | 2.5  |          | 2.8  |          | 3.2  |           | 3.8  |          | 5.3  | ns    |
| t <sub>ENZL</sub>                      | Enable Pad Z to LOW                          |          | 2.8  |          | 3.1  |          | 3.5  |           | 4.2  |          | 5.8  | ns    |
| t <sub>ENHZ</sub>                      | Enable Pad HIGH to Z                         |          | 5.2  |          | 5.7  |          | 6.5  |           | 7.6  |          | 10.7 | ns    |
| t <sub>ENLZ</sub>                      | Enable Pad LOW to Z                          |          | 4.8  |          | 5.3  |          | 6.0  |           | 7.1  |          | 9.9  | ns    |
| t <sub>GLH</sub>                       | G-to-Pad HIGH                                |          | 4.9  |          | 5.4  |          | 6.2  |           | 7.2  |          | 10.1 | ns    |
| t <sub>GHL</sub>                       | G-to-Pad LOW                                 |          | 4.9  |          | 5.4  |          | 6.2  |           | 7.2  |          | 10.1 | ns    |
| t <sub>LSU</sub>                       | I/O Latch Set-Up                             | 0.5      |      | 0.5      |      | 0.6      |      | 0.7       |      | 1.0      |      | ns    |
| t <sub>LH</sub>                        | I/O Latch Hold                               | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>LCO</sub>                       | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O   |          | 5.5  |          | 6.1  |          | 6.9  |           | 8.1  |          | 11.3 | ns    |
| t <sub>ACO</sub>                       | Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O |          | 10.6 |          | 11.8 |          | 13.4 |           | 15.7 |          | 22.0 | ns    |
| d <sub>TLH</sub>                       | Capacitive Loading, LOW to HIGH              |          | 0.04 |          | 0.04 |          | 0.04 |           | 0.05 |          | 0.07 | ns/pF |
| d <sub>THL</sub>                       | Capacitive Loading, HIGH to LOW              |          | 0.03 |          | 0.03 |          | 0.03 |           | 0.04 |          | 0.06 | ns/pF |

1. For dual-module macros, use t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

**Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T<sub>J</sub> = 70°C)**

| Parameter / Description                            |                              | -3 Speed |      | -2 Speed |      | -1 Speed |      | Std Speed |      | -F Speed |      | Units |
|----------------------------------------------------|------------------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                                    |                              | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| Logic Module Combinatorial Functions <sup>1</sup>  |                              |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>PD</sub>                                    | Internal Array Module Delay  |          | 2.0  |          | 1.8  |          | 2.1  |           | 2.5  |          | 3.4  | ns    |
| t <sub>PDD</sub>                                   | Internal Decode Module Delay |          | 1.1  |          | 2.2  |          | 2.5  |           | 3.0  |          | 4.2  | ns    |
| Logic Module Predicted Routing Delays <sup>2</sup> |                              |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>RD1</sub>                                   | FO = 1 Routing Delay         |          | 1.7  |          | 1.3  |          | 1.4  |           | 1.7  |          | 2.3  | ns    |
| t <sub>RD2</sub>                                   | FO = 2 Routing Delay         |          | 2.0  |          | 1.6  |          | 1.8  |           | 2.1  |          | 3.0  | ns    |
| t <sub>RD3</sub>                                   | FO = 3 Routing Delay         |          | 1.1  |          | 2.0  |          | 2.2  |           | 2.6  |          | 3.7  | ns    |
| t <sub>RD4</sub>                                   | FO = 4 Routing Delay         |          | 1.5  |          | 2.3  |          | 2.6  |           | 3.1  |          | 4.3  | ns    |
| t <sub>RD5</sub>                                   | FO = 8 Routing Delay         |          | 1.8  |          | 3.7  |          | 4.2  |           | 5.0  |          | 7.0  | ns    |

**Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T<sub>J</sub> = 70°C)**

| Parameter / Description                        |                                               | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|------------------------------------------------|-----------------------------------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                                |                                               | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| Logic Module Sequential Timing <sup>3, 4</sup> |                                               |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>CO</sub>                                | Flip-Flop Clock-to-Output                     |          | 2.1  |          | 2.0  |          | 2.3  |           | 2.7  |          | 3.7  | ns    |
| t <sub>GO</sub>                                | Latch Gate-to-Output                          |          | 3.4  |          | 1.9  |          | 2.1  |           | 2.5  |          | 3.4  | ns    |
| t <sub>SUD</sub>                               | Flip-Flop (Latch) Set-Up Time                 | 0.4      |      | 0.5      |      | 0.6      |      | 0.7       |      | 0.9      |      | ns    |
| t <sub>HD</sub>                                | Flip-Flop (Latch) Hold Time                   | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>RO</sub>                                | Flip-Flop (Latch) Reset-to-Output             |          | 2.0  |          | 2.2  |          | 2.5  |           | 2.9  |          | 4.1  | ns    |
| t <sub>SUENA</sub>                             | Flip-Flop (Latch) Enable Set-Up               | 0.6      |      | 0.6      |      | 0.7      |      | 0.8       |      | 1.2      |      | ns    |
| t <sub>HENA</sub>                              | Flip-Flop (Latch) Enable Hold                 | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>WCLKA</sub>                             | Flip-Flop (Latch)<br>Clock Active Pulse Width | 4.6      |      | 5.2      |      | 5.8      |      | 6.9       |      | 9.6      |      | ns    |
| t <sub>WASYN</sub>                             | Flip-Flop (Latch)<br>Asynchronous Pulse Width | 6.1      |      | 6.8      |      | 7.7      |      | 9.0       |      | 12.6     |      | ns    |
| Input Module Propagation Delays                |                                               |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>INPY</sub>                              | Input Data Pad-to-Y                           |          | 1.4  |          | 1.6  |          | 1.8  |           | 2.2  |          | 3.0  | ns    |
| t <sub>INGO</sub>                              | Input Latch Gate-to-Output                    |          | 1.8  |          | 1.9  |          | 2.2  |           | 2.6  |          | 3.6  | ns    |
| t <sub>INH</sub>                               | Input Latch Hold                              | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>INSU</sub>                              | Input Latch Set-Up                            | 0.7      |      | 0.7      |      | 0.8      |      | 1.0       |      | 1.4      |      | ns    |
| t <sub>ILA</sub>                               | Latch Active Pulse Width                      | 6.5      |      | 7.3      |      | 8.2      |      | 9.7       |      | 13.5     |      | ns    |

**Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)**(Worst-Case Commercial Conditions, VCCA = 3.0 V, T<sub>J</sub> = 70°C)

| Parameter / Description                                          | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|------------------------------------------------------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                                                  | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| t <sub>ACO</sub> Array Latch Clock-to-Out<br>(Pad-to-Pad) 32 I/O |          | 10.9 |          | 12.1 |          | 13.7 |           | 16.1 |          | 22.5 | ns    |
| d <sub>TLH</sub> Capacitive Loading, LOW to HIGH                 |          | 0.10 |          | 0.11 |          | 0.12 |           | 0.14 |          | 0.20 | ns/pF |
| d <sub>THL</sub> Capacitive Loading, HIGH to LOW                 |          | 0.10 |          | 0.11 |          | 0.12 |           | 0.14 |          | 0.20 | ns/pF |
| <b>CMOS Output Module Timing<sup>5</sup></b>                     |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>DLH</sub> Data-to-Pad HIGH                                |          | 4.9  |          | 5.5  |          | 6.2  |           | 7.3  |          | 10.3 | ns    |
| t <sub>DHL</sub> Data-to-Pad LOW                                 |          | 3.4  |          | 3.8  |          | 4.3  |           | 5.1  |          | 7.1  | ns    |
| t <sub>ENZH</sub> Enable Pad Z to HIGH                           |          | 3.7  |          | 4.1  |          | 4.7  |           | 5.5  |          | 7.7  | ns    |
| t <sub>ENZL</sub> Enable Pad Z to LOW                            |          | 4.1  |          | 4.6  |          | 5.2  |           | 6.1  |          | 8.5  | ns    |
| t <sub>ENHZ</sub> Enable Pad HIGH to Z                           |          | 7.4  |          | 8.2  |          | 9.3  |           | 10.9 |          | 15.3 | ns    |
| t <sub>ENLZ</sub> Enable Pad LOW to Z                            |          | 6.9  |          | 7.6  |          | 8.7  |           | 10.2 |          | 14.3 | ns    |
| t <sub>GLH</sub> G-to-Pad HIGH                                   |          | 7.0  |          | 7.8  |          | 8.9  |           | 10.4 |          | 14.6 | ns    |
| t <sub>GHL</sub> G-to-Pad LOW                                    |          | 7.0  |          | 7.8  |          | 8.9  |           | 10.4 |          | 14.6 | ns    |
| t <sub>LSU</sub> I/O Latch Set-Up                                | 0.7      |      | 0.7      |      | 0.8      |      | 1.0       |      | 1.4      |      | ns    |
| t <sub>LH</sub> I/O Latch Hold                                   | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>LCO</sub> I/O Latch Clock-to-Out<br>(Pad-to-Pad) 32 I/O   |          | 7.9  |          | 8.8  |          | 10.0 |           | 11.8 |          | 16.5 | ns    |

1. For dual-module macros, use t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

## 3.12 Pin Descriptions

This section lists the pin descriptions for 40MX and 42MX series FPGAs.

### CLK/A/B, I/O Global Clock

Clock inputs for clock distribution networks. CLK is for 40MX while CLKA and CLKB are for 42MX devices. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

### DCLK, I/O Diagnostic Clock

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### GND, Ground

Input LOW supply voltage.

### I/O, Input/Output

# 4 Package Pin Assignments

The following figures and tables give the details of the package pin assignments.

Figure 38 • PL44

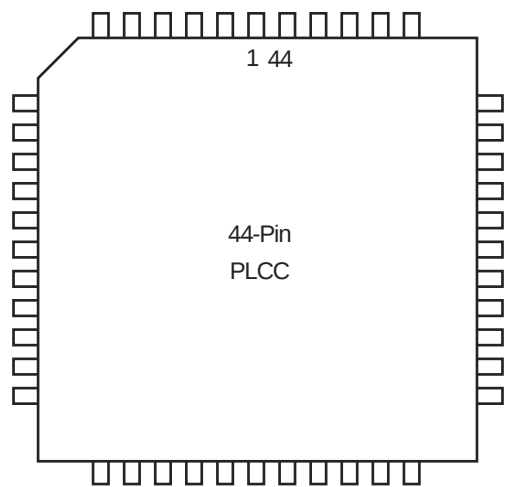


Table 47 • PL44

| PL44       |                  |                  |
|------------|------------------|------------------|
| Pin Number | A40MX02 Function | A40MX04 Function |
| 1          | I/O              | I/O              |
| 2          | I/O              | I/O              |
| 3          | VCC              | VCC              |
| 4          | I/O              | I/O              |
| 5          | I/O              | I/O              |
| 6          | I/O              | I/O              |
| 7          | I/O              | I/O              |
| 8          | I/O              | I/O              |
| 9          | I/O              | I/O              |
| 10         | GND              | GND              |
| 11         | I/O              | I/O              |
| 12         | I/O              | I/O              |
| 13         | I/O              | I/O              |
| 14         | VCC              | VCC              |
| 15         | I/O              | I/O              |
| 16         | VCC              | VCC              |
| 17         | I/O              | I/O              |
| 18         | I/O              | I/O              |
| 19         | I/O              | I/O              |
| 20         | I/O              | I/O              |

**Table 47 • PL44**

| <b>PL44</b>       |                         |                         |
|-------------------|-------------------------|-------------------------|
| <b>Pin Number</b> | <b>A40MX02 Function</b> | <b>A40MX04 Function</b> |
| 21                | GND                     | GND                     |
| 22                | I/O                     | I/O                     |
| 23                | I/O                     | I/O                     |
| 24                | I/O                     | I/O                     |
| 25                | VCC                     | VCC                     |
| 26                | I/O                     | I/O                     |
| 27                | I/O                     | I/O                     |
| 28                | I/O                     | I/O                     |
| 29                | I/O                     | I/O                     |
| 30                | I/O                     | I/O                     |
| 31                | I/O                     | I/O                     |
| 32                | GND                     | GND                     |
| 33                | CLK, I/O                | CLK, I/O                |
| 34                | MODE                    | MODE                    |
| 35                | VCC                     | VCC                     |
| 36                | SDI, I/O                | SDI, I/O                |
| 37                | DCLK, I/O               | DCLK, I/O               |
| 38                | PRA, I/O                | PRA, I/O                |
| 39                | PRB, I/O                | PRB, I/O                |
| 40                | I/O                     | I/O                     |
| 41                | I/O                     | I/O                     |
| 42                | I/O                     | I/O                     |
| 43                | GND                     | GND                     |
| 44                | I/O                     | I/O                     |

**Table 50 • PQ 100**

| <b>PQ100</b>      |                         |                         |                         |                         |
|-------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| <b>Pin Number</b> | <b>A40MX02 Function</b> | <b>A40MX04 Function</b> | <b>A42MX09 Function</b> | <b>A42MX16 Function</b> |
| 93                | VCC                     | VCC                     | I/O                     | I/O                     |
| 94                | VCC                     | VCC                     | PRB, I/O                | PRB, I/O                |
| 95                | NC                      | I/O                     | I/O                     | I/O                     |
| 96                | NC                      | I/O                     | GND                     | GND                     |
| 97                | NC                      | I/O                     | I/O                     | I/O                     |
| 98                | SDI, I/O                | SDI, I/O                | I/O                     | I/O                     |
| 99                | DCLK, I/O               | DCLK, I/O               | I/O                     | I/O                     |
| 100               | PRA, I/O                | PRA, I/O                | I/O                     | I/O                     |

**Table 52 • PQ160**

| <b>PQ160</b>      |                         |                         |                         |
|-------------------|-------------------------|-------------------------|-------------------------|
| <b>Pin Number</b> | <b>A42MX09 Function</b> | <b>A42MX16 Function</b> | <b>A42MX24 Function</b> |
| 95                | I/O                     | I/O                     | I/O                     |
| 96                | I/O                     | I/O                     | WD, I/O                 |
| 97                | I/O                     | I/O                     | I/O                     |
| 98                | VCCA                    | VCCA                    | VCCA                    |
| 99                | GND                     | GND                     | GND                     |
| 100               | NC                      | I/O                     | I/O                     |
| 101               | I/O                     | I/O                     | I/O                     |
| 102               | I/O                     | I/O                     | I/O                     |
| 103               | NC                      | I/O                     | I/O                     |
| 104               | I/O                     | I/O                     | I/O                     |
| 105               | I/O                     | I/O                     | I/O                     |
| 106               | I/O                     | I/O                     | WD, I/O                 |
| 107               | I/O                     | I/O                     | WD, I/O                 |
| 108               | I/O                     | I/O                     | I/O                     |
| 109               | GND                     | GND                     | GND                     |
| 110               | NC                      | I/O                     | I/O                     |
| 111               | I/O                     | I/O                     | WD, I/O                 |
| 112               | I/O                     | I/O                     | WD, I/O                 |
| 113               | I/O                     | I/O                     | I/O                     |
| 114               | NC                      | VCCI                    | VCCI                    |
| 115               | I/O                     | I/O                     | WD, I/O                 |
| 116               | NC                      | I/O                     | WD, I/O                 |
| 117               | I/O                     | I/O                     | I/O                     |
| 118               | I/O                     | I/O                     | TDI, I/O                |
| 119               | I/O                     | I/O                     | TMS, I/O                |
| 120               | GND                     | GND                     | GND                     |
| 121               | I/O                     | I/O                     | I/O                     |
| 122               | I/O                     | I/O                     | I/O                     |
| 123               | I/O                     | I/O                     | I/O                     |
| 124               | NC                      | I/O                     | I/O                     |
| 125               | GND                     | GND                     | GND                     |
| 126               | I/O                     | I/O                     | I/O                     |
| 127               | I/O                     | I/O                     | I/O                     |
| 128               | I/O                     | I/O                     | I/O                     |
| 129               | NC                      | I/O                     | I/O                     |
| 130               | GND                     | GND                     | GND                     |
| 131               | I/O                     | I/O                     | I/O                     |

**Table 54 • PQ240**

| <b>PQ240</b>      |                         |
|-------------------|-------------------------|
| <b>Pin Number</b> | <b>A42MX36 Function</b> |
| 52                | VCCI                    |
| 53                | I/O                     |
| 54                | WD, I/O                 |
| 55                | WD, I/O                 |
| 56                | I/O                     |
| 57                | SDI, I/O                |
| 58                | I/O                     |
| 59                | VCCA                    |
| 60                | GND                     |
| 61                | GND                     |
| 62                | I/O                     |
| 63                | I/O                     |
| 64                | I/O                     |
| 65                | I/O                     |
| 66                | I/O                     |
| 67                | I/O                     |
| 68                | I/O                     |
| 69                | I/O                     |
| 70                | I/O                     |
| 71                | VCCI                    |
| 72                | I/O                     |
| 73                | I/O                     |
| 74                | I/O                     |
| 75                | I/O                     |
| 76                | I/O                     |
| 77                | I/O                     |
| 78                | I/O                     |
| 79                | I/O                     |
| 80                | I/O                     |
| 81                | I/O                     |
| 82                | I/O                     |
| 83                | I/O                     |
| 84                | I/O                     |
| 85                | VCCA                    |
| 86                | I/O                     |
| 87                | I/O                     |
| 88                | VCCA                    |

**Table 54 • PQ240**

| <b>PQ240</b>      |                         |
|-------------------|-------------------------|
| <b>Pin Number</b> | <b>A42MX36 Function</b> |
| 163               | WD, I/O                 |
| 164               | WD, I/O                 |
| 165               | I/O                     |
| 166               | QCLKA, I/O              |
| 167               | I/O                     |
| 168               | I/O                     |
| 169               | I/O                     |
| 170               | I/O                     |
| 171               | I/O                     |
| 172               | VCCI                    |
| 173               | I/O                     |
| 174               | WD, I/O                 |
| 175               | WD, I/O                 |
| 176               | I/O                     |
| 177               | I/O                     |
| 178               | TDI, I/O                |
| 179               | TMS, I/O                |
| 180               | GND                     |
| 181               | VCCA                    |
| 182               | GND                     |
| 183               | I/O                     |
| 184               | I/O                     |
| 185               | I/O                     |
| 186               | I/O                     |
| 187               | I/O                     |
| 188               | I/O                     |
| 189               | I/O                     |
| 190               | I/O                     |
| 191               | I/O                     |
| 192               | VCCI                    |
| 193               | I/O                     |
| 194               | I/O                     |
| 195               | I/O                     |
| 196               | I/O                     |
| 197               | I/O                     |
| 198               | I/O                     |
| 199               | I/O                     |

**Table 58 • CQ208**

| <b>CQ208</b>      |                         |
|-------------------|-------------------------|
| <b>Pin Number</b> | <b>A42MX36 Function</b> |
| 74                | I/O                     |
| 75                | I/O                     |
| 76                | I/O                     |
| 77                | I/O                     |
| 78                | GND                     |
| 79                | VCCA                    |
| 80                | VCCI                    |
| 81                | I/O                     |
| 82                | I/O                     |
| 83                | I/O                     |
| 84                | I/O                     |
| 85                | WD, I/O                 |
| 86                | WD, I/O                 |
| 87                | I/O                     |
| 88                | I/O                     |
| 89                | I/O                     |
| 90                | I/O                     |
| 91                | QCLKB, I/O              |
| 92                | I/O                     |
| 93                | WD, I/O                 |
| 94                | WD, I/O                 |
| 95                | I/O                     |
| 96                | I/O                     |
| 97                | I/O                     |
| 98                | VCCI                    |
| 99                | I/O                     |
| 100               | WD, I/O                 |
| 101               | WD, I/O                 |
| 102               | I/O                     |
| 103               | TDO, I/O                |
| 104               | I/O                     |
| 105               | GND                     |
| 106               | VCCA                    |
| 107               | I/O                     |
| 108               | I/O                     |
| 109               | I/O                     |
| 110               | I/O                     |

**Table 58 • CQ208**

| <b>CQ208</b>      |                         |
|-------------------|-------------------------|
| <b>Pin Number</b> | <b>A42MX36 Function</b> |
| 148               | I/O                     |
| 149               | I/O                     |
| 150               | GND                     |
| 151               | I/O                     |
| 152               | I/O                     |
| 153               | I/O                     |
| 154               | I/O                     |
| 155               | I/O                     |
| 156               | I/O                     |
| 157               | GND                     |
| 158               | I/O                     |
| 159               | SDI, I/O                |
| 160               | I/O                     |
| 161               | WD, I/O                 |
| 162               | WD, I/O                 |
| 163               | I/O                     |
| 164               | VCCI                    |
| 165               | I/O                     |
| 166               | I/O                     |
| 167               | I/O                     |
| 168               | WD, I/O                 |
| 169               | WD, I/O                 |
| 170               | I/O                     |
| 171               | QCLKD, I/O              |
| 172               | I/O                     |
| 173               | I/O                     |
| 174               | I/O                     |
| 175               | I/O                     |
| 176               | WD, I/O                 |
| 177               | WD, I/O                 |
| 178               | PRA, I/O                |
| 179               | I/O                     |
| 180               | CLKA, I/O               |
| 181               | I/O                     |
| 182               | VCCI                    |
| 183               | VCCA                    |
| 184               | GND                     |

**Table 60 • BG272**

| <b>BG272</b>      |                         |
|-------------------|-------------------------|
| <b>Pin Number</b> | <b>A42MX36 Function</b> |
| T19               | I/O                     |
| T20               | I/O                     |
| U1                | I/O                     |
| U2                | I/O                     |
| U3                | I/O                     |
| U4                | I/O                     |
| U5                | VCCI                    |
| U6                | WD, I/O                 |
| U7                | I/O                     |
| U8                | I/O                     |
| U9                | WD, I/O                 |
| U10               | VCCA                    |
| U11               | VCCI                    |
| U12               | I/O                     |
| U13               | I/O                     |
| U14               | QCLKB, I/O              |
| U15               | I/O                     |
| U16               | VCCI                    |
| U17               | I/O                     |
| U18               | GND                     |
| U19               | I/O                     |
| U20               | I/O                     |
| V1                | I/O                     |
| V2                | I/O                     |
| V3                | GND                     |
| V4                | GND                     |
| V5                | I/O                     |
| V6                | I/O                     |
| V7                | I/O                     |
| V8                | WD, I/O                 |
| V9                | I/O                     |
| V10               | I/O                     |
| V11               | I/O                     |
| V12               | I/O                     |
| V13               | WD, I/O                 |
| V14               | I/O                     |
| V15               | WD, I/O                 |