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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

E·XFI

Product Status	Obsolete
Number of LABs/CLBs	
Number of Logic Elements/Cells	·
Total RAM Bits	
Number of I/O	125
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-1pq160

Email: info@E-XFL.COM

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Power Matters."

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2.6 Temperature Grade Offerings

Table 4 • Temperature Grade Offerings

Package	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PLCC 44	C, I, M	C, I, M				
PLCC 68	C, I, A, M	C, I, M				
PLCC 84		C, I, A, M	C, I, A, M	C, I, M	C, I, M	
PQFP 100	C, I, A, M	C, I, A, M	C, I, A, M	C, I, M		
PQFP 144			С			
PQFP 160			C, I, A, M	C, I, M	C, I, A, M	
PQFP 208				C, I, A, M	C, I, A, M	C, I, A, M
PQFP 240						C, I, A, M
VQFP 80	C, I, A, M	C, I, A, M				
VQFP 100			C, I, A, M	C, I, A, M		
TQFP 176			C, I, A, M	C, I, A, M	C, I, A, M	
PBGA 272						C, I, M
CQFP 172				С, М, В		
CQFP 208						С, М, В
CQFP 256						С, М, В
CPGA 132			С, М, В			

Note: C = Commercial

I = Industrial

A = Automotive

M = Military

B = MIL-STD-883 Class B

2.7 Speed Grade Offerings

Table 5 • Speed Grade Offerings

	– F	Std	-1	-2	-3
С	Р	Р	Р	Р	Р
I		Р	Р	Р	Р
А		Р			
М		Р	Р		
В		Р	Ρ		

Note: See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local *Microsemi Sales representative* for device availability.



- VCCA = Power supply in volts (V)
- F = Switching frequency in megahertz (MHz)

3.4.4 Equivalent Capacitance

Equivalent capacitance is calculated by measuring ICCactive at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

3.4.5 C_{EQ} Values for Microsemi MX FPGAs

Modules (C_{EQM})3.5

Input Buffers (C_{FOI})6.9

Output Buffers (C_{EQO})18.2

Routed Array Clock Buffer Loads (C_{EQCR})1.4

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. The equation below shows a piece-wise linear summation over all components.

 $\begin{aligned} \text{Power} &= \text{VCCA}^2 * [(\text{m} \times \text{C}_{\text{EQM}} * f_{\text{m}})_{\text{modules}} + (\text{n} * \text{C}_{\text{EQI}} * f_{\text{n}})_{\text{inputs}} + \overline{(\text{p} * (\text{C}_{\text{EQO}} + \text{C}_{\text{L}}) * f_{\text{p}})_{\text{outputs}}} + \\ 0.5 * (q_1 * \text{C}_{\text{EQCR}} * f_{q1})_{\text{routed}_\text{Clk1}} + (r_1 * f_{q1})_{\text{routed}_\text{Clk1}} + \\ 0.5 * (q_2 * \text{C}_{\text{EQCR}} * f_{q2})_{\text{routed}_\text{Clk2}} + (r_2 * f_{q2})_{\text{routed}_\text{Clk2}} (2)] \end{aligned}$

where:

m = Number of logic modules switching at frequency f_m

n = Number of input buffers switching at frequency f_n

p = Number of output buffers switching at frequency fp

 q_1 = Number of clock loads on the first routed array clock

q₂ = Number of clock loads on the second routed array clock

 r_1 = Fixed capacitance due to first routed array clock

r₂ = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

 C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output load capacitance in pF

f_m = Average logic module switching rate in MHz

 f_n = Average input buffer switching rate in MHz

 f_p = Average output buffer switching rate in MHz

 f_{q1} = Average first routed array clock rate in MHz

EQ 3



Figure 13 • Silicon Explorer II Setup with 42MX



Table 8 • Device Configuration Options for Probe Capability

Security Fuse(s) Programmed	Mode	PRA, PRB ¹	SDI, SDO, DCLK ¹
No	LOW	User I/Os ²	User I/Os ²
No	HIGH	Probe Circuit Outputs	Probe Circuit Inputs
Yes	_	Probe Circuit Secured	Probe Circuit Secured

1. Avoid using SDI, SDO, DCLK, PRA and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.

2. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. See the Pin Descriptions, page 83 for information on unused I/O pins

3.4.7 Design Consideration

It is recommended to use a series 70Ω termination resistor on every probe connector (SDI, SDO, MODE, DCLK, PRA and PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

3.4.8 IEEE Standard 1149.1 Boundary Scan Test (BST) Circuitry

42MX24 and 42MX36 devices are compatible with IEEE Standard 1149.1 (informally known as Joint Testing Action Group Standard or JTAG), which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic MX boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers and instruction register (Figure 14, page 18). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and some optional instructions. Table 9, page 18 describes the ports that control JTAG testing, while Table 10, page 18 describes the test instructions supported by these MX devices.

Each test section is accessed through the TAP, which has four associated pins: TCK (test clock input), TDI and TDO (test data input and output), and TMS (test mode selector).

The TAP controller is a four-bit state machine. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles.

42MX24 and 42MX36 devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.



3.4.9 JTAG Mode Activation

The JTAG test logic circuit is activated in the Designer software by selecting **Tools > Device Selection**. This brings up the Device Selection dialog box as shown in the following figure. The JTAG test logic circuit can be enabled by clicking the "Reserve JTAG Pins" check box. The following table explains the pins' behavior in either mode.

Figure 15 • Device Selection Wizard

Re	iserve <u>P</u> i	ins ———		
•	Reserve	<u>J</u> TAG		
	Reserve	e J <u>⊤</u> AG tes	streset	
Г	Reserve	e probe		

Table 11 • Boundary Scan Pin Configuration and Functionality

Reserve JTAG	Checked	Unchecked
ТСК	BST input; must be terminated to logical HIGH or LOW to avoid floating	User I/O
TDI, TMS	BST input; may float or be tied to HIGH	User I/O
TDO	BST output; may float or be connected to TDI of another device	User I/O

3.4.10 TRST Pin and TAP Controller Reset

An active reset (TRST) pin is not supported; however, MX devices contain power-on circuitry that resets the boundary scan circuitry upon power-up. Also, the TMS pin is equipped with an internal pull-up resistor. This allows the TAP controller to remain in or return to the Test-Logic-Reset state when there is no input or when a logical 1 is on the TMS pin. To reset the controller, TMS must be HIGH for at least five TCK cycles.

3.4.11 Boundary Scan Description Language (BSDL) File

Conforming to the IEEE Standard 1149.1 requires that the operation of the various JTAG components be documented. The BSDL file provides the standard format to describe the JTAG components that can be used by automatic test equipment software. The file includes the instructions that are supported, instruction bit pattern, and the boundary-scan chain order. For an in-depth discussion on BSDL files, see the *BSDL Files Format Description* application note.

BSDL files are grouped into two categories - generic and device-specific. The generic files assign all user I/Os as inouts. Device-specific files assign user I/Os as inputs, outputs or inouts.

Generic files for MX devices are available on the Microsemi SoC Product Group's website:

http://www.microsemi.com/soc/techdocs/models/bsdl.html.

3.5 Development Tool Support

The MX family of FPGAs is fully supported by Libero[®] Integrated Design Environment (IDE). Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes SynplifyPro from Synopsys, ModelSim[®] HDL Simulator from Mentor Graphics[®] and Viewdraw.

Libero IDE includes place-and-route and provides a comprehensive suite of backend support tools for FPGA development, including timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor.



Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi's integrated verification and logic analysis tool. Another tool included in the Libero software is the SmartGen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Microsemi's Libero software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synopsys, and Cadence design systems.

See the Libero IDE web content at www.microsemi.com/soc/products/software/libero/default.aspx for further information on licensing and current operating system support.

3.6 Related Documents

The following sections give the list of related documents which can be refered for this datasheet.

3.6.1 Application Notes

- AC278: BSDL Files Format Description
- AC225: Programming Antifuse Devices
- AC168: Implementation of Security in Microsemi Antifuse FPGAs

3.6.2 User Guides and Manuals

- Antifuse Macro Library Guide
- Silicon Sculptor Programmers User Guide

3.6.3 Miscellaneous

Libero IDE Flow Diagram

3.7 5.0 V Operating Conditions

The following tables show 5.0 V operating conditions.

Table 12 • Absolute Maximum Ratings for 40MX Devices*

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	-0.5 to +7.0	V
VI	Input Voltage	-0.5 to VCC+0.5	V
VO	Output Voltage	-0.5 to VCC+0.5	V
t _{STG}	Storage Temperature	-65 to +150	°C

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 13 • Absolute Maximum Ratings for 42MX Devices*

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	-0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	-0.5 to +7.0	V
VI	Input Voltage	-0.5 to VCCI+0.5	V
VO	Output Voltage	-0.5 to VCCI+0.5	V
t _{STG}	Storage Temperature	-65 to +150	°C



3.3 V LVTTL Electrical Specifications 3.8.1

Table 19 • 3.3V LVTTL Electrical Specifications

		Comn	nercial	Com	nercial -F	Indus	trial	Milita	ry	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
VOH ¹	IOH = -4 mA	2.15		2.15		2.4		2.4		V
VOL ¹	IOL = 6 mA		0.4		0.4		0.48		0.48	V
VIL		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX)		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL			-10		-10		-10		-10	μΑ
IIH			-10		-10		-10		-10	μΑ
Input Transition Time, ${\rm T_R}$ and ${\rm T_F}$			500		500		500		500	ns
C _{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC ²	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		15		25		25		25	mA
Low-Power Mode Standby Current	42MX devices only		0.5		ICC - 5.0		ICC - 5.0		ICC - 5.0	mA
IIO, I/O source	Can be derive	ed from	the IBIS mo	<i>del</i> (htt	p://www.micr	osemi.	com/soc/tech	ndocs/n	nodels/ibis.ht	ml)

sink current

Only one output tested at a time. VCC/VCCI = min. 1.

All outputs unloaded. All inputs = VCC/VCCI or GND. 2.

Mixed 5.0 V / 3.3 V Operating Conditions (for 42MX 3.9 **Devices Only)**

Table 20 • Absolute Maximum Ratings*

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	–0.5 to +7.0	V
VI	Input Voltage	-0.5 to VCCA +0.5	V
VO	Output Voltage	-0.5 to VCCI + 0.5	V
t _{STG}	Storage Temperature	-65 to +150	°C

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device



reliability. Devices should not be operated outside the recommended operating conditions.

 Table 21 •
 Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	-40 to +85	-55 to +125	°C
VCCA	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI	3.14 to 3.47	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.



A sample calculation of the absolute maximum power dissipation allowed for a TQ176 package at commercial temperature and still air is given in the following equation

MaximumPowerAllowed =
$$\frac{\text{Max} \cdot \text{junction temp} \cdot (^{\circ}\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (^{\circ}\text{C})}{\theta_{ja}(^{\circ}(\text{C/W}))} = \frac{150^{\circ}\text{C} - 70^{\circ}\text{C}}{(28^{\circ}\text{C})/\text{W}} = 2.86\text{W}$$

EQ 5

The maximum power dissipation for military-grade devices is a function of θ_{jc} . A sample calculation of the absolute maximum power dissipation allowed for CQFP 208-pin package at military temperature and still air is given in the following equation

MaximumPowerAllowed =
$$\frac{\text{Max · junction temp · (°C) - Max · ambient temp · (°C)}}{\theta_{jc}(°(C/W))} = \frac{150°C - 125°C}{(6.3°C)/W} = 3.97W$$

EQ 6

Table 27 • Package Thermal Characteristics

			θ_{ja}			
Plastic Packages	Pin Count	θ_{jc}	Still Air	1.0 m/s 200 ft/min.	2.5 m/s 500 ft/min.	Units
Plastic Quad Flat Pack	100	12.0	27.8	23.4	21.2	°C/W
Plastic Quad Flat Pack	144	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	160	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	208	8.0	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack	240	8.5	25.6	22.3	20.8	°C/W
Plastic Leaded Chip Carrier	44	16.0	20.0	24.5	22.0	°C/W
Plastic Leaded Chip Carrier	68	13.0	25.0	21.0	19.4	°C/W
Plastic Leaded Chip Carrier	84	12.0	22.5	18.9	17.6	°C/W
Thin Plastic Quad Flat Pack	176	11.0	24.7	19.9	18.0	°C/W
Very Thin Plastic Quad Flat Pack	80	12.0	38.2	31.9	29.4	°C/W
Very Thin Plastic Quad Flat Pack	100	10.0	35.3	29.4	27.1	°C/W
Plastic Ball Grid Array	272	3.0	18.3	14.9	13.9	°C/W
Ceramic Packages						
Ceramic Pin Grid Array	132	4.8	25.0	20.6	18.7	°C/W
Ceramic Quad Flat Pack	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack	256	2.0	20.0	16.5	15.0	°C/W









Note: Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions.

3.10.1 Parameter Measurement

The following figures show parameter measurement details.

Figure 21 • Output Buffer Delays







Table 38 •A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial
Conditions, VCCA = 4.75 V, T_J = 70°C)

		–3 Sp	beed	–2 S	peed	–1 Sp	beed	Std S	Speed	–F S	peed	
Parame	eter / Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
TTL Ou	tput Module Timing ⁵											
t _{DLH}	Data-to-Pad HIGH		2.5		2.7		3.1		3.6		5.1	ns
t _{DHL}	Data-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t _{ENZH}	Enable Pad Z to HIGH		2.6		2.9		3.3		3.9		5.5	ns
t _{ENZL}	Enable Pad Z to LOW		2.9		3.2		3.7		4.3		6.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		4.9		5.4		6.2		7.3		10.2	ns
t _{ENLZ}	Enable Pad LOW to Z		5.3		5.9		6.7		7.9		11.1	ns
t _{GLH}	G-to-Pad HIGH		2.6		2.9		3.3		3.8		5.3	ns
t _{GHL}	G-to-Pad LOW		2.6		2.9		3.3		3.8		5.3	ns
t _{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.2		5.8		6.6		7.7		10.8	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.4		8.2		9.3		10.9		15.3	ns
d _{TLH}	Capacity Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF
d _{THL}	Capacity Loading, HIGH to LOW		0.04		0.04		0.04		0.05		0.07	ns/pF



Table 44 •A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions,
VCCA = 4.75 V, T_J = 70°C)

		–3 S	peed	–2 S	beed	–1 Sp	beed	Std S	peed	–F Sp	eed	
Paramet	er / Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
TTL Out	put Module Timing ⁵ (Continued)											
t _{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t _{GLH}	G-to-Pad HIGH		2.9		3.3		3.7		4.4		6.1	ns
t _{GHL}	G-to-Pad LOW		2.9		3.3		3.7		4.4		6.1	ns
t _{LSU}	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF



4 Package Pin Assignments

The following figures and tables give the details of the package pin assignments.

Figure 38 • PL44



Table 47 • PL44

PL44		
Pin Number	A40MX02 Function	A40MX04 Function
1	I/O	I/O
2	I/O	I/O
3	VCC	VCC
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	GND	GND
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	VCC	VCC
15	I/O	I/O
16	VCC	VCC
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O



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PL68		
Pin Number	A40MX02 Function	A40MX04 Function
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	GND	GND
67	I/O	I/O
68	I/O	I/O

Figure 40 • PL84



Table 49 • PL84

A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
I/O	I/O	I/O	I/O
I/O	CLKB, I/O	CLKB, I/O	CLKB, I/O
I/O	I/O	I/O	I/O
VCC	PRB, I/O	PRB, I/O	PRB, I/O
I/O	I/O	I/O	WD, I/O
I/O	GND	GND	GND
I/O	I/O	I/O	I/O
I/O	I/O	I/O	WD, I/O
I/O	I/O	I/O	WD, I/O
	A40MX04 Function I/O I/O I/O VCC I/O 	A40MX04 Function A42MX09 Function I/O I/O I/O CLKB, I/O I/O I/O VCC PRB, I/O I/O I/O	A40MX04 Function A42MX09 Function A42MX16 Function I/O I/O I/O I/O CLKB, I/O CLKB, I/O I/O I/O I/O



Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
10	I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O
11	I/O	I/O	I/O	I/O
12	NC	MODE	MODE	MODE
13	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	I/O	I/O	I/O	I/O
18	GND	I/O	I/O	I/O
19	GND	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	VCCA	VCCI	VCCI
23	I/O	VCCI	VCCA	VCCA
24	I/O	I/O	I/O	I/O
25	VCC	I/O	I/O	I/O
26	VCC	I/O	I/O	I/O
27	I/O	I/O	I/O	I/O
28	I/O	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	I/O	I/O	I/O	I/O
31	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	VCC	I/O	I/O	I/O
34	I/O	I/O	I/O	TMS, I/O
35	I/O	I/O	I/O	TDI, I/O
36	I/O	I/O	I/O	WD, I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	WD, I/O
39	I/O	I/O	I/O	WD, I/O
40	GND	I/O	I/O	I/O
41	I/O	I/O	I/O	I/O
42	I/O	I/O	I/O	I/O
43	I/O	VCCA	VCCA	VCCA
44	I/O	I/O	I/O	WD, I/O
45	I/O	I/O	I/O	WD, I/O
46	VCC	I/O	I/O	WD, I/O



Table 49 • PL84



Table 50 • PQ 100

PQ100				
Pin Number	A40MX02 Function	A40MX04 Function	A42MX09 Function	A42MX16 Function
1	NC	NC	I/O	I/O
2	NC	NC	DCLK, I/O	DCLK, I/O
3	NC	NC	I/O	I/O
4	NC	NC	MODE	MODE
5	NC	NC	I/O	I/O
6	PRB, I/O	PRB, I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	GND	GND
10	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O
13	GND	GND	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	VCCA	VCCA
17	I/O	I/O	VCCI	VCCA
18	I/O	I/O	I/O	I/O



Figure 44 • PQ208



Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
1	GND	GND	GND
2	NC	VCCA	VCCA
3	MODE	MODE	MODE
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	NC	I/O	I/O
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	NC	I/O	I/O
17	VCCA	VCCA	VCCA
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O



CQ208		
Pin Number	A42MX36 Function	
148	I/O	
149	I/O	
150	GND	
151	I/O	
152	I/O	
153	I/O	
154	I/O	
155	I/O	
156	I/O	
157	GND	
158	I/O	
159	SDI, I/O	
160	I/O	
161	WD, I/O	
162	WD, I/O	
163	I/O	
164	VCCI	
165	I/O	
166	I/O	
167	I/O	
168	WD, I/O	
169	WD, I/O	
170	I/O	
171	QCLKD, I/O	
172	I/O	
173	I/O	
174	I/O	
175	I/O	
176	WD, I/O	
177	WD, I/O	
178	PRA, I/O	
179	I/O	
180	CLKA, I/O	
181	I/O	
182	VCCI	
183	VCCA	_
184	GND	



<i>Table 59</i> • CQ256			
CQ256			
Pin Number	A42MX36 Function		
244	WD, I/O		
245	I/O		
246	I/O		
247	I/O		
248	VCCI		
249	I/O		
250	WD, I/O		
251	WD, I/O		
252	I/O		
253	SDI, I/O		
254	I/O		
255	GND		
256	NC		

Figure 51 • BG272

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
А	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6
в	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
С	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D	0	0	0	0	0	0	0	Ο	0	0	0	0	0	0	0	Ο	0	Ο	Ο	0
Е	0	0	0	0													0	Ο	Ο	0
F	0	0	0	0													0	0	0	0
G	0	0	0	0				2	72-	Pin		3G/	A				0	Ο	Ο	0
н	0	0	0	0					-	_		_					0	0	0	0
J	0	0	0	0					Ō	Ō	Ō	Q					0	0	Ο	$\circ $
к	0	Õ	Õ	Õ					Ō	Ō	Ō	Ō					Q	Q	Ō	0
L	0	Õ	Õ	Õ					Õ	Õ	Õ	Õ					Ō	Ō	Ō	0
М	0	Õ	Õ	Õ					0	0	0	0					Ō	Ō	Ō	0
N	0	Ō	Ō	Ō													Ō	Ō	Ō	0
Р	0	Õ	Õ	õ													õ	õ	õ	õl
R	Õ	Õ	Õ	Õ													Õ	õ	õ	οl
Т	Õ	Ő	Õ	Õ	~	~	~	~	~	~	~	~	~	~	~	~	õ	õ	õ	õl
U	Õ	Õ	Õ	Õ	Õ	Õ	Õ	Õ	Õ	Õ	Õ	Õ	Õ	Õ	Õ	Õ	Õ	Õ	Õ	õ
V	0	Ő	Ő	Ő	Ő	õ	õ	Ő	õ	õ	õ	õ	õ	õ	õ	Ő	Ő	Ő	Ő	SI
W	0	Ő	Ő	Ő	Ő	Ő	Š	Ő	Ő	Ő	Ő	Ő	Ő	Ő	Ő	0 0	Ő	Ő	Ő	2
Υ	$\sqrt{0}$	0	0	0	Ο	Ο	Ο	0	O	0	0	0	Ο	0	0	Ο	0	Ο	Ο	0

BG272							
Pin Number	A42MX36 Function						
A1	GND						
A2	GND						
A3	I/O						
A4	WD, I/O						
A5	I/O						