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### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### **Details**

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	125
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-1pqg160i">https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-1pqg160i</a>

# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- Table 15, page 21 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 22, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 23, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

## 1.2 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Added CQFP package information for A42MX16 device in Product Profile, page 1 and Ceramic Device Resources, page 4 (SAR 79522).
- Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in Temperature Grade Offerings, page 5 (SAR 79519)
- Changed Silicon Sculptor II to Silicon Sculptor in Programming, page 12 (SAR 38754)
- Added Figure 53, page 158 CQ172 package (SAR 79522).

## 1.3 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Added Figure 42, page 97 PQ144 Package for A42MX09 device (SAR 69776)
- Added Figure 52, page 153 PQ132 Package for A42MX09 device (SAR 69776)

## 1.4 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Added information on power-up behavior for A42MX24 and A42MX36 devices to the Power Supply, page 13 (SAR 42096)
- Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793)

## 1.5 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- The FuseLock logo and accompanying text was removed from the User Security, page 12. This marking is no longer used on Microsemi devices (PCN 0915)
- The Development Tool Support, page 19 was updated (SAR 38512)

## 1.6 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- Ordering Information, page 3 was updated to include lead-free package ordering codes (SAR 21968)
- The User Security, page 12 was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673)

### 3.4.9 JTAG Mode Activation

The JTAG test logic circuit is activated in the Designer software by selecting **Tools > Device Selection**. This brings up the Device Selection dialog box as shown in the following figure. The JTAG test logic circuit can be enabled by clicking the “Reserve JTAG Pins” check box. The following table explains the pins’ behavior in either mode.

**Figure 15 • Device Selection Wizard**

**Table 11 • Boundary Scan Pin Configuration and Functionality**

Reserve JTAG	Checked	Unchecked
TCK	BST input; must be terminated to logical HIGH or LOW to avoid floating	User I/O
TDI, TMS	BST input; may float or be tied to HIGH	User I/O
TDO	BST output; may float or be connected to TDI of another device	User I/O

### 3.4.10 TRST Pin and TAP Controller Reset

An active reset (TRST) pin is not supported; however, MX devices contain power-on circuitry that resets the boundary scan circuitry upon power-up. Also, the TMS pin is equipped with an internal pull-up resistor. This allows the TAP controller to remain in or return to the Test-Logic-Reset state when there is no input or when a logical 1 is on the TMS pin. To reset the controller, TMS must be HIGH for at least five TCK cycles.

### 3.4.11 Boundary Scan Description Language (BSDL) File

Conforming to the IEEE Standard 1149.1 requires that the operation of the various JTAG components be documented. The BSDL file provides the standard format to describe the JTAG components that can be used by automatic test equipment software. The file includes the instructions that are supported, instruction bit pattern, and the boundary-scan chain order. For an in-depth discussion on BSDL files, see the *BSDL Files Format Description* application note.

BSDL files are grouped into two categories - generic and device-specific. The generic files assign all user I/Os as inouts. Device-specific files assign user I/Os as inputs, outputs or inouts.

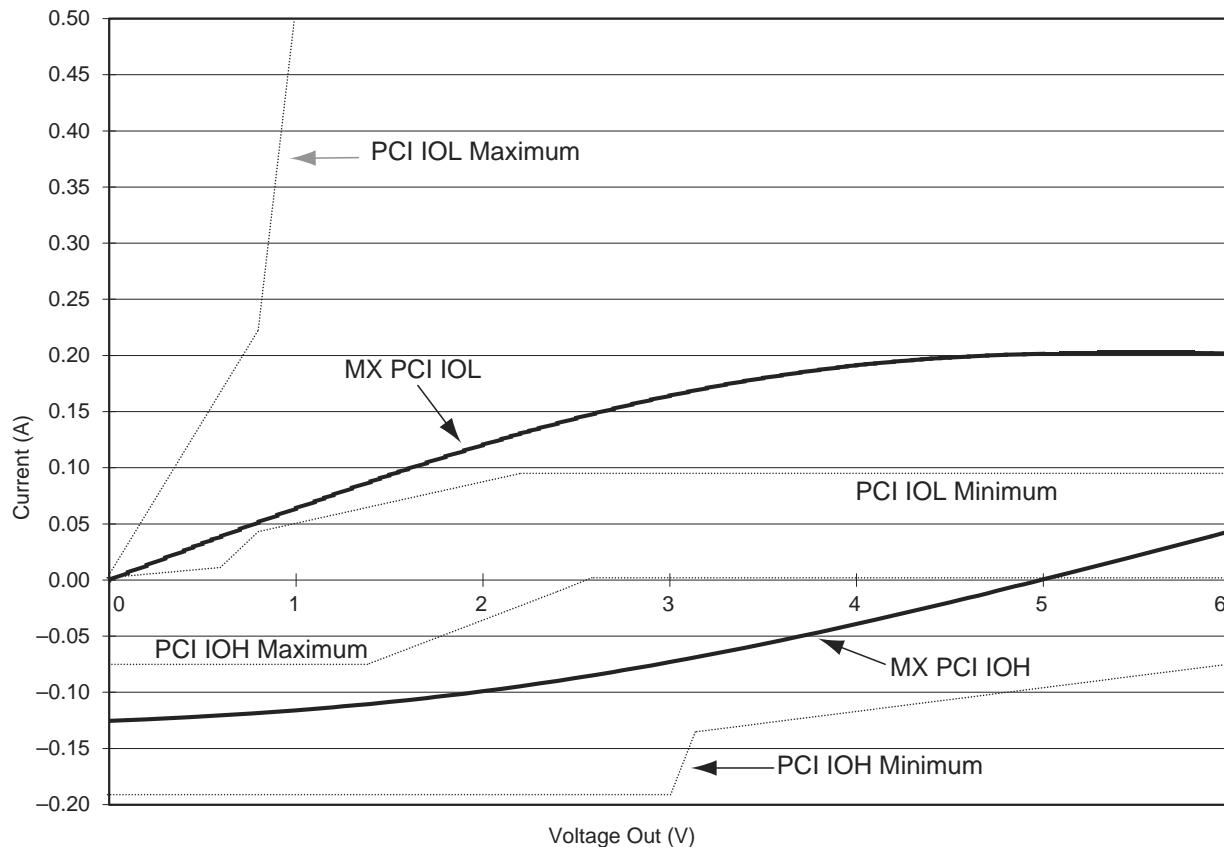
Generic files for MX devices are available on the Microsemi SoC Product Group's website:

<http://www.microsemi.com/soc/techdocs/models/bsdl.html>.

## 3.5 Development Tool Support

The MX family of FPGAs is fully supported by Libero® Integrated Design Environment (IDE). Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes SynplifyPro from Synopsys, ModelSim® HDL Simulator from Mentor Graphics® and Viewdraw.

Libero IDE includes place-and-route and provides a comprehensive suite of backend support tools for FPGA development, including timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor.

**Figure 16 • Typical Output Drive Characteristics (Based Upon Measured Data)**

### 3.9.4 Junction Temperature ( $T_J$ )

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a(1)$$

EQ 4

where:

- $T_a$  = Ambient Temperature
- $\Delta T$  = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$  (2)
- $P$  = Power
- $\theta_{ja}$  = Junction to ambient of package.  $\theta_{ja}$  numbers are located in Table 27, page 29.

### 3.9.5 Package Thermal Characteristics

The device junction-to-case thermal characteristic is  $\theta_{jc}$ , and the junction-to-ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates.

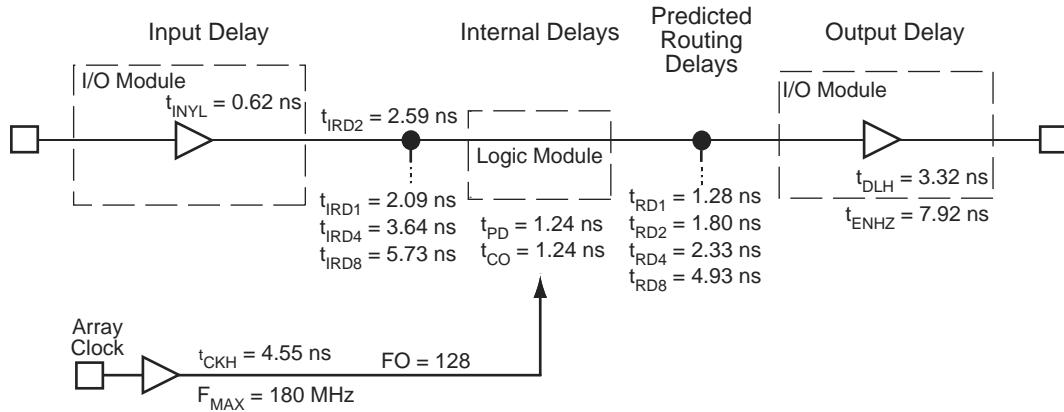
The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of  $\theta_{ja}$ .

### 3.10 Timing Models

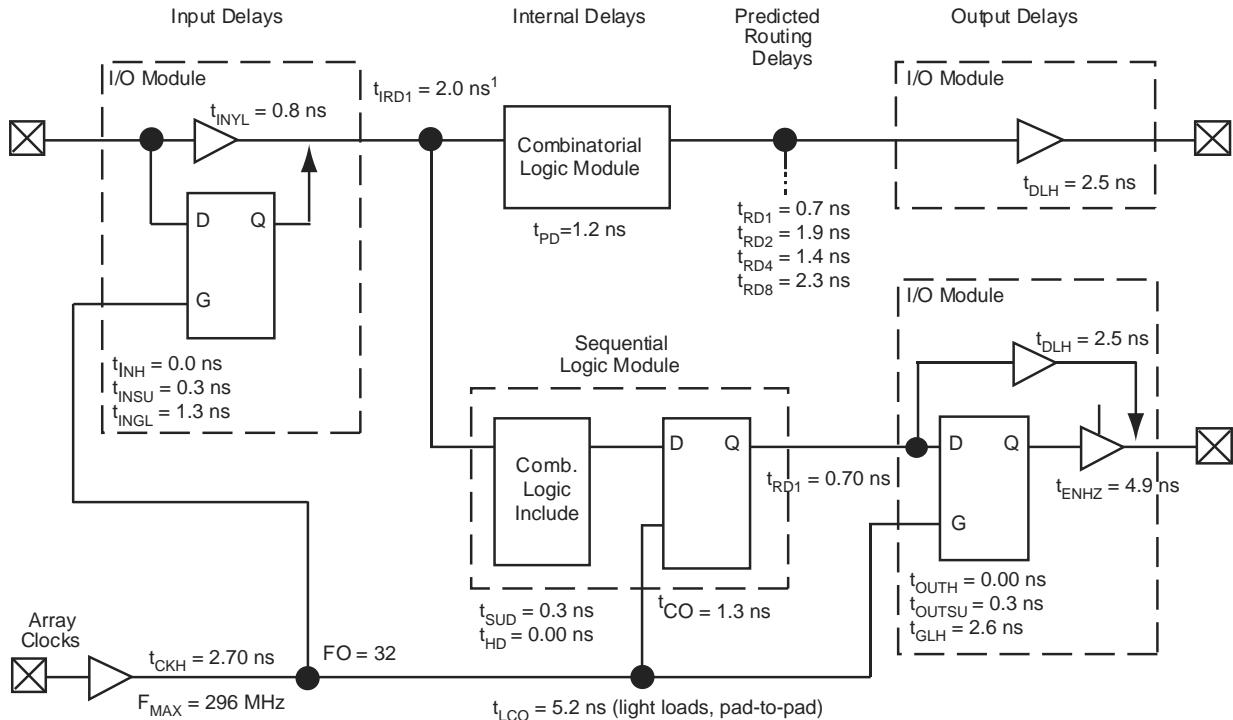
The following figures show various timing models.

**Figure 17 • 40MX Timing Model\***



**Note:** Values are shown for 40MX –3 speed devices at 5.0 V worst-case commercial conditions.

**Figure 18 • 42MX Timing Model**



**Note:** 1. Input module predicted routing delay

**Note:** 2. Values are shown for A42MX09 –3 at 5.0 V worst-case commercial conditions.

**Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 3.0 V, TJ = 70°C)**

<b>Parameter / Description</b>	<b>-3 Speed</b>		<b>-2 Speed</b>		<b>-1 Speed</b>		<b>Std Speed</b>		<b>-F Speed</b>		<b>Units</b>
	<b>Min.</b>	<b>Max.</b>	<b>Min.</b>	<b>Max.</b>	<b>Min.</b>	<b>Max.</b>	<b>Min.</b>	<b>Max.</b>	<b>Min.</b>	<b>Max.</b>	
t <sub>WCLKA</sub> Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t <sub>WASYN</sub> Flip-Flop (Latch) Asynchronous Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t <sub>A</sub> Flip-Flop Clock Input Period	6.8		7.8		8.9		10.4		14.6		ns
f <sub>MAX</sub> Flip-Flop (Latch) Clock Frequency (FO = 128)		109		101		92		80		48	MHz
<b>Input Module Propagation Delays</b>											
t <sub>I<sub>NYH</sub></sub> Pad-to-Y HIGH		1.0		1.1		1.3		1.5		2.1	ns
t <sub>I<sub>NYL</sub></sub> Pad-to-Y LOW		0.9		1.0		1.1		1.3		1.9	ns

**Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, TJ = 70°C)**

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>CMOS Output Module Timing<sup>5</sup></b>											
t <sub>DLH</sub>	Data-to-Pad HIGH		2.4		2.7		3.1		3.6		5.1 ns
t <sub>DHL</sub>	Data-to-Pad LOW		2.9		3.2		3.6		4.3		6.0 ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		2.7		2.9		3.3		3.9		5.5 ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		2.9		3.2		3.7		4.3		6.1 ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		4.9		5.4		6.2		7.3		10.2 ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		5.3		5.9		6.7		7.9		11.1 ns
t <sub>GLH</sub>	G-to-Pad HIGH		4.2		4.6		5.2		6.1		8.6 ns
t <sub>GHL</sub>	G-to-Pad LOW		4.2		4.6		5.2		6.1		8.6 ns
t <sub>LSU</sub>	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0	ns
t <sub>LH</sub>	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0	ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.2		5.8		6.6		7.7		10.8 ns
t <sub>ACO</sub>	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.4		8.2		9.3		10.9		15.3 ns
d <sub>TLH</sub>	Capacity Loading, LOW to HIGH	0.03		0.03		0.03		0.04		0.06	ns/pF
d <sub>THL</sub>	Capacity Loading, HIGH to LOW	0.04		0.04		0.04		0.05		0.07	ns/pF

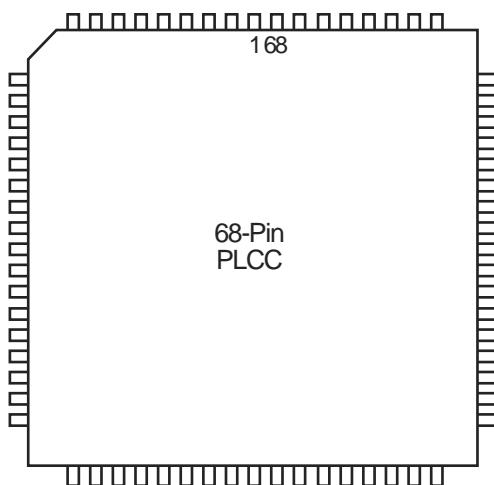
- For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
- Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
- Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
- Delays based on 35 pF loading

**Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, TJ = 70°C)**

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Logic Module Propagation Delays<sup>1</sup></b>											
t <sub>PD1</sub>	Single Module	1.6		1.8		2.1		2.5		3.5	ns
t <sub>CO</sub>	Sequential Clock-to-Q	1.8		2.0		2.3		2.7		3.8	ns
t <sub>GO</sub>	Latch G-to-Q	1.7		1.9		2.1		2.5		3.5	ns
t <sub>RS</sub>	Flip-Flop (Latch) Reset-to-Q	2.0		2.2		2.5		2.9		4.1	ns
<b>Logic Module Predicted Routing Delays<sup>2</sup></b>											
t <sub>RD1</sub>	FO = 1 Routing Delay	1.0		1.1		1.2		1.4		2.0	ns
t <sub>RD2</sub>	FO = 2 Routing Delay	1.3		1.4		1.6		1.9		2.7	ns
t <sub>RD3</sub>	FO = 3 Routing Delay	1.6		1.8		2.0		2.4		3.3	ns

**Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, TJ = 70°C)**

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Asynchronous SRAM Operations</b>											
t <sub>RPD</sub>	Asynchronous Access Time		8.1		9.0		10.2		12.0		16.8 ns
t <sub>RDADV</sub>	Read Address Valid		8.8		9.8		11.1		13.0		18.2 ns
t <sub>ADSU</sub>	Address/Data Set-Up Time		1.6		1.8		2.0		2.4		3.4 ns
t <sub>ADH</sub>	Address/Data Hold Time		0.0		0.0		0.0		0.0		0.0 ns
t <sub>RENSUA</sub>	Read Enable Set-Up to Address Valid		0.6		0.7		0.8		0.9		1.3 ns
t <sub>RENHA</sub>	Read Enable Hold		3.4		3.8		4.3		5.0		7.0 ns
t <sub>WENSU</sub>	Write Enable Set-Up		2.7		3.0		3.4		4.0		5.6 ns
t <sub>WENH</sub>	Write Enable Hold		0.0		0.0		0.0		0.0		0.0 ns
t <sub>DOH</sub>	Data Out Hold Time		1.2		1.3		1.5		1.8		2.5 ns
<b>Input Module Propagation Delays</b>											
t <sub>INPY</sub>	Input Data Pad-to-Y		1.0		1.1		1.3		1.5		2.1 ns
t <sub>INGO</sub>	Input Latch Gate-to-Output		1.4		1.6		1.8		2.1		2.9 ns
t <sub>INH</sub>	Input Latch Hold		0.0		0.0		0.0		0.0		0.0 ns
t <sub>INSU</sub>	Input Latch Set-Up		0.5		0.5		0.6		0.7		1.0 ns
t <sub>ILA</sub>	Latch Active Pulse Width		4.7		5.2		5.9		6.9		9.7 ns
<b>Input Module Predicted Routing Delays<sup>2</sup></b>											
t <sub>IRD1</sub>	FO = 1 Routing Delay		2.0		2.2		2.5		2.9		4.1 ns
t <sub>IRD2</sub>	FO = 2 Routing Delay		2.3		2.6		2.9		3.4		4.8 ns
t <sub>IRD3</sub>	FO = 3 Routing Delay		2.6		2.9		3.3		3.9		5.5 ns
t <sub>IRD4</sub>	FO = 4 Routing Delay		3.0		3.3		3.8		4.4		6.2 ns
t <sub>IRD8</sub>	FO = 8 Routing Delay		4.3		4.8		5.5		6.4		9.0 ns
<b>Global Clock Network</b>											
t <sub>CKH</sub>	Input LOW to HIGH	FO = 32	2.7		3.0		3.4		4.0		5.6 ns
		FO = 635	3.0		3.3		3.8		4.4		6.2 ns
t <sub>CKL</sub>	Input HIGH to LOW	FO = 32	3.8		4.2		4.8		5.6		7.8 ns
		FO = 635	4.9		5.4		6.1		7.2		10.1 ns
t <sub>PWH</sub>	Minimum Pulse Width HIGH	FO = 32	1.8		2.0		2.2		2.6		3.6 ns
		FO = 635	2.0		2.2		2.5		2.9		4.1 ns
t <sub>PWL</sub>	Minimum Pulse Width LOW	FO = 32	1.8		2.0		2.2		2.6		3.6 ns
		FO = 635	2.0		2.2		2.5		2.9		4.1 ns
t <sub>CKSW</sub>	Maximum Skew	FO = 32	0.8		0.8		0.9		1.0		1.4 ns
		FO = 635	0.8		0.8		0.9		1.0		1.4 ns

**Figure 39 • PL68****Table 48 • PL68**

<b>PL68</b>		
<b>Pin Number</b>	<b>A40MX02 Function</b>	<b>A40MX04 Function</b>
1	I/O	I/O
2	I/O	I/O
3	I/O	I/O
4	VCC	VCC
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	GND	GND
15	GND	GND
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	VCC	VCC
22	I/O	I/O
23	I/O	I/O

**Table 51 • PQ144**

<b>PQ144</b>	
<b>Pin Number</b>	<b>A42MX09 Function</b>
117	GNDI
118	NC
119	I/O
120	I/O
121	I/O
122	I/O
123	PROBA
124	I/O
125	CLKA
126	VCC
127	VCCI
128	NC
129	I/O
130	CLKB
131	I/O
132	PROBB
133	I/O
134	I/O
135	I/O
136	GND
137	GNDI
138	NC
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	DCLK

**Table 52 • PQ160**

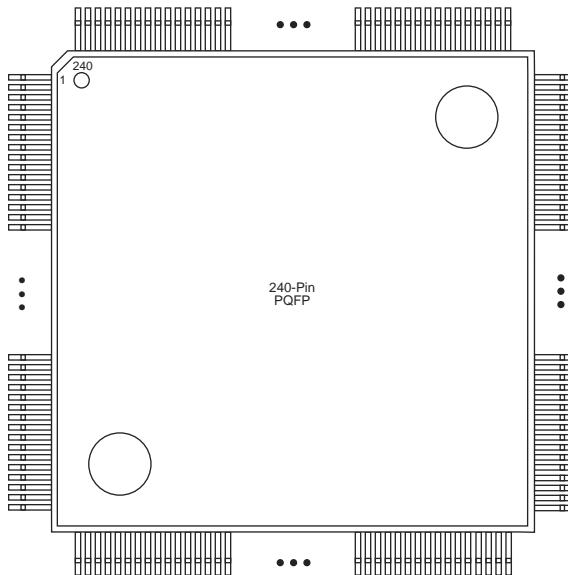
<b>PQ160</b>	<b>Pin Number</b>	<b>A42MX09 Function</b>	<b>A42MX16 Function</b>	<b>A42MX24 Function</b>
	132	I/O	I/O	I/O
	133	I/O	I/O	I/O
	134	I/O	I/O	I/O
	135	NC	VCCA	VCCA
	136	I/O	I/O	I/O
	137	I/O	I/O	I/O
	138	NC	VCCA	VCCA
	139	VCCI	VCCI	VCCI
	140	GND	GND	GND
	141	NC	I/O	I/O
	142	I/O	I/O	I/O
	143	I/O	I/O	I/O
	144	I/O	I/O	I/O
	145	GND	GND	GND
	146	NC	I/O	I/O
	147	I/O	I/O	I/O
	148	I/O	I/O	I/O
	149	I/O	I/O	I/O
	150	NC	VCCA	VCCA
	151	NC	I/O	I/O
	152	NC	I/O	I/O
	153	NC	I/O	I/O
	154	NC	I/O	I/O
	155	GND	GND	GND
	156	I/O	I/O	I/O
	157	I/O	I/O	I/O
	158	I/O	I/O	I/O
	159	MODE	MODE	MODE
	160	GND	GND	GND

**Table 53 • PQ208**

<b>PQ208</b>	<b>Pin Number</b>	<b>A42MX16 Function</b>	<b>A42MX24 Function</b>	<b>A42MX36 Function</b>
	21	I/O	I/O	I/O
	22	GND	GND	GND
	23	I/O	I/O	I/O
	24	I/O	I/O	I/O
	25	I/O	I/O	I/O
	26	I/O	I/O	I/O
	27	GND	GND	GND
	28	VCCI	VCCI	VCCI
	29	VCCA	VCCA	VCCA
	30	I/O	I/O	I/O
	31	I/O	I/O	I/O
	32	VCCA	VCCA	VCCA
	33	I/O	I/O	I/O
	34	I/O	I/O	I/O
	35	I/O	I/O	I/O
	36	I/O	I/O	I/O
	37	I/O	I/O	I/O
	38	I/O	I/O	I/O
	39	I/O	I/O	I/O
	40	I/O	I/O	I/O
	41	NC	I/O	I/O
	42	NC	I/O	I/O
	43	NC	I/O	I/O
	44	I/O	I/O	I/O
	45	I/O	I/O	I/O
	46	I/O	I/O	I/O
	47	I/O	I/O	I/O
	48	I/O	I/O	I/O
	49	I/O	I/O	I/O
	50	NC	I/O	I/O
	51	NC	I/O	I/O
	52	GND	GND	GND
	53	GND	GND	GND
	54	I/O	TMS, I/O	TMS, I/O
	55	I/O	TDI, I/O	TDI, I/O
	56	I/O	I/O	I/O
	57	I/O	WD, I/O	WD, I/O

**Table 53 • PQ208**

<b>PQ208</b>			
<b>Pin Number</b>	<b>A42MX16 Function</b>	<b>A42MX24 Function</b>	<b>A42MX36 Function</b>
206	I/O	I/O	I/O
207	DCLK, I/O	DCLK, I/O	DCLK, I/O
208	I/O	I/O	I/O

**Figure 45 • PQ240**

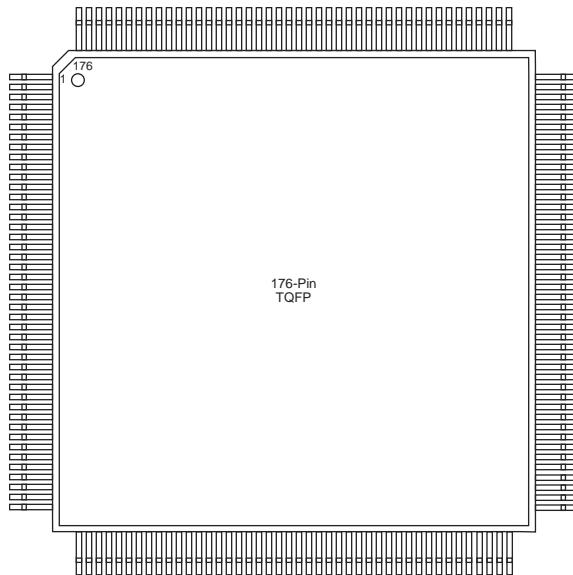
**Note:** This figure shows the 240-Pin PQFP Package top view.

**Table 54 • PQ240**

<b>PQ240</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
1	I/O
2	DCLK, I/O
3	I/O
4	I/O
5	I/O
6	WD, I/O
7	WD, I/O
8	VCCI
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O

**Table 56 • VQ100**

VQ100		
Pin Number	A42MX09 Function	A42MX16 Function
93	I/O	I/O
94	GND	GND
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	DCLK, I/O	DCLK, I/O

**Figure 48 • TQ176****Table 57 • TQ176**

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	GND	GND	GND
2	MODE	MODE	MODE
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	NC	NC	I/O
9	I/O	I/O	I/O

**Table 57 • TQ176**

<b>TQ176</b>	<b>Pin Number</b>	<b>A42MX09 Function</b>	<b>A42MX16 Function</b>	<b>A42MX24 Function</b>
	84	I/O	I/O	WD, I/O
	85	I/O	I/O	WD, I/O
	86	NC	I/O	I/O
	87	SDO, I/O	SDO, I/O	SDO, TDO, I/O
	88	I/O	I/O	I/O
	89	GND	GND	GND
	90	I/O	I/O	I/O
	91	I/O	I/O	I/O
	92	I/O	I/O	I/O
	93	I/O	I/O	I/O
	94	I/O	I/O	I/O
	95	I/O	I/O	I/O
	96	NC	I/O	I/O
	97	NC	I/O	I/O
	98	I/O	I/O	I/O
	99	I/O	I/O	I/O
	100	I/O	I/O	I/O
	101	NC	NC	I/O
	102	I/O	I/O	I/O
	103	NC	I/O	I/O
	104	I/O	I/O	I/O
	105	I/O	I/O	I/O
	106	GND	GND	GND
	107	NC	I/O	I/O
	108	NC	I/O	TCK, I/O
	109	LP	LP	LP
	110	VCCA	VCCA	VCCA
	111	GND	GND	GND
	112	VCCI	VCCI	VCCI
	113	VCCA	VCCA	VCCA
	114	NC	I/O	I/O
	115	NC	I/O	I/O
	116	NC	VCCA	VCCA
	117	I/O	I/O	I/O
	118	I/O	I/O	I/O
	119	I/O	I/O	I/O
	120	I/O	I/O	I/O

**Table 57 • TQ176**

<b>TQ176</b>	<b>Pin Number</b>	<b>A42MX09 Function</b>	<b>A42MX16 Function</b>	<b>A42MX24 Function</b>
	121	NC	NC	I/O
	122	I/O	I/O	I/O
	123	I/O	I/O	I/O
	124	NC	I/O	I/O
	125	NC	I/O	I/O
	126	NC	NC	I/O
	127	I/O	I/O	I/O
	128	I/O	I/O	I/O
	129	I/O	I/O	I/O
	130	I/O	I/O	I/O
	131	I/O	I/O	I/O
	132	I/O	I/O	I/O
	133	GND	GND	GND
	134	I/O	I/O	I/O
	135	SDI, I/O	SDI, I/O	SDI, I/O
	136	NC	I/O	I/O
	137	I/O	I/O	WD, I/O
	138	I/O	I/O	WD, I/O
	139	I/O	I/O	I/O
	140	NC	VCCI	VCCI
	141	I/O	I/O	I/O
	142	I/O	I/O	I/O
	143	NC	I/O	I/O
	144	NC	I/O	WD, I/O
	145	NC	NC	WD, I/O
	146	I/O	I/O	I/O
	147	NC	I/O	I/O
	148	I/O	I/O	I/O
	149	I/O	I/O	I/O
	150	I/O	I/O	WD, I/O
	151	NC	I/O	WD, I/O
	152	PRA, I/O	PRA, I/O	PRA, I/O
	153	I/O	I/O	I/O
	154	CLKA, I/O	CLKA, I/O	CLKA, I/O
	155	VCCA	VCCA	VCCA
	156	GND	GND	GND
	157	I/O	I/O	I/O

**Table 58 • CQ208**

<b>CQ208</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
1	GND
2	VCCA
3	MODE
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	VCCA
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	VCCI
29	VCCA
30	I/O
31	I/O
32	VCCA
33	I/O
34	I/O
35	I/O
36	I/O

**Table 58 • CQ208**

<b>CQ208</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
185	I/O
186	CLKB, I/O
187	I/O
188	PRB, I/O
189	I/O
190	WD, I/O
191	WD, I/O
192	I/O
193	I/O
194	WD, I/O
195	WD, I/O
196	QCLKC, I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	I/O
202	VCCI
203	WD, I/O
204	WD, I/O
205	I/O
206	I/O
207	DCLK, I/O
208	I/O

**Table 60 • BG272**

<b>BG272</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
T19	I/O
T20	I/O
U1	I/O
U2	I/O
U3	I/O
U4	I/O
U5	VCCI
U6	WD, I/O
U7	I/O
U8	I/O
U9	WD, I/O
U10	VCCA
U11	VCCI
U12	I/O
U13	I/O
U14	QCLKB, I/O
U15	I/O
U16	VCCI
U17	I/O
U18	GND
U19	I/O
U20	I/O
V1	I/O
V2	I/O
V3	GND
V4	GND
V5	I/O
V6	I/O
V7	I/O
V8	WD, I/O
V9	I/O
V10	I/O
V11	I/O
V12	I/O
V13	WD, I/O
V14	I/O
V15	WD, I/O

**Table 60 • BG272**

<b>BG272</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
V16	I/O
V17	I/O
V18	SDO, TDO, I/O
V19	I/O
V20	I/O
W1	GND
W2	GND
W3	I/O
W4	TMS, I/O
W5	I/O
W6	I/O
W7	I/O
W8	WD, I/O
W9	WD, I/O
W10	I/O
W11	I/O
W12	I/O
W13	WD, I/O
W14	I/O
W15	I/O
W16	WD, I/O
W17	I/O
W18	WD, I/O
W19	GND
W20	GND
Y1	GND
Y2	GND
Y3	I/O
Y4	TDI, I/O
Y5	WD, I/O
Y6	I/O
Y7	QCLKA, I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	I/O

**Table 61 • PG132**

<b>PG132</b>	
<b>Pin Number</b>	<b>A42MX09 Function</b>
F2	I/O
F1	I/O
G1	I/O
G4	VSV
H1	I/O
H2	I/O
H3	I/O
H4	I/O
J1	I/O
K1	I/O
L1	I/O
K2	I/O
M1	I/O
K3	I/O
L2	I/O
N1	I/O
L3	BININ
M2	BINOUT
N2	I/O
M3	I/O
L4	I/O
N3	I/O
M4	I/O
N4	I/O
M5	I/O
K6	I/O
N5	I/O
N6	I/O
L6	I/O
M6	I/O
M7	I/O
N7	I/O
N8	I/O
M8	I/O
L8	I/O
K8	I/O
N9	I/O