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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	72
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-2pl84i

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2 40MX and 42MX FPGA Families

2.1 Features

The following sections list out various features of the 40MX and 42MX FPGA family devices.

2.1.1 High Capacity

- Single-Chip ASIC Alternative
- 3,000 to 54,000 System Gates
- Up to 2.5 kbits Configurable Dual-Port SRAM
- Fast Wide-Decode Circuitry
- Up to 202 User-Programmable I/O Pins

2.1.2 High Performance

- 5.6 ns Clock-to-Out
- 250 MHz Performance
- 5 ns Dual-Port SRAM Access
- 100 MHz FIFOs
- 7.5 ns 35-Bit Address Decode

2.1.3 HiRel Features

- Commercial, Industrial, Automotive, and Military Temperature Plastic Packages
- Commercial, Military Temperature, and MIL-STD-883 Ceramic Packages
- QML Certification
- Ceramic Devices Available to DSCC SMD

2.1.4 Ease of Integration

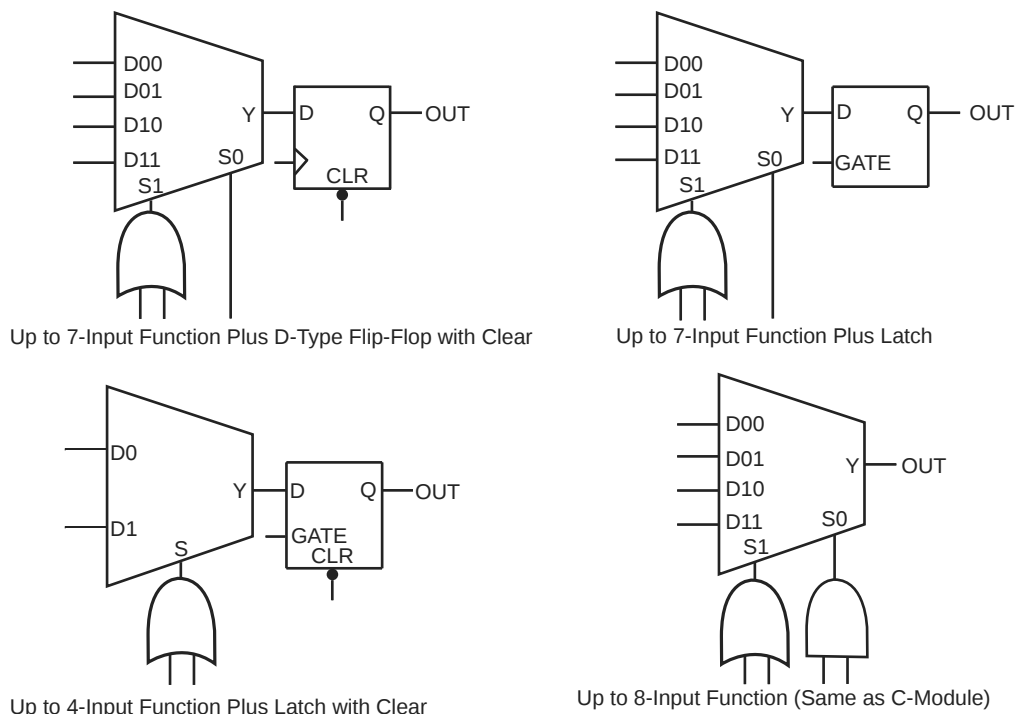
- Mixed-Voltage Operation (5.0 V or 3.3 V for core and I/Os), with PCI-Compliant I/Os
- Up to 100% Resource Utilization and 100% Pin Locking
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Low Power Consumption
- IEEE Standard 1149.1 (JTAG) Boundary Scan Testing

2.2 Product Profile

The following table gives the features of the products.

Table 1 • Product profile

Device	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
Capacity						
System Gates	3,000	6,000	14,000	24,000	36,000	54,000
SRAM Bits	–	–	–	–	–	2,560
Logic Modules						
Sequential	–	–	348	624	954	1,230
Combinatorial	295	547	336	608	912	1,184
Decode	–	–	–	–	24	24
Clock-to-Out	9.5 ns	9.5 ns	5.6 ns	6.1 ns	6.1 ns	6.3 ns
SRAM Modules (64x4 or 32x8)						
	–	–	–	–	–	10
Dedicated Flip-Flops	–	–	348	624	954	1,230

Figure 4 • 42MX S-Module Implementation

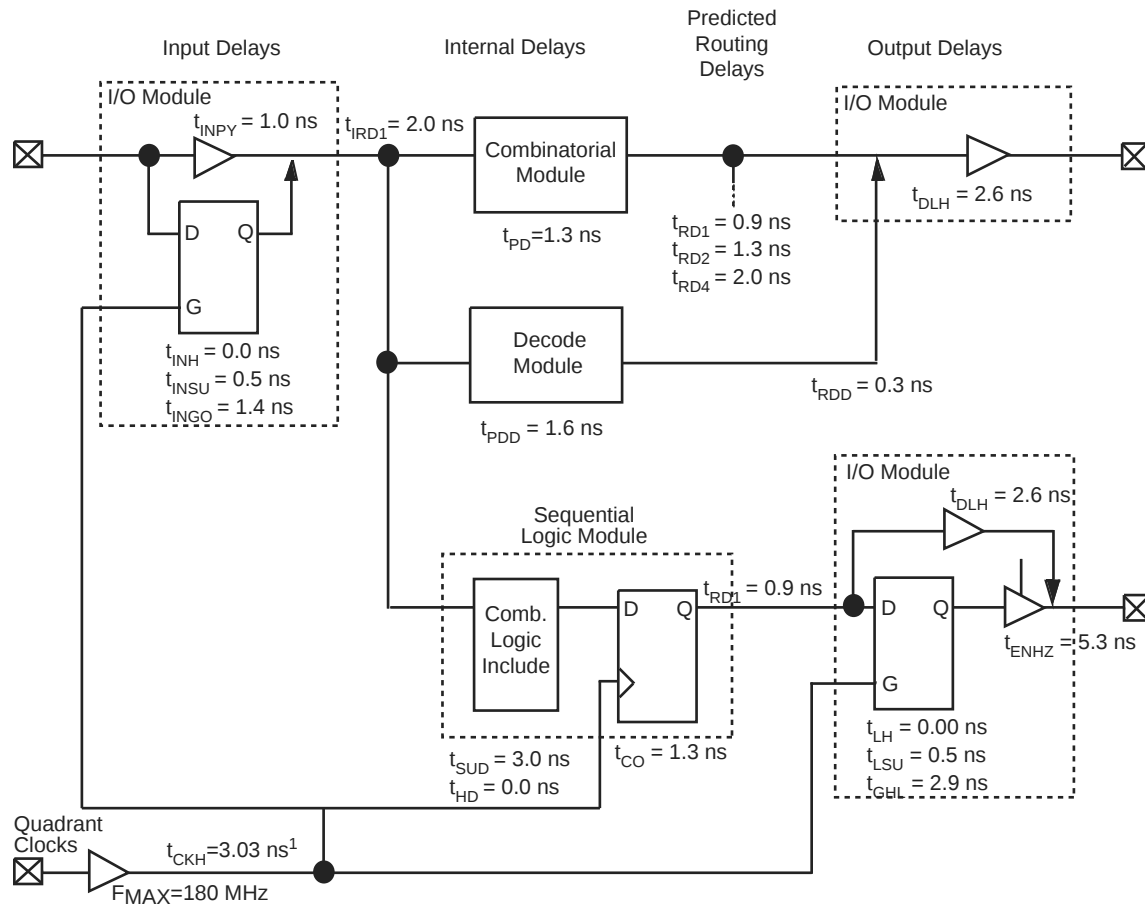
A42MX24 and A42MX36 devices contain D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry, providing a fast, wide-input AND function similar to that found in CPLD architectures (Figure 5, page 9). The D-module allows A42MX24 and A42MX36 devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin, and can also be fed back into the array to be incorporated into other logic.

3.2.2 Dual-Port SRAM Modules

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the A42MX36 dual-port SRAM block is shown in Figure 6, page 9.

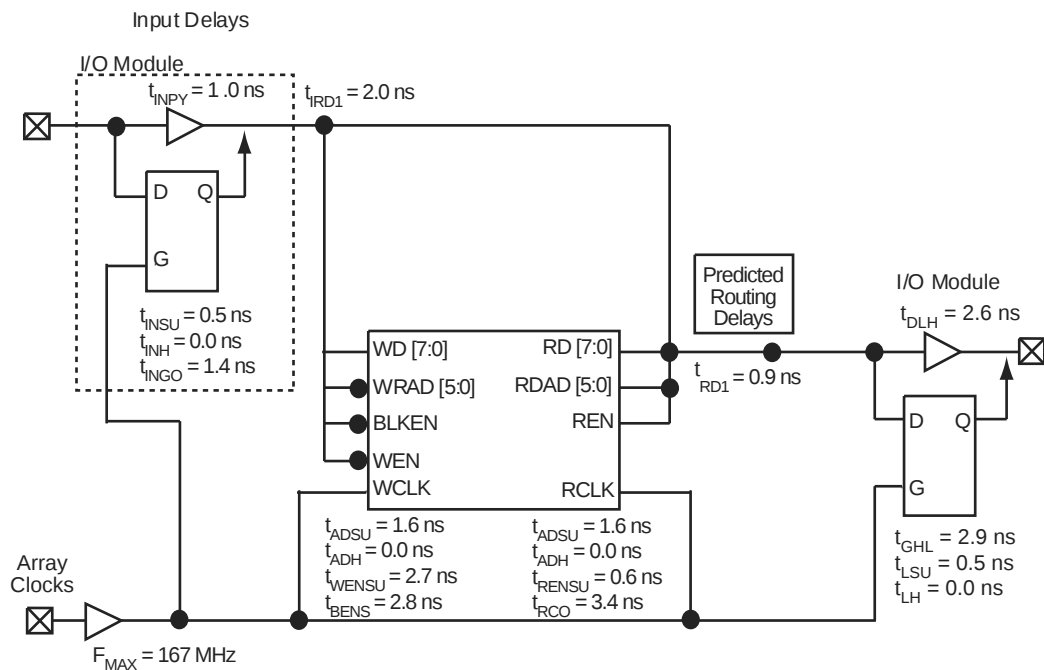
The A42MX36 SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]), which are connected to segmented vertical routing tracks.

The A42MX36 dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring FIFO and LIFO queues. The ACTgen Macro Builder within Microsemi's designer software provides capability to quickly design memory functions with the SRAM blocks. Unused SRAM blocks can be used to implement registers for other user logic within the design.

Figure 19 • 42MX Timing Model (Logic Functions Using Quadrant Clocks)

Note: 1. Load-dependent

Note: 2. Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions

Figure 20 • 42MX Timing Model (SRAM Functions)

Note: Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions.

3.10.1 Parameter Measurement

The following figures show parameter measurement details.

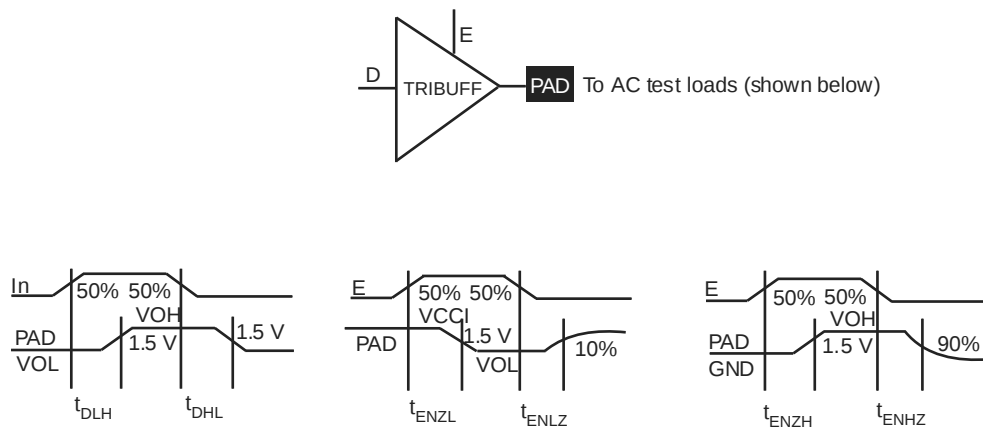
Figure 21 • Output Buffer Delays

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ¹												
t _{DLH}	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t _{DHL}	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t _{ENZH}	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t _{ENZL}	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t _{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t _{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d _{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer utility from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading

Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t _{PD2}	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t _{CO}	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t _{GO}	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays ¹												
t _{RD1}	FO = 1 Routing Delay		1.9		2.2		2.5		3.0		4.2	ns
t _{RD2}	FO = 2 Routing Delay		2.7		3.1		3.5		4.1		5.7	ns
t _{RD3}	FO = 3 Routing Delay		3.4		3.9		4.4		5.2		7.3	ns
t _{RD4}	FO = 4 Routing Delay		4.1		4.8		5.4		6.3		8.9	ns
t _{RD8}	FO = 8 Routing Delay		7.1		8.1		9.2		10.9		15.2	ns
Logic Module Sequential Timing ²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		4.3		5.0		5.6		6.6		9.2	ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		4.3		5.0		5.6		6.6		9.2	ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns

Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t _{INYH}	Pad-to-Y HIGH			1.0		1.2		1.3		1.6		2.2	ns
t _{INYL}	Pad-to-Y LOW			0.8		0.9		1.0		1.2		1.7	ns
t _{INGH}	G to Y HIGH			1.3		1.4		1.6		1.9		2.7	ns
t _{INGL}	G to Y LOW			1.3		1.4		1.6		1.9		2.7	ns
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay			2.0		2.2		2.5		3.0		4.2	ns
t _{IRD2}	FO = 2 Routing Delay			2.3		2.5		2.9		3.4		4.7	ns
t _{IRD3}	FO = 3 Routing Delay			2.5		2.8		3.2		3.7		5.2	ns
t _{IRD4}	FO = 4 Routing Delay			2.8		3.1		3.5		4.1		5.7	ns
t _{IRD8}	FO = 8 Routing Delay			3.7		4.1		4.7		5.5		7.7	ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32		2.4		2.7		3.0		3.6		5.0	ns
		FO = 256		2.7		3.0		3.4		4.0		5.5	ns
t _{CKL}	Input HIGH to LOW	FO = 32		3.5		3.9		4.4		5.2		7.3	ns
		FO = 256		3.9		4.3		4.9		5.7		8.0	ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t _{CKSW}	Maximum Skew	FO = 32		0.3		0.3		0.4		0.5		0.6	ns
		FO = 256		0.3		0.3		0.4		0.5		0.6	ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	2.3		2.6		3.0		3.5		4.9		ns
		FO = 256	2.2		2.4		3.3		3.9		5.5		ns
t _P	Minimum Period	FO = 32	3.4		3.7		4.0		4.7		7.8		ns
		FO = 256	3.7		4.1		4.5		5.2		8.6		ns
f _{MAX}	Maximum Frequency	FO = 32		296		269		247		215		129	MHz
		FO = 256		268		244		224		195		117	MHz

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Asynchronous SRAM Operations													
t _{RPD}	Asynchronous Access Time		8.1		9.0		10.2		12.0		16.8		ns
t _{RDADV}	Read Address Valid		8.8		9.8		11.1		13.0		18.2		ns
t _{ADSU}	Address/Data Set-Up Time		1.6		1.8		2.0		2.4		3.4		ns
t _{ADH}	Address/Data Hold Time		0.0		0.0		0.0		0.0		0.0		ns
t _{RENSUA}	Read Enable Set-Up to Address Valid		0.6		0.7		0.8		0.9		1.3		ns
t _{RENHA}	Read Enable Hold		3.4		3.8		4.3		5.0		7.0		ns
t _{WENSU}	Write Enable Set-Up		2.7		3.0		3.4		4.0		5.6		ns
t _{WENH}	Write Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{DOH}	Data Out Hold Time		1.2		1.3		1.5		1.8		2.5		ns
Input Module Propagation Delays													
t _{INPY}	Input Data Pad-to-Y		1.0		1.1		1.3		1.5		2.1		ns
t _{INGO}	Input Latch Gate-to-Output		1.4		1.6		1.8		2.1		2.9		ns
t _{INH}	Input Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Latch Set-Up		0.5		0.5		0.6		0.7		1.0		ns
t _{ILA}	Latch Active Pulse Width		4.7		5.2		5.9		6.9		9.7		ns
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay		2.0		2.2		2.5		2.9		4.1		ns
t _{IRD2}	FO = 2 Routing Delay		2.3		2.6		2.9		3.4		4.8		ns
t _{IRD3}	FO = 3 Routing Delay		2.6		2.9		3.3		3.9		5.5		ns
t _{IRD4}	FO = 4 Routing Delay		3.0		3.3		3.8		4.4		6.2		ns
t _{IRD8}	FO = 8 Routing Delay		4.3		4.8		5.5		6.4		9.0		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32	2.7	3.0	3.4	4.0	5.6	ns					
		FO = 635	3.0	3.3	3.8	4.4	6.2	ns					
t _{CKL}	Input HIGH to LOW	FO = 32	3.8	4.2	4.8	5.6	7.8	ns					
		FO = 635	4.9	5.4	6.1	7.2	10.1	ns					
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	1.8	2.0	2.2	2.6	3.6	ns					
		FO = 635	2.0	2.2	2.5	2.9	4.1	ns					
t _{PWL}	Minimum Pulse Width LOW	FO = 32	1.8	2.0	2.2	2.6	3.6	ns					
		FO = 635	2.0	2.2	2.5	2.9	4.1	ns					
t _{CKSW}	Maximum Skew	FO = 32	0.8	0.8	0.9	1.0	1.4	ns					
		FO = 635	0.8	0.8	0.9	1.0	1.4	ns					

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		3.5		3.9		4.5		5.2		7.3	ns
t _{DHL}	Data-to-Pad LOW		2.5		2.7		3.1		3.6		5.1	ns
t _{ENZH}	Enable Pad Z to HIGH		2.7		3.0		3.3		3.9		5.5	ns
t _{ENZL}	Enable Pad Z to LOW		2.9		3.3		3.7		4.3		6.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		5.3		5.8		6.6		7.8		10.9	ns
t _{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t _{GLH}	G-to-Pad HIGH		5.0		5.6		6.3		7.5		10.4	ns
t _{GHL}	G-to-Pad LOW		5.0		5.6		6.3		7.5		10.4	ns
t _{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions ¹												
t _{PD}	Internal Array Module Delay		1.9		2.1		2.3		2.7		3.8	ns
t _{PDD}	Internal Decode Module Delay		2.2		2.5		2.8		3.3		4.7	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.7	ns
t _{RD2}	FO = 2 Routing Delay		1.8		2.0		2.3		2.7		3.7	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.5		2.8		3.4		4.7	ns
t _{RD4}	FO = 4 Routing Delay		2.8		3.1		3.5		4.1		5.7	ns

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous SRAM Operations (continued)												
t _{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RENSU}	Read Enable Set-Up	0.9		1.0		1.1		1.3		1.8		ns
t _{RENH}	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t _{WENSU}	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t _{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{BENS}	Block Enable Set-Up	3.9		4.3		4.9		5.7		8.0		ns
t _{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations												
t _{RPD}	Asynchronous Access Time		11.3		12.6		14.3		16.8		23.5	ns
t _{RDADV}	Read Address Valid	12.3		13.7		15.5		18.2		25.5		ns
t _{ADSU}	Address/Data Set-Up Time	2.3		2.5		2.8		3.4		4.8		ns
t _{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RENSUA}	Read Enable Set-Up to Address Valid	0.9		1.0		1.1		1.3		1.8		ns
t _{RENHA}	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t _{WENSU}	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t _{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{DOH}	Data Out Hold Time		1.8		2.0		2.1		2.5		3.5	ns
Input Module Propagation Delays												
t _{INPY}	Input Data Pad-to-Y		1.4		1.6		1.8		2.1		3.0	ns
t _{INGO}	Input Latch Gate-to-Output		2.0		2.2		2.5		2.9		4.1	ns
t _{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t _{ILA}	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

Input, output, tristate or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/Os pins are configured by the Designer software as shown in Table 46, page 84.

Table 46 • Configuration of Unused I/Os

Device	Configuration
A40MX02, A40MX04	Pulled LOW
A42MX09, A42MX16	Pulled LOW
A42MX24, A42MX36	Tristated

In all cases, it is recommended to tie all unused MX I/O pins to LOW on the board. This applies to all dual-purpose pins when configured as I/Os as well.

LP, Low Power Mode

Controls the low power mode of all 42MX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation in 200 μ s after the LP pin is driven to a logic LOW.

MODE, Mode

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). The MODE pin is held HIGH to provide verification capability. The MODE pin should be terminated to GND through a 10k Ω resistor so that the MODE pin can be pulled HIGH when required.

NC, No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O

PRB, I/OProbe A/B

The Probe pin is used to output data from any user-defined design node within the device. Each diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. The Probe pin is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

QCLKA/B/C/D, I/O Quadrant Clock

Quadrant clock inputs for A42MX36 devices. When not used as a register control signal, these pins can function as user I/Os.

SDI, I/O Serial Data Input

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDO, I/O Serial Data Output

Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. SDO is available for 42MX devices only.

When Silicon Explorer II is being used, SDO will act as an output while the "checksum" command is run. It will return to user I/O when "checksum" is complete.

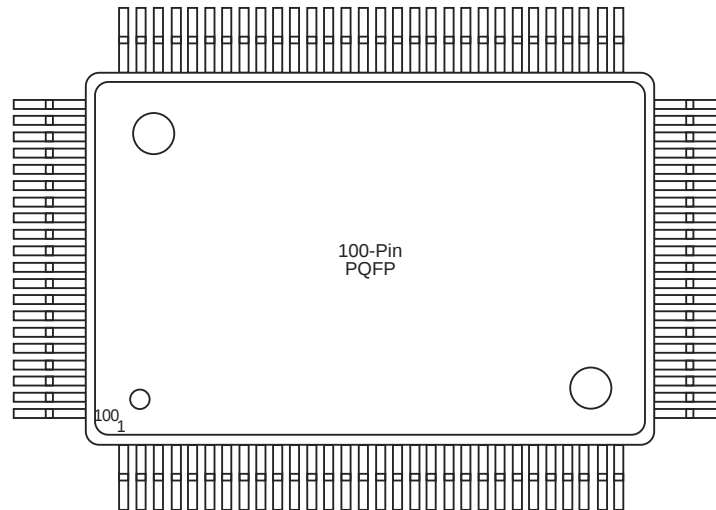
TCK, I/O Test Clock

Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
10	I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O
11	I/O	I/O	I/O	I/O
12	NC	MODE	MODE	MODE
13	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	I/O	I/O	I/O	I/O
18	GND	I/O	I/O	I/O
19	GND	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	VCCA	VCCI	VCCI
23	I/O	VCCI	VCCA	VCCA
24	I/O	I/O	I/O	I/O
25	VCC	I/O	I/O	I/O
26	VCC	I/O	I/O	I/O
27	I/O	I/O	I/O	I/O
28	I/O	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	I/O	I/O	I/O	I/O
31	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	VCC	I/O	I/O	I/O
34	I/O	I/O	I/O	TMS, I/O
35	I/O	I/O	I/O	TDI, I/O
36	I/O	I/O	I/O	WD, I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	WD, I/O
39	I/O	I/O	I/O	WD, I/O
40	GND	I/O	I/O	I/O
41	I/O	I/O	I/O	I/O
42	I/O	I/O	I/O	I/O
43	I/O	VCCA	VCCA	VCCA
44	I/O	I/O	I/O	WD, I/O
45	I/O	I/O	I/O	WD, I/O
46	VCC	I/O	I/O	WD, I/O

Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
84	I/O	VCCA	VCCA	VCCA

Figure 41 • PQ100**Table 50 • PQ 100**

PQ100				
Pin Number	A40MX02 Function	A40MX04 Function	A42MX09 Function	A42MX16 Function
1	NC	NC	I/O	I/O
2	NC	NC	DCLK, I/O	DCLK, I/O
3	NC	NC	I/O	I/O
4	NC	NC	MODE	MODE
5	NC	NC	I/O	I/O
6	PRB, I/O	PRB, I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	GND	GND
10	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O
13	GND	GND	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	VCCA	VCCA
17	I/O	I/O	VCCI	VCCA
18	I/O	I/O	I/O	I/O

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
95	NC	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	VCCI	VCCI	VCCI
99	I/O	I/O	I/O
100	I/O	WD, I/O	WD, I/O
101	I/O	WD, I/O	WD, I/O
102	I/O	I/O	I/O
103	SDO, I/O	SDO, TDO, I/O	SDO, TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	VCCA	VCCA
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	NC	I/O	I/O
113	NC	I/O	I/O
114	NC	I/O	I/O
115	NC	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	I/O	I/O	I/O
126	GND	GND	GND
127	I/O	I/O	I/O
128	I/O	TCK, I/O	TCK, I/O
129	LP	LP	LP
130	VCCA	VCCA	VCCA
131	GND	GND	GND

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
15	QCLKC, I/O
16	I/O
17	WD, I/O
18	WD, I/O
19	I/O
20	I/O
21	WD, I/O
22	WD, I/O
23	I/O
24	PRB, I/O
25	I/O
26	CLKB, I/O
27	I/O
28	GND
29	VCCA
30	VCCI
31	I/O
32	CLKA, I/O
33	I/O
34	PRA, I/O
35	I/O
36	I/O
37	WD, I/O
38	WD, I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	QCLKD, I/O
46	I/O
47	WD, I/O
48	WD, I/O
49	I/O
50	I/O
51	I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
126	WD, I/O
127	I/O
128	VCCI
129	I/O
130	I/O
131	I/O
132	WD, I/O
133	WD, I/O
134	I/O
135	QCLKB, I/O
136	I/O
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	WD, I/O
143	WD, I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	VCCI
151	VCCA
152	GND
153	I/O
154	I/O
155	I/O
156	I/O
157	I/O
158	I/O
159	WD, I/O
160	WD, I/O
161	I/O
162	I/O

Table 55 • VQ80

VQ80		
Pin Number	A40MX02 Function	A40MX04 Function
49	I/O	I/O
50	CLK, I/O	CLK, I/O
51	I/O	I/O
52	MODE	MODE
53	VCC	VCC
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	GND	GND
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	VCC	VCC
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O

Table 61 • PG132

PG132	
Pin Number	A42MX09 Function
G12	VSV
F13	I/O
F12	I/O
F11	I/O
F10	I/O
E13	I/O
D13	I/O
D12	I/O
C13	I/O
B13	I/O
D11	I/O
C12	I/O
A13	I/O
C11	I/O
B12	SDI
B11	I/O
C10	I/O
A12	I/O
A11	I/O
B10	I/O
D8	I/O
A10	I/O
C8	I/O
A9	I/O
B8	PRBA
A8	I/O
B7	CLKA
A7	I/O
B6	CLKB
A6	I/O
C6	PRBB
A5	I/O
D6	I/O
A4	I/O
B4	I/O
A3	I/O
C4	I/O