# Microchip Technology - A42MX16-2PLG84 Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 72 |
| Number of Gates | 24000 |
| Voltage - Supply | 3V ~ 3.6V, 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 84-LCC (J-Lead) |
| Supplier Device Package | 84-PLCC (29.31x29.31) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-2plg84 |

Power Matters.™

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Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

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- The Transient Current, page 13 is new (SAR 36930).
- Package names were revised according to standards established in *Package Mechanical Drawings* (SAR 34774)

## 1.7 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document

- In Table 20, page 23, the limits in VI were changed from -0.5 to VCCI + 0.5 to -0.5 to VCCA + 0.5

In Table 22, page 25, $V_{OH}$ was changed from 3.7 to 2.4 for the min in industrial and military. $V_{IH}$ had $V_{CCI}$ and that was changed to VCCA

## 1.8 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- The Ease of Integration, page 1 was updated
- The Temperature Grade Offerings, page 5 is new
- The Speed Grade Offerings, page 5 is new
- The General Description, page 6 was updated
- The MultiPlex I/O Modules, page 11 was updated
- The User Security, page 12 was updated
- Table 6, page 13 was updated
- The Power Dissipation, page 14 was updated.
- The Static Power Component, page 14 was updated
- The Equivalent Capacitance, page 15 was updated
- Figure 13, page 17 was updated
- Table 10, page 18 was updated.
- Figure 14, page 18 was updated.
- Table 11, page 19 was updated.

# 2 40MX and 42MX FPGA Families

## 2.1 Features

The following sections list out various features of the 40MX and 42MX FPGA family devices.

### 2.1.1 High Capacity

- Single-Chip ASIC Alternative
- 3,000 to 54,000 System Gates
- Up to 2.5 kbits Configurable Dual-Port SRAM
- Fast Wide-Decode Circuitry
- Up to 202 User-Programmable I/O Pins

### 2.1.2 High Performance

- 5.6 ns Clock-to-Out
- 250 MHz Performance
- 5 ns Dual-Port SRAM Access
- 100 MHz FIFOs
- 7.5 ns 35-Bit Address Decode

### 2.1.3 HiRel Features

- Commercial, Industrial, Automotive, and Military Temperature Plastic Packages
- Commercial, Military Temperature, and MIL-STD-883 Ceramic Packages
- QML Certification
- Ceramic Devices Available to DSCC SMD

### 2.1.4 Ease of Integration

- Mixed-Voltage Operation (5.0 V or 3.3 V for core and I/Os), with PCI-Compliant I/Os
- Up to 100% Resource Utilization and 100% Pin Locking
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Low Power Consumption
- IEEE Standard 1149.1 (JTAG) Boundary Scan Testing

## 2.2 Product Profile

The following table gives the features of the products.

***Table 1 •*** **Product profile**

| **Device** | **A40MX02** | **A40MX04** | **A42MX09** | **A42MX16** | **A42MX24** | **A42MX36** |
|---|---|---|---|---|---|---|
| **Capacity** | | | | | | |
| System Gates | 3,000 | 6,000 | 14,000 | 24,000 | 36,000 | 54,000 |
| SRAM Bits | – | – | – | – | – | 2,560 |
| **Logic Modules** | | | | | | |
| Sequential | – | – | 348 | 624 | 954 | 1,230 |
| Combinatorial | 295 | 547 | 336 | 608 | 912 | 1,184 |
| Decode | – | – | – | – | 24 | 24 |
| **Clock-to-Out** | 9.5 ns | 9.5 ns | 5.6 ns | 6.1 ns | 6.1 ns | 6.3 ns |
| **SRAM Modules (64x4 or 32x8)** | – | – | – | – | – | 10 |
| **Dedicated Flip-Flops** | – | – | 348 | 624 | 954 | 1,230 |

## 2.6 Temperature Grade Offerings

*Table 4 •* **Temperature Grade Offerings**

| Package | A40MX02 | A40MX04 | A42MX09 | A42MX16 | A42MX24 | A42MX36 |
|---|---|---|---|---|---|---|
| PLCC 44 | C, I, M | C, I, M | | | | |
| PLCC 68 | C, I, A, M | C, I, M | | | | |
| PLCC 84 | | C, I, A, M | C, I, A, M | C, I, M | C, I, M | |
| PQFP 100 | C, I, A, M | C, I, A, M | C, I, A, M | C, I, M | | |
| PQFP 144 | | | C | | | |
| PQFP 160 | | | C, I, A, M | C, I, M | C, I, A, M | |
| PQFP 208 | | | | C, I, A, M | C, I, A, M | C, I, A, M |
| PQFP 240 | | | | | | C, I, A, M |
| VQFP 80 | C, I, A, M | C, I, A, M | | | | |
| VQFP 100 | | | C, I, A, M | C, I, A, M | | |
| TQFP 176 | | | C, I, A, M | C, I, A, M | C, I, A, M | |
| PBGA 272 | | | | | | C, I, M |
| CQFP 172 | | | | C, M, B | | |
| CQFP 208 | | | | | | C, M, B |
| CQFP 256 | | | | | | C, M, B |
| CPGA 132 | | | C, M, B | | | |

**Note:** C = Commercial
I = Industrial
A = Automotive
M = Military
B = MIL-STD-883 Class B

## 2.7 Speed Grade Offerings

*Table 5 •* **Speed Grade Offerings**

| | – F | Std | –1 | –2 | –3 |
|---|---|---|---|---|---|
| C | P | P | P | P | P |
| I | | P | P | P | P |
| A | | P | | | |
| M | | P | P | | |
| B | | P | P | | |

**Note:** See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local *Microsemi Sales representative* for device availability.

Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi's integrated verification and logic analysis tool. Another tool included in the Libero software is the SmartGen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Microsemi's Libero software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synopsys, and Cadence design systems.

See the Libero IDE web content at www.microsemi.com/soc/products/software/libero/default.aspx for further information on licensing and current operating system support.

## 3.6 Related Documents

The following sections give the list of related documents which can be refered for this datasheet.

### 3.6.1 Application Notes

- *AC278: BSDL Files Format Description*
- *AC225: Programming Antifuse Devices*
- *AC168: Implementation of Security in Microsemi Antifuse FPGAs*

### 3.6.2 User Guides and Manuals

- *Antifuse Macro Library Guide*
- *Silicon Sculptor Programmers User Guide*

### 3.6.3 Miscellaneous

*Libero IDE Flow Diagram*

## 3.7 5.0 V Operating Conditions

The following tables show 5.0 V operating conditions.

***Table 12 •*** **Absolute Maximum Ratings for 40MX Devices***

| **Symbol** | **Parameter** | **Limits** | **Units** |
|---|---|---|---|
| VCC | DC Supply Voltage | –0.5 to +7.0 | V |
| VI | Input Voltage | –0.5 to VCC+0.5 | V |
| VO | Output Voltage | –0.5 to VCC+0.5 | V |
| $t_{STG}$ | Storage Temperature | –65 to +150 | °C |

**Note:** *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

***Table 13 •*** **Absolute Maximum Ratings for 42MX Devices***

| **Symbol** | **Parameter** | **Limits** | **Units** |
|---|---|---|---|
| VCCI | DC Supply Voltage for I/Os | –0.5 to +7.0 | V |
| VCCA | DC Supply Voltage for Array | –0.5 to +7.0 | V |
| VI | Input Voltage | –0.5 to VCCI+0.5 | V |
| VO | Output Voltage | –0.5 to VCCI+0.5 | V |
| $t_{STG}$ | Storage Temperature | –65 to +150 | °C |

3. All outputs unloaded. All inputs = VCC/VCCI or GND

## 3.8 3.3 V Operating Conditions

The following table shows 3.3 V operating conditions.

***Table 16 •*** **Absolute Maximum Ratings for 40MX Devices***

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCC | DC Supply Voltage | –0.5 to +7.0 | V |
| VI | Input Voltage | –0.5 to VCC + 0.5 | V |
| VO | Output Voltage | –0.5 to VCC + 0.5 | V |
| $t_{STG}$ | Storage Temperature | –65 to + 150 | °C |

**Note:** *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

***Table 17 •*** **Absolute Maximum Ratings for 42MX Devices***

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCCI | DC Supply Voltage for I/Os | –0.5 to +7.0 | V |
| VCCA | DC Supply Voltage for Array | –0.5 to +7.0 | V |
| VI | Input Voltage | –0.5 to VCCI+0.5 | V |
| VO | Output Voltage | –0.5 to VCCI+0.5 | V |
| $t_{STG}$ | Storage Temperature | –65 to +150 | °C |

**Note:** *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

***Table 18 •*** **Recommended Operating Conditions**

| Parameter | Commercial | Industrial | Military | Units |
|---|---|---|---|---|
| Temperature Range* | 0 to +70 | –40 to +85 | –55 to +125 | °C |
| VCC (40MX) | 3.0 to 3.6 | 3.0 to 3.6 | 3.0 to 3.6 | V |
| VCCA (42MX) | 3.0 to 3.6 | 3.0 to 3.6 | 3.0 to 3.6 | V |
| VCCI (42MX) | 3.0 to 3.6 | 3.0 to 3.6 | 3.0 to 3.6 | V |

**Note:** *Ambient temperature ($T_A$) is used for commercial and industrial grades; case temperature ($T_C$) is used for military grades.

All the following tables show various specifications and operating conditions of 40MX and 42MX FPGAs.

**Figure 22 •** **AC Test Loads**

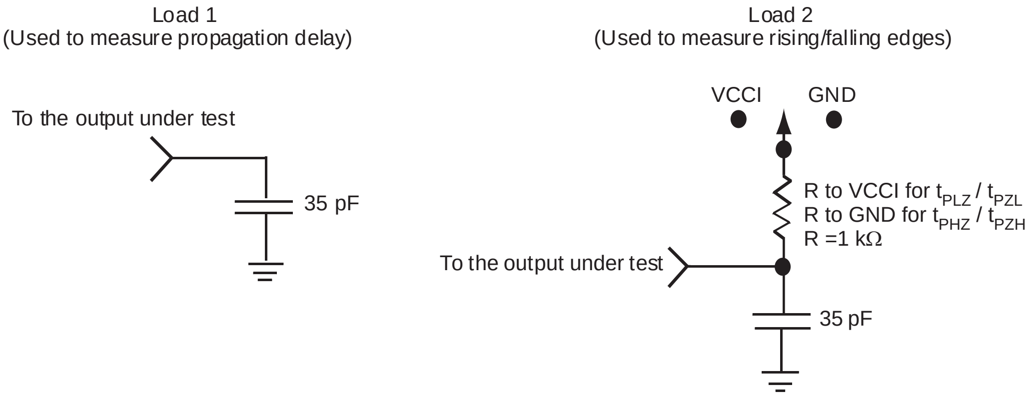


**Figure 23 •** **Input Buffer Delays**

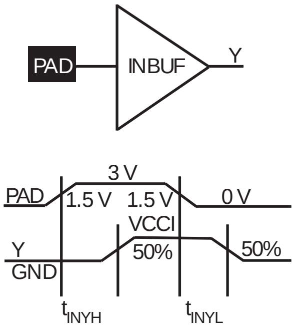


**Figure 24 •** **Module Delays**

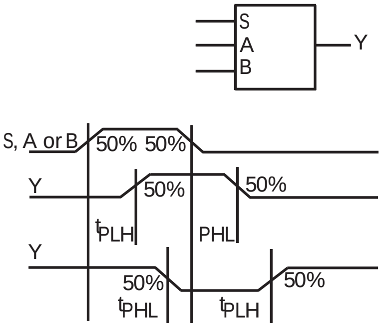
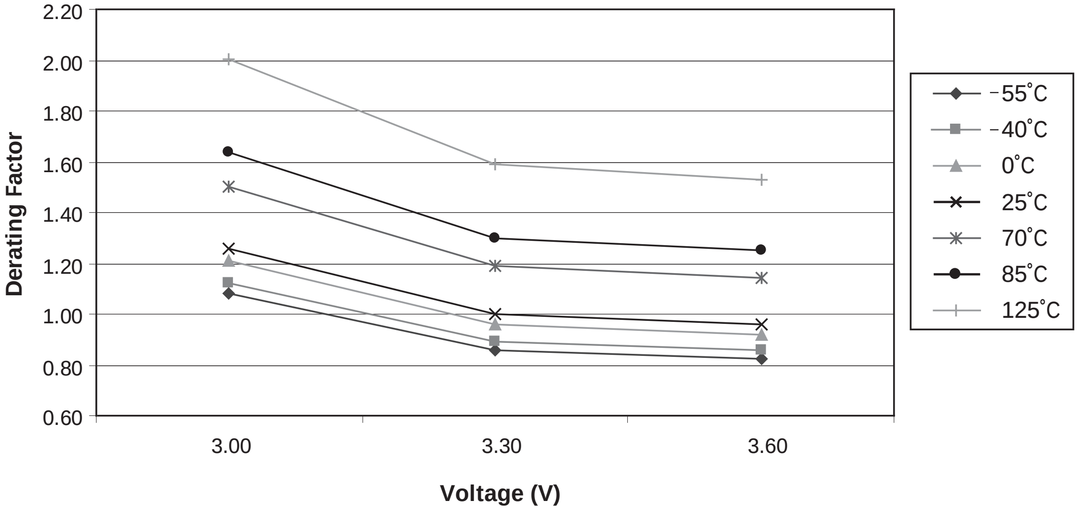


**Table 31 •** **40MX Temperature and Voltage Derating Factors (Normalized to TJ = 25°C, VCC = 3.3 V)**

| | Temperature | | | | | | |
|---|---|---|---|---|---|---|---|
| **40MX Voltage** | **–55°C** | **–40°C** | **0°C** | **25°C** | **70°C** | **85°C** | **125°C** |
| 3.60 | 0.83 | 0.85 | 0.92 | 0.96 | 1.14 | 1.25 | 1.53 |

**Figure 37 •** **40MX Junction Temperature and Voltage Derating Curves (Normalized to TJ = 25°C, VCC = 3.3 V)**



**Note:** This derating factor applies to all routing and propagation delays

## 3.11.5 PCI System Timing Specification

The following tables list the critical PCI timing parameters and the corresponding timing parameters for the MX PCI-compliant devices.

## 3.11.6 PCI Models

Microsemi provides synthesizable VHDL and Verilog-HDL models for a PCI Target interface, a PCI Target and Target+DMA Master interface. Contact the Microsemi sales representative for more details.

**Table 32 •** **Clock Specification for 33 MHz PCI**

| | | PCI | | A42MX24 | | A42MX36 | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $t_{CYC}$ | CLK Cycle Time | 30 | – | 4.0 | – | 4.0 | – | ns |
| $t_{HIGH}$ | CLK High Time | 11 | – | 1.9 | – | 1.9 | – | ns |
| $t_{LOW}$ | CLK Low Time | 11 | – | 1.9 | – | 1.9 | – | ns |

**Table 33 •** **Timing Parameters for 33 MHz PCI**

| | | PCI | | A42MX24 | | A42MX36 | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $t_{VAL}$ | CLK to Signal Valid—Bused Signals | 2 | 11 | 2.0 | 9.0 | 2.0 | 9.0 | ns |
| $t_{VAL(PTP)}$ | CLK to Signal Valid—Point-to-Point | 2 [2] | 12 | 2.0 | 9.0 | 2.0 | 9.0 | ns |
| $t_{ON}$ | Float to Active | 2 | – | 2.0 | 4.0 | 2.0 | 4.0 | ns |
| $t_{OFF}$ | Active to Float | – | 28 | – | 8.3[1] | – | 8.3[1] | ns |
| $t_{SU}$ | Input Set-Up Time to CLK—Bused Signals | 7 | – | 1.5 | – | 1.5 | – | ns |

*Table 40 •* **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| **CMOS Output Module Timing**[5] | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 3.2 | | 3.6 | | 4.0 | | 4.7 | | 6.6 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 2.5 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 2.7 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 3.0 | | 3.3 | | 3.8 | | 4.4 | | 6.2 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 5.4 | | 6.0 | | 6.8 | | 8.0 | | 11.2 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.0 | | 5.6 | | 6.3 | | 7.4 | | 10.4 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | 5.1 | | 5.6 | | 6.4 | | 7.5 | | 10.5 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | 5.1 | | 5.6 | | 6.4 | | 7.5 | | 10.5 | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 5.7 | | 6.3 | | 7.1 | | 8.4 | | 11.9 | ns |
| $t_{ACO}$ | Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 8.0 | | 8.9 | | 10.1 | | 11.9 | | 16.7 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.06 | ns/pF |

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, point and position whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

*Table 41 •* **A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| **Logic Module Propagation Delays**[1] | | | | | | | | | | | | |
| $t_{PD1}$ | Single Module | | 1.9 | | 2.1 | | 2.4 | | 2.8 | | 4.0 | ns |
| $t_{CO}$ | Sequential Clock-to-Q | | 2.0 | | 2.2 | | 2.5 | | 3.0 | | 4.2 | ns |
| $t_{GO}$ | Latch G-to-Q | | 1.9 | | 2.1 | | 2.4 | | 2.8 | | 4.0 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset-to-Q | | 2.2 | | 2.4 | | 2.8 | | 3.3 | | 4.6 | ns |
| **Logic Module Predicted Routing Delays**[2] | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 1.1 | | 1.2 | | 1.4 | | 1.6 | | 2.3 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.5 | | 1.6 | | 1.8 | | 2.1 | | 3.0 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 3.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 2.2 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.5 | ns |

**Table 42 •** **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INPY}$ | Input Data Pad-to-Y | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{INGO}$ | Input Latch Gate-to-Output | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.6 | ns |
| $t_{INH}$ | Input Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Latch Set-Up | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{ILA}$ | Latch Active Pulse Width | 4.7 | | 5.2 | | 5.9 | | 6.9 | | 9.7 | | ns |

***Table 42 •*** **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Input Module Predicted Routing Delays**[2] | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 3.8 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 2.1 | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 2.3 | | 2.5 | | 2.9 | | 3.4 | | 4.8 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 2.5 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 3.4 | | 3.8 | | 4.3 | | 5.1 | | 7.1 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 32 | | 2.6 | | 2.9 | | 3.3 | | 3.9 | | 5.4 | ns |
| | | FO = 486 | | 2.9 | | 3.2 | | 3.6 | | 4.3 | | 5.9 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 32 | | 3.7 | | 4.1 | | 4.6 | | 5.4 | | 7.6 | ns |
| | | FO = 486 | | 4.3 | | 4.7 | | 5.4 | | 6.3 | | 8.8 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 32 | 2.2 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | | ns |
| | | FO = 486 | 2.4 | | 2.6 | | 3.0 | | 3.5 | | 4.9 | | ns |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 2.2 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | | ns |
| | | FO = 486 | 2.4 | | 2.6 | | 3.0 | | 3.5 | | 4.9 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| | | FO = 486 | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 486 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | | ns |
| | | FO = 486 | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | | ns |
| $t_P$ | Minimum Period (1/$f_{MAX}$) | FO = 32 | 4.7 | | 5.2 | | 5.7 | | 6.5 | | 10.9 | | ns |
| | | FO = 486 | 5.1 | | 5.7 | | 6.2 | | 7.1 | | 11.9 | | ns |

**Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| **TTL Output Module Timing[5] (continued)** | | | | | | | | | | | | |
| $t_{LH}$ | I/O Latch Output Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | 7.7 | | 8.5 | | 9.6 | | 11.3 | | 15.9 | ns |
| $t_{ACO}$ | Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | 14.8 | | 16.5 | | 18.7 | | 22.0 | | 30.8 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.10 | ns/pF |
| $d_{THL}$ | Capacitive Loading, HIGH to LOW | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| **CMOS Output Module Timing[5]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 4.8 | | 5.3 | | 5.5 | | 6.4 | | 9.0 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 3.5 | | 3.9 | | 4.1 | | 4.9 | | 6.8 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.4 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 3.4 | | 4.0 | | 5.0 | | 5.8 | | 8.2 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 7.2 | | 8.0 | | 9.0 | | 10.7 | | 14.9 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 6.7 | | 7.5 | | 8.5 | | 9.9 | | 13.9 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | 6.8 | | 7.6 | | 8.6 | | 10.1 | | 14.2 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | 6.8 | | 7.6 | | 8.6 | | 10.1 | | 14.2 | ns |
| $t_{LSU}$ | I/O Latch Set-Up | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{LH}$ | I/O Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | 7.7 | | 8.5 | | 9.6 | | 11.3 | | 15.9 | ns |
| $t_{ACO}$ | Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | 14.8 | | 16.5 | | 18.7 | | 22.0 | | 30.8 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.10 | ns/pF |
| $d_{THL}$ | Capacitive Loading, HIGH to LOW | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| $t_{HEXT}$ | Input Latch External Hold FO = 32 | 3.9 | | 4.3 | | 4.9 | | 5.7 | | 8.1 | | ns |
| | FO = 486 | 4.6 | | 5.2 | | 5.8 | | 6.9 | | 9.6 | | ns |
| $t_P$ | Minimum Period ($1/f_{MAX}$) FO = 32 | 7.8 | | 8.7 | | 9.5 | | 10.8 | | 18.2 | | ns |
| | FO = 486 | 8.6 | | 9.5 | | 10.4 | | 11.9 | | 19.9 | | ns |

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

***Table 45 •*** **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Input Module Predicted Routing Delays**[2] | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 3.2 | | 3.5 | | 4.1 | | 4.8 | | 6.7 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 7.7 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 4.2 | | 4.6 | | 5.3 | | 6.2 | | 8.7 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 6.1 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 32 | | 4.6 | | 5.1 | | 5.7 | | 6.7 | | 9.3 | ns |
| | | FO = 635 | | 5.0 | | 5.6 | | 6.3 | | 7.4 | | 10.3 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 32 | | 5.3 | | 5.9 | | 6.7 | | 7.8 | | 11.0 | ns |
| | | FO = 635 | | 6.8 | | 7.6 | | 8.6 | | 10.1 | | 14.1 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 32 | 2.5 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | | ns |
| | | FO = 635 | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | | ns |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 2.5 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | | ns |
| | | FO = 635 | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.2 | ns |
| | | FO = 635 | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.2 | ns |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 635 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 4.0 | | 4.4 | | 5.0 | | 5.9 | | 8.2 | | ns |
| | | FO = 635 | 4.6 | | 5.2 | | 5.9 | | 6.9 | | 9.6 | | ns |
| $t_P$ | Minimum Period ($1/f_{MAX}$) | FO = 32 | 9.2 | | 10.2 | | 11.1 | | 12.7 | | 21.2 | | ns |
| | | FO = 635 | 9.9 | | 11.0 | | 12.0 | | 13.8 | | 23.0 | | ns |
| $f_{MAX}$ | Maximum Datapath Frequency | FO = 32 | | 108 | | 98 | | 90 | | 79 | | 47 | MHz |
| | | FO = 635 | | 100 | | 91 | | 83 | | 73 | | 44 | MHz |
| **TTL Output Module Timing**[5] | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.4 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 4.2 | | 4.6 | | 5.2 | | 6.2 | | 8.6 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.7 | | 4.2 | | 4.7 | | 5.5 | | 7.7 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 4.1 | | 4.6 | | 5.2 | | 6.1 | | 8.5 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.34 | | 8.2 | | 9.3 | | 10.9 | | 15.3 | ns |
| **TTL Output Module Timing**[5] | | | | | | | | | | | | | |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 6.9 | | 7.6 | | 8.7 | | 10.2 | | 14.3 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 4.9 | | 5.5 | | 6.2 | | 7.3 | | 10.2 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 4.9 | | 5.5 | | 6.2 | | 7.3 | | 10.2 | ns |
| $t_{LSU}$ | I/O Latch Output Set-Up | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{LH}$ | I/O Latch Output Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | | 7.9 | | 8.8 | | 10.0 | | 11.8 | | 16.5 | ns |

***Table 51 •*** **PQ144**

| **PQ144** | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| 80 | GNDI |
| 81 | NC |
| 82 | I/O |
| 83 | I/O |
| 84 | I/O |
| 85 | I/O |
| 86 | I/O |
| 87 | I/O |
| 88 | VKS |
| 89 | VPP |
| 90 | VCC |
| 91 | VCCI |
| 92 | NC |
| 93 | VSV |
| 94 | I/O |
| 95 | I/O |
| 96 | I/O |
| 97 | I/O |
| 98 | I/O |
| 99 | I/O |
| 100 | GND |
| 101 | GNDI |
| 102 | NC |
| 103 | I/O |
| 104 | I/O |
| 105 | I/O |
| 106 | I/O |
| 107 | I/O |
| 108 | I/O |
| 109 | I/O |
| 110 | SDI |
| 111 | I/O |
| 112 | I/O |
| 113 | I/O |
| 114 | I/O |
| 115 | I/O |
| 116 | GNDQ |

**Table 52 • PQ160**

| **PQ160** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | WD, I/O |
| 97 | I/O | I/O | I/O |
| 98 | VCCA | VCCA | VCCA |
| 99 | GND | GND | GND |
| 100 | NC | I/O | I/O |
| 101 | I/O | I/O | I/O |
| 102 | I/O | I/O | I/O |
| 103 | NC | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | I/O | I/O | WD, I/O |
| 107 | I/O | I/O | WD, I/O |
| 108 | I/O | I/O | I/O |
| 109 | GND | GND | GND |
| 110 | NC | I/O | I/O |
| 111 | I/O | I/O | WD, I/O |
| 112 | I/O | I/O | WD, I/O |
| 113 | I/O | I/O | I/O |
| 114 | NC | VCCI | VCCI |
| 115 | I/O | I/O | WD, I/O |
| 116 | NC | I/O | WD, I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | TDI, I/O |
| 119 | I/O | I/O | TMS, I/O |
| 120 | GND | GND | GND |
| 121 | I/O | I/O | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | NC | I/O | I/O |
| 125 | GND | GND | GND |
| 126 | I/O | I/O | I/O |
| 127 | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O |
| 129 | NC | I/O | I/O |
| 130 | GND | GND | GND |
| 131 | I/O | I/O | I/O |

*Table 53 •* **PQ208**

| PQ208 | | | |
|---|---|---|---|
| **Pin Number** | **A42MX16 Function** | **A42MX24 Function** | **A42MX36 Function** |
| 21 | I/O | I/O | I/O |
| 22 | GND | GND | GND |
| 23 | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O |
| 27 | GND | GND | GND |
| 28 | VCCI | VCCI | VCCI |
| 29 | VCCA | VCCA | VCCA |
| 30 | I/O | I/O | I/O |
| 31 | I/O | I/O | I/O |
| 32 | VCCA | VCCA | VCCA |
| 33 | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O |
| 35 | I/O | I/O | I/O |
| 36 | I/O | I/O | I/O |
| 37 | I/O | I/O | I/O |
| 38 | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O |
| 40 | I/O | I/O | I/O |
| 41 | NC | I/O | I/O |
| 42 | NC | I/O | I/O |
| 43 | NC | I/O | I/O |
| 44 | I/O | I/O | I/O |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O |
| 50 | NC | I/O | I/O |
| 51 | NC | I/O | I/O |
| 52 | GND | GND | GND |
| 53 | GND | GND | GND |
| 54 | I/O | TMS, I/O | TMS, I/O |
| 55 | I/O | TDI, I/O | TDI, I/O |
| 56 | I/O | I/O | I/O |
| 57 | I/O | WD, I/O | WD, I/O |

**Figure 47 •** **VQ100**

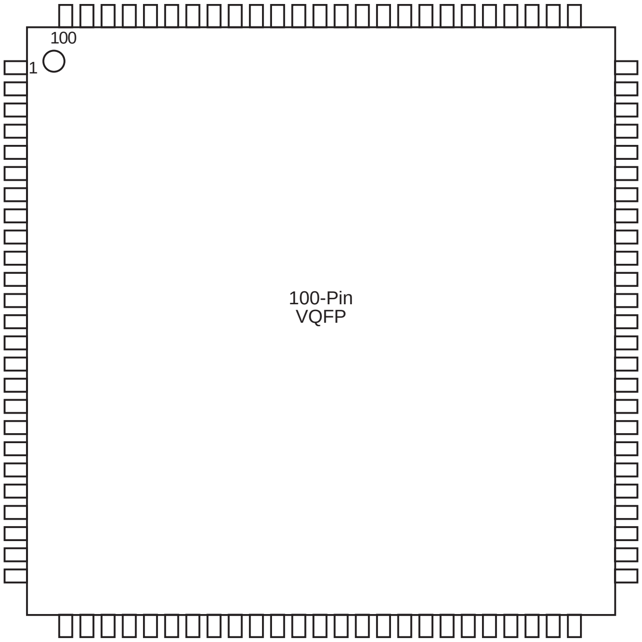


**Table 56 •** **VQ100**

| VQ100 | | |
|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** |
| 1 | I/O | I/O |
| 2 | MODE | MODE |
| 3 | I/O | I/O |
| 4 | I/O | I/O |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | GND | GND |
| 8 | I/O | I/O |
| 9 | I/O | I/O |
| 10 | I/O | I/O |
| 11 | I/O | I/O |
| 12 | I/O | I/O |
| 13 | I/O | I/O |
| 14 | VCCA | NC |
| 15 | VCCI | VCCI |
| 16 | I/O | I/O |
| 17 | I/O | I/O |
| 18 | I/O | I/O |
| 19 | I/O | I/O |
| 20 | GND | GND |

*Table 57 •* **TQ176**

| TQ176 | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 47 | I/O | I/O | TDI, I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | WD, I/O |
| 50 | I/O | I/O | WD, I/O |
| 51 | I/O | I/O | I/O |
| 52 | NC | VCCI | VCCI |
| 53 | I/O | I/O | I/O |
| 54 | NC | I/O | I/O |
| 55 | NC | I/O | WD, I/O |
| 56 | I/O | I/O | WD, I/O |
| 57 | NC | NC | I/O |
| 58 | I/O | I/O | I/O |
| 59 | I/O | I/O | WD, I/O |
| 60 | I/O | I/O | WD, I/O |
| 61 | NC | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | NC | I/O | I/O |
| 65 | I/O | I/O | I/O |
| 66 | NC | I/O | I/O |
| 67 | GND | GND | GND |
| 68 | VCCA | VCCA | VCCA |
| 69 | I/O | I/O | WD, I/O |
| 70 | I/O | I/O | WD, I/O |
| 71 | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O |
| 74 | NC | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | NC | NC | WD, I/O |
| 78 | NC | I/O | WD, I/O |
| 79 | I/O | I/O | I/O |
| 80 | NC | I/O | I/O |
| 81 | I/O | I/O | I/O |
| 82 | NC | VCCI | VCCI |
| 83 | I/O | I/O | I/O |

*Table 58 •* **CQ208**

| **CQ208** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 74 | I/O |
| 75 | I/O |
| 76 | I/O |
| 77 | I/O |
| 78 | GND |
| 79 | VCCA |
| 80 | VCCI |
| 81 | I/O |
| 82 | I/O |
| 83 | I/O |
| 84 | I/O |
| 85 | WD, I/O |
| 86 | WD, I/O |
| 87 | I/O |
| 88 | I/O |
| 89 | I/O |
| 90 | I/O |
| 91 | QCLKB, I/O |
| 92 | I/O |
| 93 | WD, I/O |
| 94 | WD, I/O |
| 95 | I/O |
| 96 | I/O |
| 97 | I/O |
| 98 | VCCI |
| 99 | I/O |
| 100 | WD, I/O |
| 101 | WD, I/O |
| 102 | I/O |
| 103 | TDO, I/O |
| 104 | I/O |
| 105 | GND |
| 106 | VCCA |
| 107 | I/O |
| 108 | I/O |
| 109 | I/O |
| 110 | I/O |