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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

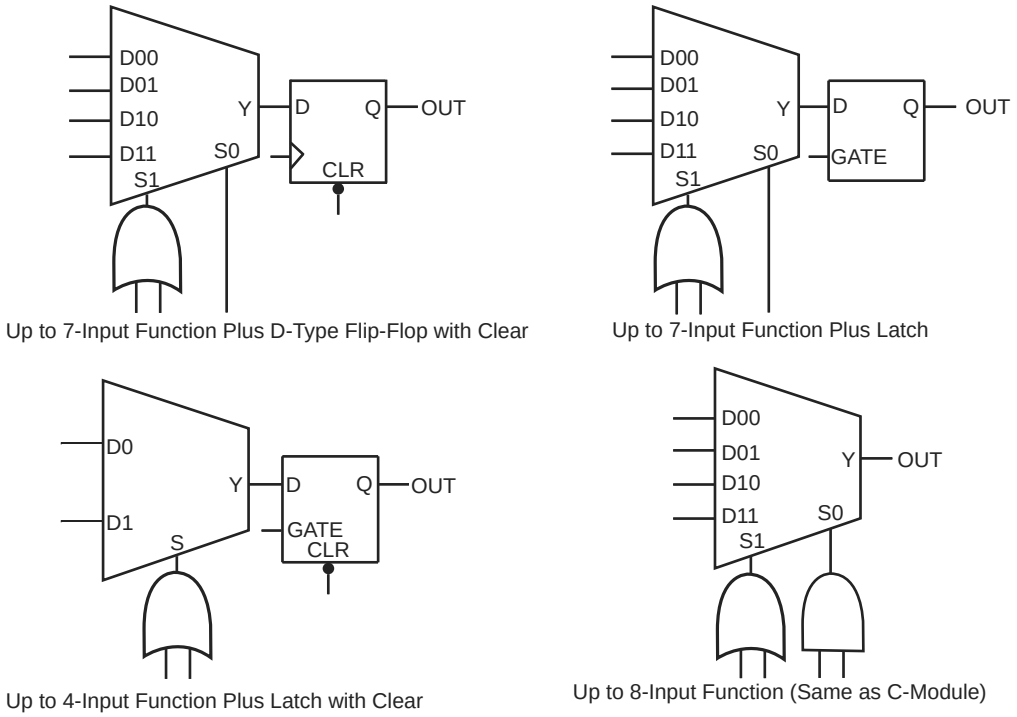
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 140 |
| Number of Gates | 24000 |
| Voltage - Supply | 3V ~ 3.6V, 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-2pq208 |

# Figures

# Tables

***Figure 4 •*** **42MX S-Module Implementation**




A42MX24 and A42MX36 devices contain D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry, providing a fast, wide-input AND function similar to that found in CPLD architectures (Figure 5, page 9). The D-module allows A42MX24 and A42MX36 devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin, and can also be fed back into the array to be incorporated into other logic.

## 3.2.2 Dual-Port SRAM Modules

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the A42MX36 dual-port SRAM block is shown in Figure 6, page 9.

The A42MX36 SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]), which are connected to segmented vertical routing tracks.

The A42MX36 dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring FIFO and LIFO queues. The ACTgen Macro Builder within Microsemi's designer software provides capability to quickly design memory functions with the SRAM blocks. Unused SRAM blocks can be used to implement registers for other user logic within the design.

***Figure 8 •*** **Clock Networks of 42MX Devices**

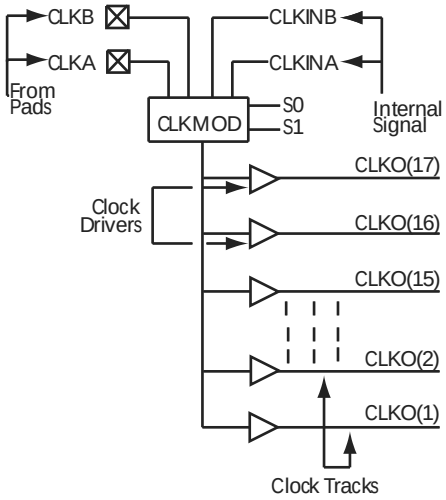
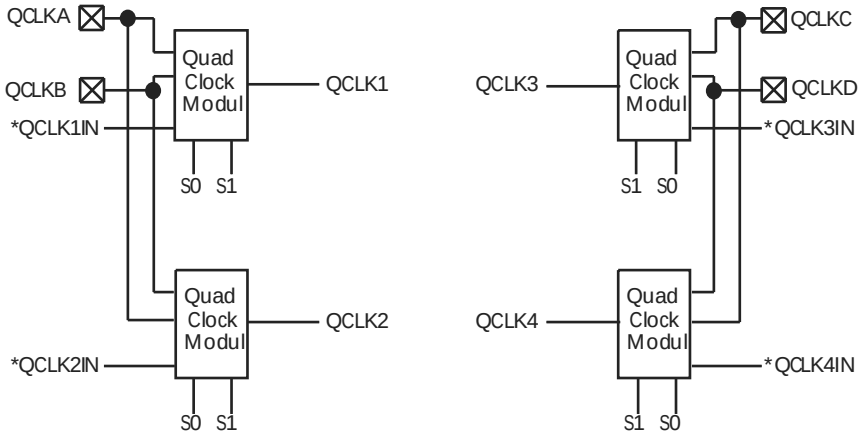



***Figure 9 •*** **Quadrant Clock Network of A42MX36 Devices**




**Note:** *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

## 3.2.5 MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 10, page 12 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (See the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

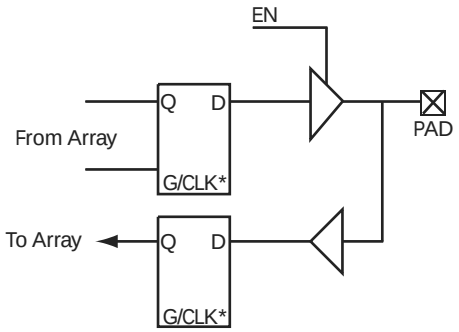
All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 10, page 12). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. See the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 µA.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 11, page 12). When the PCI fuse is not programmed, the output drive is standard.

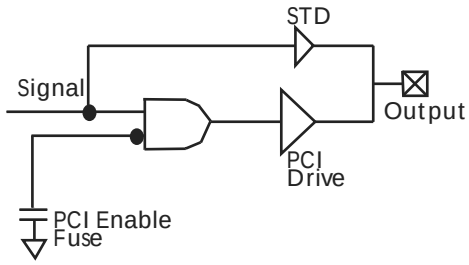
Designer software development tools provide a design library of I/O macro functions that can implement all I/O configurations supported by the MX FPGAs.

***Figure 10 •*** **42MX I/O Module**




***Note:*** **Can be configured as a Latch or D Flip-Flop (Using C-Module)*

***Figure 11 •*** **PCI Output Structure of A42MX24 and A42MX36 Devices**




# 3.3 Other Architectural Features

The following sections cover other architectural features of 40MX and 42MX FPGAs.

## 3.3.1 Performance

MX devices can operate with internal clock frequencies of 250 MHz, enabling fast execution of complex logic functions. MX devices are live on power-up and do not require auxiliary configuration devices and thus are an optimal platform to integrate the functionality contained in multiple programmable logic devices. In addition, designs that previously would have required a gate array to meet performance can be integrated into an MX device with improvements in cost and time-to-market. Using timing-driven place-and-route (TDPR) tools, designers can achieve highly deterministic device performance.

## 3.3.2 User Security

Microsemi FuseLock provides robust security against design theft. Special security fuses are hidden in the fabric of the device and protect against unauthorized users attempting to access the programming and/or probe interfaces. It is virtually impossible to identify or bypass these fuses without damaging the device, making Microsemi antifuse FPGAs protected with the highest level of security available from both invasive and noninvasive attacks.

Special security fuses in 40MX devices include the Probe Fuse and Program Fuse. The former disables the probing circuitry while the latter prohibits further programming of all fuses, including the Probe Fuse. In 42MX devices, there is the Security Fuse which, when programmed, both disables the probing circuitry and prohibits further programming of the device.

## 3.3.3 Programming

Device programming is supported through the Silicon Sculptor series of programmers. Silicon Sculptor is a compact, robust, single-site and multi-site device programmer for the PC. With standalone software, Silicon Sculptor is designed to allow concurrent programming of multiple units from the same PC.

**Note:** *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

***Table 14 •*** **Recommended Operating Conditions**

| Parameter | Commercial | Industrial | Military | Units |
|---|---|---|---|---|
| Temperature Range* | 0 to +70 | –40 to +85 | –55 to +125 | °C |
| VCC (40MX) | 4.75 to 5.25 | 4.5 to 5.5 | 4.5 to 5.5 | V |
| VCCA (42MX) | 4.75 to 5.25 | 4.5 to 5.5 | 4.5 to 5.5 | V |
| VCCI (42MX) | 4.75 to 5.25 | 4.5 to 5.5 | 4.5 to 5.5 | V |

**Note:** * Ambient temperature ($T_A$) is used for commercial and industrial grades; case temperature ($T_C$) is used for military grades.

## 3.7.1 5 V TTL Electrical Specifications

The following tables show 5 V TTL electrical specifications.

***Table 15 •*** **5V TTL Electrical Specifications**

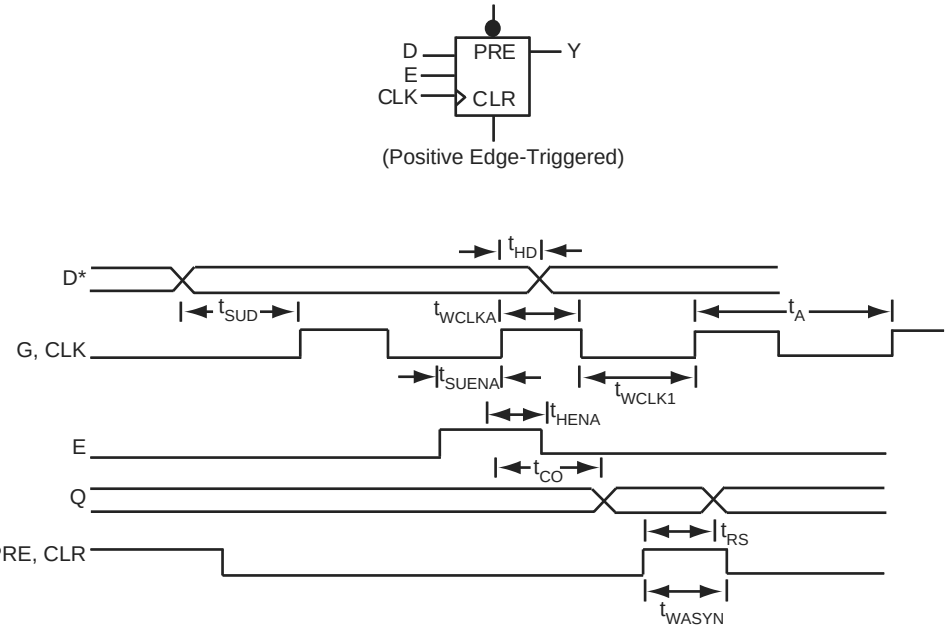
| | | Commercial | | Commercial -F | | Industrial | | Military | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| VOH[1] | IOH = –10 mA | 2.4 | | 2.4 | | | | | | V |
| | IOH = –4 mA | | | | | 3.7 | | 3.7 | | V |
| VOL[1] | IOL = 10 mA | | 0.5 | | 0.5 | | | | | V |
| | IOL = 6 mA | | | | | | 0.4 | | 0.4 | V |
| VIL | | –0.3 | 0.8 | –0.3 | 0.8 | –0.3 | 0.8 | –0.3 | 0.8 | V |
| VIH (40MX) | | 2.0 | VCC + 0.3 | 2.0 | VCC + 0.3 | 2.0 | VCC + 0.3 | 2.0 | VCC + 0.3 | V |
| VIH (42MX)[2] | | 2.0 | VCCI + 0.3 | 2.0 | VCCI + 0.3 | 2.0 | VCCI + 0.3 | 2.0 | VCCI + 0.3 | V |
| IIL | VIN = 0.5 V | | –10 | | –10 | | –10 | | –10 | µA |
| IIH | VIN = 2.7 V | | –10 | | –10 | | –10 | | –10 | µA |
| Input Transition Time, $T_R$ and $T_F$ | | | 500 | | 500 | | 500 | | 500 | ns |
| $C_{IO}$ I/O Capacitance | | | 10 | | 10 | | 10 | | 10 | pF |
| Standby Current, ICC[3] | A40MX02, A40MX04 | | 3 | | 25 | | 10 | | 25 | mA |
| | A42MX09 | | 5 | | 25 | | 25 | | 25 | mA |
| | A42MX16 | | 6 | | 25 | | 25 | | 25 | mA |
| | A42MX24, A42MX36 | | 20 | | 25 | | 25 | | 25 | mA |
| Low power mode Standby Current | 42MX devices only | | 0.5 | | ICC – 5.0 | | ICC – 5.0 | | ICC – 5.0 | mA |
| IIO, I/O source sink current | Can be derived from the *IBIS model* (http://www.microsemi.com/soc/techdocs/models/ibis.html) | | | | | | | | | |

1. Only one output tested at a time. VCC/VCCI = min
2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

## 3.10.2 Sequential Module Timing Characteristics

The following figure shows sequential module timing characteristics.

***Figure 25 •*** **Flip-Flops and Latches**




**Note:** *D represents all data functions involving A, B, and S for multiplexed flip-flops.

## 3.10.3 Sequential Timing Characteristics

The following figures show sequential timing characteristics.

***Figure 26 •*** **Input Buffer Latches**

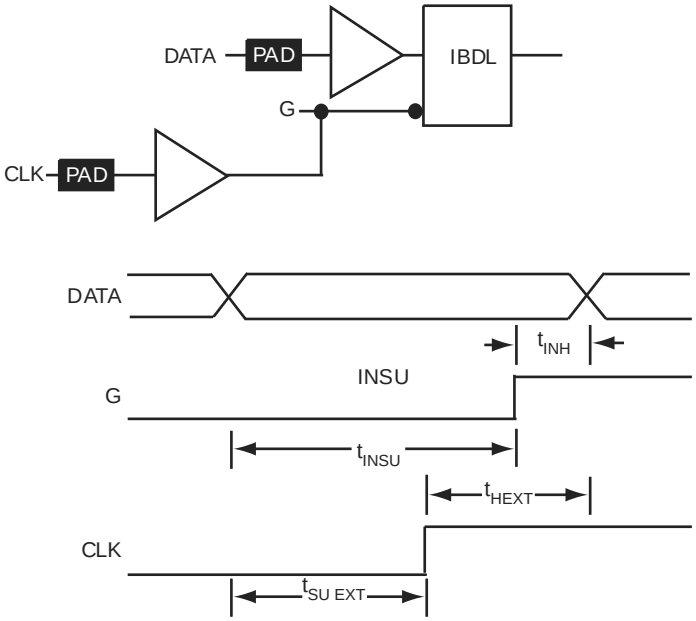
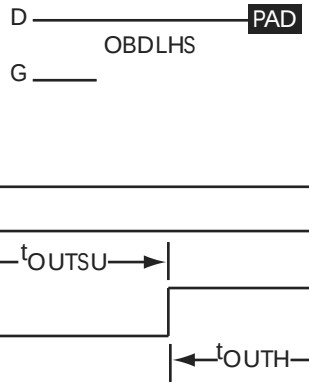


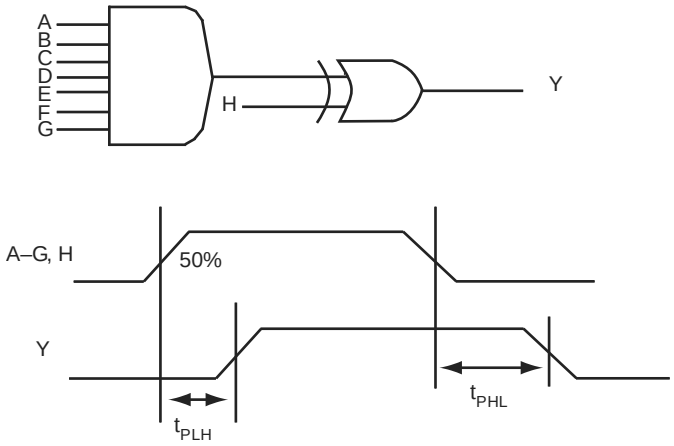
***Figure 27 •*** **Output Buffer Latches**




## 3.10.4 Decode Module Timing

The following figure shows decode module timing.

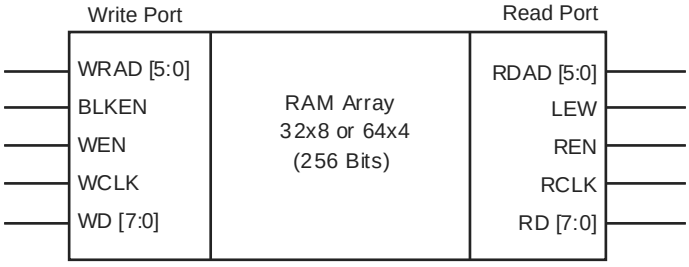
***Figure 28 •*** **Decode Module Timing**




## 3.10.5 SRAM Timing Characteristics

The following figure shows SRAM timing characteristics.

***Figure 29 •*** **SRAM Timing Characteristics**




## 3.10.6 Dual-Port SRAM Timing Waveforms

The following figures show dual-port SRAM timing waveforms.

***Table 41 •*** **A42MX16 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Sequential Timing[3, 4]** | | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Set-Up | | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 0.9 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | | 1.0 | | 1.1 | | 1.2 | | 1.4 | | 2.0 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | | 4.8 | | 5.3 | | 6.0 | | 7.1 | | 9.9 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | | 6.2 | | 6.9 | | 7.9 | | 9.2 | | 12.9 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | | 9.5 | | 10.6 | | 12.0 | | 14.1 | | 19.8 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Buffer Latch Set-Up | | 0.7 | | 0.8 | | 0.9 | | 1.01 | | 1.4 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTSU}$ | Output Buffer Latch Set-Up | | 0.7 | | 0.8 | | 0.89 | | 1.01 | | 1.4 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | | 129 | | 117 | | 108 | | 94 | | 56 | MHz |
| **Input Module Propagation Delays** | | | | | | | | | | | | | |
| $t_{INYH}$ | Pad-to-Y HIGH | | | 1.5 | | 1.6 | | 1.9 | | 2.2 | | 3.1 | ns |
| $t_{INYL}$ | Pad-to-Y LOW | | | 1.1 | | 1.3 | | 1.4 | | 1.7 | | 2.4 | ns |
| $t_{INGH}$ | G to Y HIGH | | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{INGL}$ | G to Y LOW | | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| **Input Module Predicted Routing Delays[2]** | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.6 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 2.9 | | 3.2 | | 3.7 | | 4.3 | | 6.1 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 3.3 | | 3.6 | | 4.1 | | 4.9 | | 6.8 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 3.6 | | 4.0 | | 4.6 | | 5.4 | | 7.6 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 5.1 | | 5.6 | | 6.4 | | 7.5 | | 10.5 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 32 | | 4.4 | | 4.8 | | 5.5 | | 6.5 | | 9.0 | ns |
| | | FO = 384 | | 4.8 | | 5.3 | | 6.0 | | 7.1 | | 9.9 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 32 | | 5.3 | | 5.9 | | 6.7 | | 7.8 | | 11.0 | ns |
| | | FO = 384 | | 6.2 | | 6.9 | | 7.9 | | 9.2 | | 12.9 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 32 | 5.7 | | 6.3 | | 7.1 | | 8.4 | | 11.8 | | ns |
| | | FO = 384 | 6.6 | | 7.4 | | 8.3 | | 9.8 | | 13.7 | | ns |

***Table 43 •*** **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Logic Module Sequential Timing[3, 4]** | | | | | | | | | | | | |
| $t_{CO}$ | Flip-Flop Clock-to-Output | | 2.1 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{GO}$ | Latch Gate-to-Output | | 3.4 | | 1.9 | | 2.1 | | 2.5 | | 3.4 | ns |
| $t_{SUD}$ | Flip-Flop (Latch) Set-Up Time | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 0.9 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RO}$ | Flip-Flop (Latch) Reset-to-Output | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 1.2 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.6 | | 5.2 | | 5.8 | | 6.9 | | 9.6 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 6.1 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INPY}$ | Input Data Pad-to-Y | | 1.4 | | 1.6 | | 1.8 | | 2.2 | | 3.0 | ns |
| $t_{INGO}$ | Input Latch Gate-to-Output | | 1.8 | | 1.9 | | 2.2 | | 2.6 | | 3.6 | ns |
| $t_{INH}$ | Input Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Latch Set-Up | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{ILA}$ | Latch Active Pulse Width | 6.5 | | 7.3 | | 8.2 | | 9.7 | | 13.5 | | ns |

***Table 49 •*** **PL84**

| **PL84** | | | | |
|---|---|---|---|---|
| **Pin Number** | **A40MX04 Function** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 84 | I/O | VCCA | VCCA | VCCA |

***Figure 41 •*** **PQ100**

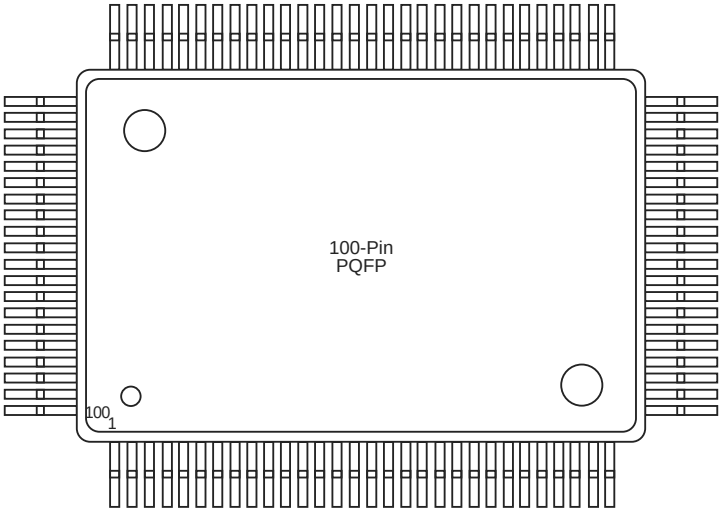



***Table 50 •*** **PQ 100**

| **PQ100** | | | | |
|---|---|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** | **A42MX09 Function** | **A42MX16 Function** |
| 1 | NC | NC | I/O | I/O |
| 2 | NC | NC | DCLK, I/O | DCLK, I/O |
| 3 | NC | NC | I/O | I/O |
| 4 | NC | NC | MODE | MODE |
| 5 | NC | NC | I/O | I/O |
| 6 | PRB, I/O | PRB, I/O | I/O | I/O |
| 7 | I/O | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O | I/O |
| 9 | I/O | I/O | GND | GND |
| 10 | I/O | I/O | I/O | I/O |
| 11 | I/O | I/O | I/O | I/O |
| 12 | I/O | I/O | I/O | I/O |
| 13 | GND | GND | I/O | I/O |
| 14 | I/O | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O | I/O |
| 16 | I/O | I/O | VCCA | VCCA |
| 17 | I/O | I/O | VCCI | VCCA |
| 18 | I/O | I/O | I/O | I/O |

***Table 50 •*** **PQ 100**

| **PQ100** | | | | |
|---|---|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** | **A42MX09 Function** | **A42MX16 Function** |
| 19 | VCC | $V_{CC}$ | I/O | I/O |
| 20 | I/O | I/O | I/O | I/O |
| 21 | I/O | I/O | I/O | I/O |
| 22 | I/O | I/O | GND | GND |
| 23 | I/O | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O | I/O |
| 27 | NC | NC | I/O | I/O |
| 28 | NC | NC | I/O | I/O |
| 29 | NC | NC | I/O | I/O |
| 30 | NC | NC | I/O | I/O |
| 31 | NC | I/O | I/O | I/O |
| 32 | NC | I/O | I/O | I/O |
| 33 | NC | I/O | I/O | I/O |
| 34 | I/O | I/O | GND | GND |
| 35 | I/O | I/O | I/O | I/O |
| 36 | GND | GND | I/O | I/O |
| 37 | GND | GND | I/O | I/O |
| 38 | I/O | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O | I/O |
| 40 | I/O | I/O | VCCA | VCCA |
| 41 | I/O | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O | I/O |
| 43 | VCC | VCC | I/O | I/O |
| 44 | VCC | VCC | I/O | I/O |
| 45 | I/O | I/O | I/O | I/O |
| 46 | I/O | I/O | GND | GND |
| 47 | I/O | I/O | I/O | I/O |
| 48 | NC | I/O | I/O | I/O |
| 49 | NC | I/O | I/O | I/O |
| 50 | NC | I/O | I/O | I/O |
| 51 | NC | NC | I/O | I/O |
| 52 | NC | NC | SDO, I/O | SDO, I/O |
| 53 | NC | NC | I/O | I/O |
| 54 | NC | NC | I/O | I/O |
| 55 | NC | NC | I/O | I/O |

***Table 51 •*** **PQ144**

| **PQ144** | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| 43 | I/O |
| 44 | GNDQ |
| 45 | GNDI |
| 46 | NC |
| 47 | I/O |
| 48 | I/O |
| 49 | I/O |
| 50 | I/O |
| 51 | I/O |
| 52 | I/O |
| 53 | I/O |
| 54 | VCC |
| 55 | VCCI |
| 56 | NC |
| 57 | I/O |
| 58 | I/O |
| 59 | I/O |
| 60 | I/O |
| 61 | I/O |
| 62 | I/O |
| 63 | I/O |
| 64 | GND |
| 65 | GNDI |
| 66 | I/O |
| 67 | I/O |
| 68 | I/O |
| 69 | I/O |
| 70 | I/O |
| 71 | SDO |
| 72 | I/O |
| 73 | I/O |
| 74 | I/O |
| 75 | I/O |
| 76 | I/O |
| 77 | I/O |
| 78 | I/O |
| 79 | GNDQ |

***Table 53 •*** **PQ208**

| **PQ208** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX16 Function** | **A42MX24 Function** | **A42MX36 Function** |
| 95 | NC | I/O | I/O |
| 96 | NC | I/O | I/O |
| 97 | NC | I/O | I/O |
| 98 | VCCI | VCCI | VCCI |
| 99 | I/O | I/O | I/O |
| 100 | I/O | WD, I/O | WD, I/O |
| 101 | I/O | WD, I/O | WD, I/O |
| 102 | I/O | I/O | I/O |
| 103 | SDO, I/O | SDO, TDO, I/O | SDO, TDO, I/O |
| 104 | I/O | I/O | I/O |
| 105 | GND | GND | GND |
| 106 | NC | VCCA | VCCA |
| 107 | I/O | I/O | I/O |
| 108 | I/O | I/O | I/O |
| 109 | I/O | I/O | I/O |
| 110 | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O |
| 112 | NC | I/O | I/O |
| 113 | NC | I/O | I/O |
| 114 | NC | I/O | I/O |
| 115 | NC | I/O | I/O |
| 116 | I/O | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O |
| 125 | I/O | I/O | I/O |
| 126 | GND | GND | GND |
| 127 | I/O | I/O | I/O |
| 128 | I/O | TCK, I/O | TCK, I/O |
| 129 | LP | LP | LP |
| 130 | VCCA | VCCA | VCCA |
| 131 | GND | GND | GND |

***Table 54 •*** **PQ240**

| **PQ240** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 163 | WD, I/O |
| 164 | WD, I/O |
| 165 | I/O |
| 166 | QCLKA, I/O |
| 167 | I/O |
| 168 | I/O |
| 169 | I/O |
| 170 | I/O |
| 171 | I/O |
| 172 | VCCI |
| 173 | I/O |
| 174 | WD, I/O |
| 175 | WD, I/O |
| 176 | I/O |
| 177 | I/O |
| 178 | TDI, I/O |
| 179 | TMS, I/O |
| 180 | GND |
| 181 | VCCA |
| 182 | GND |
| 183 | I/O |
| 184 | I/O |
| 185 | I/O |
| 186 | I/O |
| 187 | I/O |
| 188 | I/O |
| 189 | I/O |
| 190 | I/O |
| 191 | I/O |
| 192 | VCCI |
| 193 | I/O |
| 194 | I/O |
| 195 | I/O |
| 196 | I/O |
| 197 | I/O |
| 198 | I/O |
| 199 | I/O |

***Table 55 •*** **VQ80**

| **VQ80** | | |
|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** |
| 49 | I/O | I/O |
| 50 | CLK, I/O | CLK, I/O |
| 51 | I/O | I/O |
| 52 | MODE | MODE |
| 53 | VCC | VCC |
| 54 | NC | I/O |
| 55 | NC | I/O |
| 56 | NC | I/O |
| 57 | SDI, I/O | SDI, I/O |
| 58 | DCLK, I/O | DCLK, I/O |
| 59 | PRA, I/O | PRA, I/O |
| 60 | NC | NC |
| 61 | PRB, I/O | PRB, I/O |
| 62 | I/O | I/O |
| 63 | I/O | I/O |
| 64 | I/O | I/O |
| 65 | I/O | I/O |
| 66 | I/O | I/O |
| 67 | I/O | I/O |
| 68 | GND | GND |
| 69 | I/O | I/O |
| 70 | I/O | I/O |
| 71 | I/O | I/O |
| 72 | I/O | I/O |
| 73 | I/O | I/O |
| 74 | VCC | **VCC** |
| 75 | I/O | I/O |
| 76 | I/O | I/O |
| 77 | I/O | I/O |
| 78 | I/O | I/O |
| 79 | I/O | I/O |
| 80 | I/O | I/O |

***Table 58 •*** **CQ208**

| **CQ208** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 1 | GND |
| 2 | VCCA |
| 3 | MODE |
| 4 | I/O |
| 5 | I/O |
| 6 | I/O |
| 7 | I/O |
| 8 | I/O |
| 9 | I/O |
| 10 | I/O |
| 11 | I/O |
| 12 | I/O |
| 13 | I/O |
| 14 | I/O |
| 15 | I/O |
| 16 | I/O |
| 17 | VCCA |
| 18 | I/O |
| 19 | I/O |
| 20 | I/O |
| 21 | I/O |
| 22 | GND |
| 23 | I/O |
| 24 | I/O |
| 25 | I/O |
| 26 | I/O |
| 27 | GND |
| 28 | VCCI |
| 29 | VCCA |
| 30 | I/O |
| 31 | I/O |
| 32 | VCCA |
| 33 | I/O |
| 34 | I/O |
| 35 | I/O |
| 36 | I/O |

***Table 59 •*** **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 22 | I/O |
| 23 | I/O |
| 24 | I/O |
| 25 | I/O |
| 26 | VCCA |
| 27 | I/O |
| 28 | I/O |
| 29 | VCCA |
| 30 | VCCI |
| 31 | GND |
| 32 | VCCA |
| 33 | LP |
| 34 | TCK, I/O |
| 35 | I/O |
| 36 | GND |
| 37 | I/O |
| 38 | I/O |
| 39 | I/O |
| 40 | I/O |
| 41 | I/O |
| 42 | I/O |
| 43 | I/O |
| 44 | I/O |
| 45 | I/O |
| 46 | I/O |
| 47 | I/O |
| 48 | GND |
| 49 | I/O |
| 50 | I/O |
| 51 | I/O |
| 52 | I/O |
| 53 | I/O |
| 54 | I/O |
| 55 | I/O |
| 56 | I/O |
| 57 | I/O |
| 58 | I/O |

***Table 62 •*** **CQ172**

| | |
|---|---|
| 99 | I/O |
| 100 | I/O |
| 101 | I/O |
| 102 | I/O |
| 103 | GND |
| 104 | I/O |
| 105 | I/O |
| 106 | VKS |
| 107 | VPP |
| 108 | GND |
| 109 | VCCI |
| 110 | VSV |
| 111 | I/O |
| 112 | I/O |
| 113 | VCC |
| 114 | I/O |
| 115 | I/O |
| 116 | I/O |
| 117 | I/O |
| 118 | GND |
| 119 | I/O |
| 120 | I/O |
| 121 | I/O |
| 122 | I/O |
| 123 | GNDI |
| 124 | I/O |
| 125 | I/O |
| 126 | I/O |
| 127 | I/O |
| 128 | I/O |
| 129 | I/O |
| 130 | I/O |
| 131 | SDI |
| 132 | I/O |
| 133 | I/O |
| 134 | I/O |
| 135 | I/O |
| 136 | VCCI |
| 137 | I/O |