Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	140
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	176-LQFP
Supplier Device Package	176-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a42mx16-2tq176i

Figures

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- Table 15, page 21 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 22, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 23, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

1.2 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Added CQFP package information for A42MX16 device in Product Profile, page 1 and Ceramic Device Resources, page 4 (SAR 79522).
- Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in Temperature Grade Offerings, page 5 (SAR 79519)
- Changed Silicon Sculptor II to Silicon Sculptor in Programming, page 12 (SAR 38754)
- Added Figure 53, page 158 CQ172 package (SAR 79522).

1.3 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Added Figure 42, page 97 PQ144 Package for A42MX09 device (SAR 69776)
- Added Figure 52, page 153 PQ132 Package for A42MX09 device (SAR 69776)

1.4 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Added information on power-up behavior for A42MX24 and A42MX36 devices to the Power Supply, page 13 (SAR 42096
- Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793)

1.5 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- The FuseLock logo and accompanying text was removed from the User Security, page 12. This marking is no longer used on Microsemi devices (PCN 0915)
- The Development Tool Support, page 19 was updated (SAR 38512)

1.6 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- Ordering Information, page 3 was updated to include lead-free package ordering codes (SAR 21968)
- The User Security, page 12 was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673)

f_{q2} = Average second routed array clock rate in MHz)

Table 7 • **Fixed Capacitance Values for MX FPGAs (pF)**

Device Type	r1 routed_Clk1	r2 routed_Clk2
A40MX02	41.4	N/A
A40MX04	68.6	N/A
A42MX09	118	118
A42MX16	165	165
A42MX24	185	185
A42MX36	220	220

3.4.6 Test Circuitry and Silicon Explorer II Probe

MX devices contain probing circuitry that provides built-in access to every node in a design, via the use of Silicon Explorer II. Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer software, allow users to examine any of the internal nets of the device while it is operating in a prototyping or a production system. The user can probe into an MX device without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle and providing a true representation of the device under actual functional situations.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

Silicon Explorer II is used to control the MODE, DCLK, SDI and SDO pins in MX devices to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the MODE pin is held HIGH.

Figure 12, page 16 illustrates the interconnection between Silicon Explorer II and 40MX devices, while Figure 13, page 17 illustrates the interconnection between Silicon Explorer II and 42MX devices

To allow for probing capabilities, the security fuses must not be programmed. (See User Security, page 12 for the security fuses of 40MX and 42MX devices). Table 8, page 17 summarizes the possible device configurations for probing.

PRA and PRB pins are dual-purpose pins. When the “Reserve Probe Pin” is checked in the Designer software, PRA and PRB pins are reserved as dedicated outputs for probing. If PRA and PRB pins are required as user I/Os to achieve successful layout and “Reserve Probe Pin” is checked, the layout tool will override the option and place user I/Os on PRA and PRB pins.

Figure 12 • **Silicon Explorer II Setup with 40MX**

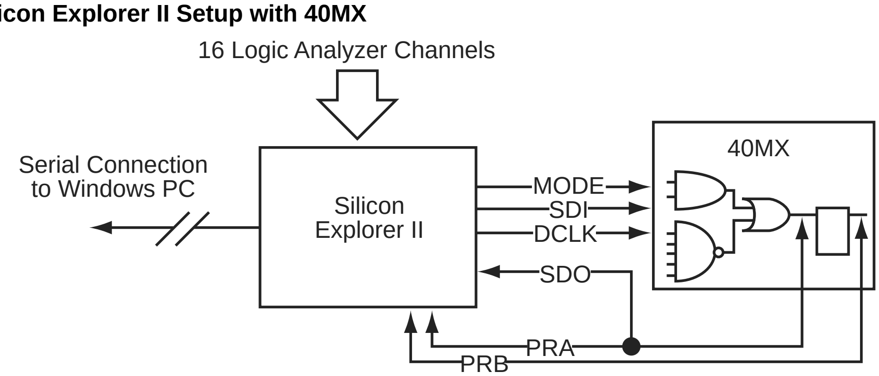

Figure 13 • **Silicon Explorer II Setup with 42MX**

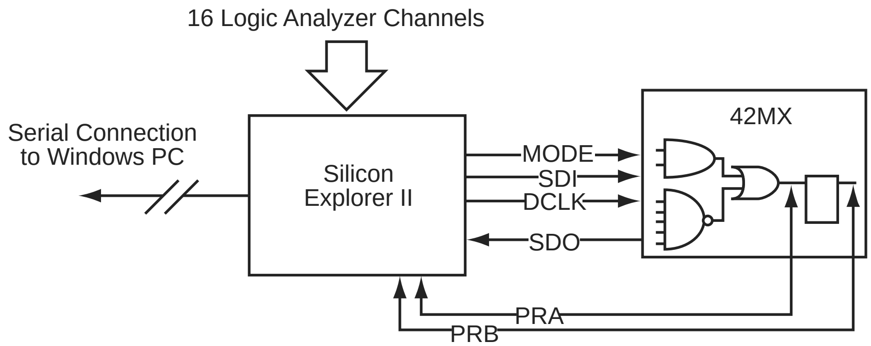

Table 8 • **Device Configuration Options for Probe Capability**

Security Fuse(s) Programmed	Mode	PRA, PRB[1]	SDI, SDO, DCLK[1]
No	LOW	User I/Os[2]	User I/Os[2]
No	HIGH	Probe Circuit Outputs	Probe Circuit Inputs
Yes	–	Probe Circuit Secured	Probe Circuit Secured

1. *Avoid using SDI, SDO, DCLK, PRA and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
2. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. See the Pin Descriptions,* page 83 *for information on unused I/O pins*

3.4.7 Design Consideration

It is recommended to use a series 70 : termination resistor on every probe connector (SDI, SDO, MODE, DCLK, PRA and PRB). The 70 : series termination is used to prevent data transmission corruption during probing and reading back the checksum.

3.4.8 IEEE Standard 1149.1 Boundary Scan Test (BST) Circuitry

42MX24 and 42MX36 devices are compatible with IEEE Standard 1149.1 (informally known as Joint Testing Action Group Standard or JTAG), which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic MX boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers and instruction register (Figure 14, page 18). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and some optional instructions. Table 9, page 18 describes the ports that control JTAG testing, while Table 10, page 18 describes the test instructions supported by these MX devices.

Each test section is accessed through the TAP, which has four associated pins: TCK (test clock input), TDI and TDO (test data input and output), and TMS (test mode selector).

The TAP controller is a four-bit state machine. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles.

42MX24 and 42MX36 devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary-scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

Figure 14 • **42MX IEEE 1149.1 Boundary Scan Circuitry**

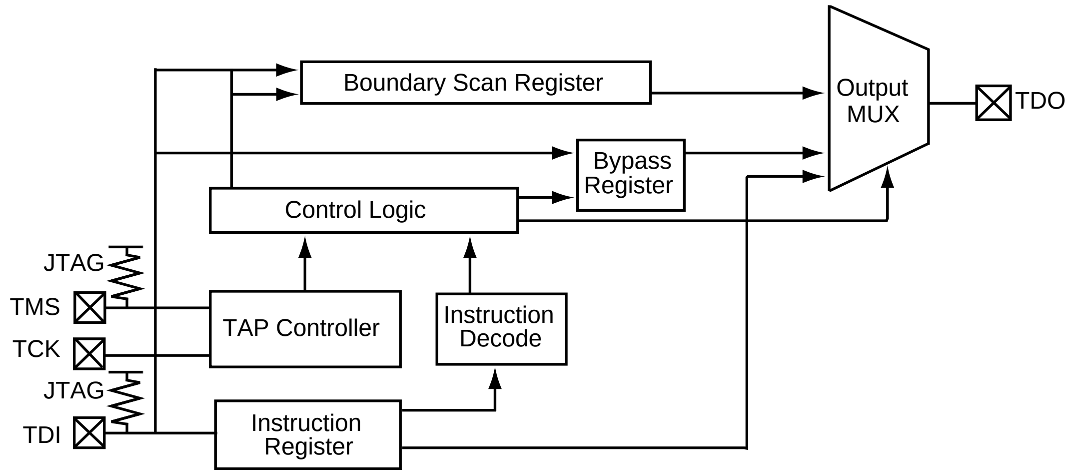

Table 9 • **Test Access Port Descriptions**

Port	Description
TMS (Test Mode Select)	Serial input for the test logic control bits. Data is captured on the rising edge of the test logic clock (TCK).
TCK (Test Clock Input)	Dedicated test logic clock used serially to shift test instruction, test data, and control inputs on the rising edge of the clock, and serially to shift the output data on the falling edge of the clock. The maximum clock frequency for TCK is 20 MHz.
TDI (Test Data Input)	Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock.
TDO (Test Data Output)	Serial output for test instruction and data from the test logic. TDO is set to an Inactive Drive state (high impedance) when data scanning is not in progress.

Table 10 • **Supported BST Public Instructions**

Instruction	IR Code (IR2.IR0)	Instruction Type	Description
EXTEST	000	Mandatory	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
SAMPLE/PRELOAD	001	Mandatory	Allows a snapshot of the signals at the device pins to be captured and examined during operation
HIGH Z	101	Optional	Tristates all I/Os to allow external signals to drive pins. See the IEEE Standard 1149.1 specification.
CLAMP	110	Optional	Allows state of signals driven from component pins to be determined from the Boundary-Scan Register. See the IEEE Standard 1149.1 specification for details.
BYPASS	111	Mandatory	Enables the bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the test chain.

3.9.1 Mixed 5.0V/3.3V Electrical Specifications

Table 22 • **Mixed 5.0V/3.3V Electrical Specifications**

		Commercial		Commercial –F		Industrial		Military		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
VOH[1]	IOH = –10 mA	2.4		2.4						V
	IOH = –4 mA					2.4		2.4		V
VOL[1]	IOL = 10 mA		0.5		0.5					V
	IOL = 6 mA						0.4		0.4	V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH[2]		2.0	VCCA + 0.3	2.0	VCCA + 0.3	2.0	VCCA + 0.3	2.0	VCCA + 0.3	V
IL	VIN = 0.5 V		–10		–10		–10		–10	µA
IH	VIN = 2.7 V		–10		–10		–10		–10	µA
Input Transition Time, T_R and T_F			500		500		500		500	ns
C_{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC[3]	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		20		25		25		25	mA
Low Power Mode Standby Current			0.5		ICC – 5.0		ICC – 5.0		ICC – 5.0	mA
IIO I/O source sink current	Can be derived from the *IBIS model* (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCCI = min.
2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
3. All outputs unloaded. All inputs = VCCI or GND

3.9.2 Output Drive Characteristics for 5.0 V PCI Signaling

MX PCI device I/O drivers were designed specifically for high-performance PCI systems. Figure 16, page 28 shows the typical output drive characteristics of the MX devices. MX output drivers are compliant with the PCI Local Bus Specification.

Table 23 • **DC Specification (5.0 V PCI Signaling)[1]**

			PCI		MX		
Symbol	**Parameter**	**Condition**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
VCCI	Supply Voltage for I/Os		4.75	5.25	4.75	5.25[2]	V
VIH[3]	Input High Voltage		2.0	VCC + 0.5	2.0	VCCI + 0.3	V
VIL	Input Low Voltage		–0.5	0.8	–0.3	0.8	V
IIH	Input High Leakage Current	VIN = 2.7 V		70	—	10	µA
IIL	Input Low Leakage Current	VIN=0.5 V		–70	—	–10	µA
VOH	Output High Voltage	IOUT = –2 mA IOUT = –6 mA	2.4		 3.84		V
VOL	Output Low Voltage	IOUT = 3 mA, 6 mA		0.55	—	0.33	V

3.9.3 Output Drive Characteristics for 3.3 V PCI Signaling

Table 25 • **DC Specification (3.3 V PCI Signaling)[1]**

			PCI		MX		
Symbol	**Parameter**	**Condition**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
VCCI	Supply Voltage for I/Os		3.0	3.6	3.0	3.6[2]	V
VIH	Input High Voltage		0.5	VCC + 0.5	0.5	VCCI + 0.3	V
VIL	Input Low Voltage		–0.5	0.8	–0.3	0.8	V
IIH	Input High Leakage Current	VIN = 2.7 V		70		10	µA
IIL	Input Leakage Current			–70		–10	µA
VOH	Output High Voltage	IOUT = –2 mA	0.9		3.3		V
VOL	Output Low Voltage	IOUT = 3 mA, 6 mA		0.1		0.1 VCCI	V
C_{IN}	Input Pin Capacitance			10		10	pF
C_{CLK}	CLK Pin Capacitance		5	12		10	pF
L_{PIN}	Pin Inductance			20		< 8 nH[3]	nH

1. PCI Local Bus Specification, Version 2.1, Section 4.2.2.1.
2. Maximum rating for VCCI –0.5 V to 7.0V.
3. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

Table 26 • **AC Specifications for (3.3 V PCI Signaling)[*]**

			PCI		MX		
Symbol	**Parameter**	**Condition**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
ICL	Low Clamp Current	–5 < VIN d–1	–25 + (VIN +1) /0.015		–60	–10	mA
Slew (r)	Output Rise Slew Rate	0.2 V to 0.6 V load	1	4	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	0.6 V to 0.2 V load	1	4	2.8	4.0	V/ns

Note: *PCI Local Bus Specification, Version 2.1, Section 4.2.2.2.

Table 41 • A42MX16 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
Logic Module Sequential Timing[3, 4]													
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up		0.5		0.5		0.6		0.7		0.9		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up		1.0		1.1		1.2		1.4		2.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		4.8		5.3		6.0		7.1		9.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		6.2		6.9		7.9		9.2		12.9		ns
t_A	Flip-Flop Clock Input Period		9.5		10.6		12.0		14.1		19.8		ns
t_{INH}	Input Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Set-Up		0.7		0.8		0.9		1.01		1.4		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up		0.7		0.8		0.89		1.01		1.4		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency			129		117		108		94		56	MHz
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			1.5		1.6		1.9		2.2		3.1	ns
t_{INYL}	Pad-to-Y LOW			1.1		1.3		1.4		1.7		2.4	ns
t_{INGH}	G to Y HIGH			2.0		2.2		2.5		2.9		4.1	ns
t_{INGL}	G to Y LOW			2.0		2.2		2.5		2.9		4.1	ns
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			2.6		2.9		3.2		3.8		5.3	ns
t_{IRD2}	FO = 2 Routing Delay			2.9		3.2		3.7		4.3		6.1	ns
t_{IRD3}	FO = 3 Routing Delay			3.3		3.6		4.1		4.9		6.8	ns
t_{IRD4}	FO = 4 Routing Delay			3.6		4.0		4.6		5.4		7.6	ns
t_{IRD8}	FO = 8 Routing Delay			5.1		5.6		6.4		7.5		10.5	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32 FO = 384		4.4 4.8		4.8 5.3		5.5 6.0		6.5 7.1		9.0 9.9	ns ns
t_{CKL}	Input HIGH to LOW	FO = 32 FO = 384		5.3 6.2		5.9 6.9		6.7 7.9		7.8 9.2		11.0 12.9	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32 FO = 384	5.7 6.6		6.3 7.4		7.1 8.3		8.4 9.8		11.8 13.7		ns ns

Table 41 • A42MX16 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{ACO}	Array Clock-to-Out (Pad-to-Pad),64 Clock Loading		11.3		12.5		14.2		16.7		23.3	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

1. For dual-module macros use tPD1 + tRD1 + taped, to + tRD1 + taped, or tPD1 + tRD1 + tusk, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing ansalysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Logic Module Combinatorial Functions[1]												
t_{PD}	Internal Array Module Delay		1.2		1.3		1.5		1.8		2.5	ns
t_{PDD}	Internal Decode Module Delay		1.4		1.6		1.8		2.1		3.0	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.8		0.9		1.0		1.2		1.7	ns
t_{RD2}	FO = 2 Routing Delay		1.0		1.2		1.3		1.5		2.1	ns
t_{RD3}	FO = 3 Routing Delay		1.3		1.4		1.6		1.9		2.6	ns
t_{RD4}	FO = 4 Routing Delay		1.5		1.7		1.9		2.2		3.1	ns
t_{RD5}	FO = 8 Routing Delay		2.4		2.7		3.0		3.6		5.0	ns
Logic Module Sequential Timing[3, 4]												
t_{CO}	Flip-Flop Clock-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch Gate-to-Output		1.2		1.3		1.5		1.8		2.5	ns
t_{SUD}	Flip-Flop (Latch) Set-Up Time	0.3		0.4		0.4		0.5		0.7		ns
t_{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		1.4		1.6		1.8		2.1		2.9	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.4		0.5		0.5		0.6		0.8		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.3		6.5		9.0		ns

Table 49 • **PL84**

PL84				
Pin Number	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
47	I/O	I/O	I/O	WD, I/O
48	I/O	I/O	I/O	I/O
49	I/O	GND	GND	GND
50	I/O	I/O	I/O	WD, I/O
51	I/O	I/O	I/O	WD, I/O
52	I/O	SDO, I/O	SDO, I/O	SDO, TDO, I/O
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	GND	I/O	I/O	I/O
61	GND	I/O	I/O	I/O
62	I/O	I/O	I/O	TCK, I/O
63	I/O	LP	LP	LP
64	CLK, I/O	VCCA	VCCA	VCCA
65	I/O	VCCI	VCCI	VCCI
66	MODE	I/O	I/O	I/O
67	VCC	I/O	I/O	I/O
68	VCC	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	GND	GND	GND
71	I/O	I/O	I/O	I/O
72	SDI, I/O	I/O	I/O	I/O
73	DCLK, I/O	I/O	I/O	I/O
74	PRA, I/O	I/O	I/O	I/O
75	PRB, I/O	I/O	I/O	I/O
76	I/O	SDI, I/O	SDI, I/O	SDI, I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	WD, I/O
79	I/O	I/O	I/O	WD, I/O
80	I/O	I/O	I/O	WD, I/O
81	I/O	PRA, I/O	PRA, I/O	PRA, I/O
82	GND	I/O	I/O	I/O
83	I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O

Table 50 • **PQ 100**

PQ100				
Pin Number	**A40MX02 Function**	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**
56	VCC	VCC	I/O	I/O
57	I/O	I/O	GND	GND
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	I/O	I/O	I/O	I/O
61	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	GND	GND	I/O	I/O
64	I/O	I/O	LP	LP
65	I/O	I/O	VCCA	VCCA
66	I/O	I/O	VCCI	VCCI
67	I/O	I/O	VCCA	VCCA
68	I/O	I/O	I/O	I/O
69	VCC	VCC	I/O	I/O
70	I/O	I/O	I/O	I/O
71	I/O	I/O	I/O	I/O
72	I/O	I/O	GND	GND
73	I/O	I/O	I/O	I/O
74	I/O	I/O	I/O	I/O
75	I/O	I/O	I/O	I/O
76	I/O	I/O	I/O	I/O
77	NC	NC	I/O	I/O
78	NC	NC	I/O	I/O
79	NC	NC	SDI, I/O	SDI, I/O
80	NC	I/O	I/O	I/O
81	NC	I/O	I/O	I/O
82	NC	I/O	I/O	I/O
83	I/O	I/O	I/O	I/O
84	I/O	I/O	GND	GND
85	I/O	I/O	I/O	I/O
86	GND	GND	I/O	I/O
87	GND	GND	PRA, I/O	PRA, I/O
88	I/O	I/O	I/O	I/O
89	I/O	I/O	CLKA, I/O	CLKA, I/O
90	CLK, I/O	CLK, I/O	VCCA	VCCA
91	I/O	I/O	I/O	I/O
92	MODE	MODE	CLKB, I/O	CLKB, I/O

Table 51 • **PQ144**

PQ144	
Pin Number	**A42MX09 Function**
43	I/O
44	GNDQ
45	GNDI
46	NC
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	VCC
55	VCCI
56	NC
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	GND
65	GNDI
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	SDO
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	GNDQ

Table 53 • **PQ208**

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
169	I/O	WD, I/O	WD, I/O
170	I/O	I/O	I/O
171	NC	I/O	QCLKD, I/O
172	I/O	I/O	I/O
173	I/O	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	I/O	WD, I/O	WD, I/O
177	I/O	WD, I/O	WD, I/O
178	PRA, I/O	PRA, I/O	PRA, I/O
179	I/O	I/O	I/O
180	CLKA, I/O	CLKA, I/O	CLKA, I/O
181	NC	I/O	I/O
182	NC	VCCI	VCCI
183	VCCA	VCCA	VCCA
184	GND	GND	GND
185	I/O	I/O	I/O
186	CLKB, I/O	CLKB, I/O	CLKB, I/O
187	I/O	I/O	I/O
188	PRB, I/O	PRB, I/O	PRB, I/O
189	I/O	I/O	I/O
190	I/O	WD, I/O	WD, I/O
191	I/O	WD, I/O	WD, I/O
192	I/O	I/O	I/O
193	NC	I/O	I/O
194	NC	WD, I/O	WD, I/O
195	NC	WD, I/O	WD, I/O
196	I/O	I/O	QCLKC, I/O
197	NC	I/O	I/O
198	I/O	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	NC	I/O	I/O
202	VCCI	VCCI	VCCI
203	I/O	WD, I/O	WD, I/O
204	I/O	WD, I/O	WD, I/O
205	I/O	I/O	I/O

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
244	WD, I/O
245	I/O
246	I/O
247	I/O
248	VCCI
249	I/O
250	WD, I/O
251	WD, I/O
252	I/O
253	SDI, I/O
254	I/O
255	GND
256	NC

Figure 51 • **BG272**

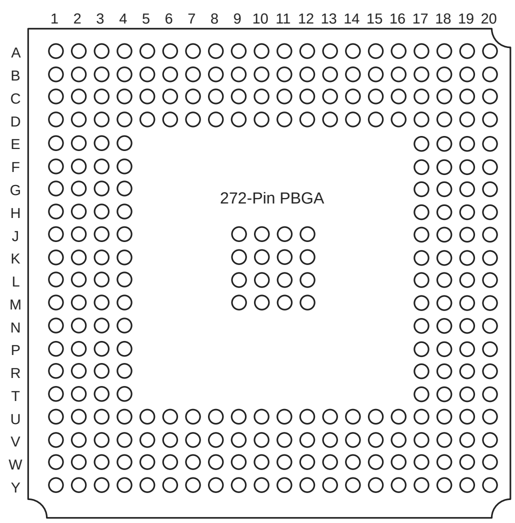

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
A1	GND
A2	GND
A3	I/O
A4	WD, I/O
A5	I/O