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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	72
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-pl84a

Contents

2   40MX and 42MX FPGA Families

2.1   Features

The following sections list out various features of the 40MX and 42MX FPGA family devices.

2.1.1   High Capacity

- Single-Chip ASIC Alternative
- 3,000 to 54,000 System Gates
- Up to 2.5 kbits Configurable Dual-Port SRAM
- Fast Wide-Decode Circuitry
- Up to 202 User-Programmable I/O Pins

2.1.2   High Performance

- 5.6 ns Clock-to-Out
- 250 MHz Performance
- 5 ns Dual-Port SRAM Access
- 100 MHz FIFOs
- 7.5 ns 35-Bit Address Decode

2.1.3   HiRel Features

- Commercial, Industrial, Automotive, and Military Temperature Plastic Packages
- Commercial, Military Temperature, and MIL-STD-883 Ceramic Packages
- QML Certification
- Ceramic Devices Available to DSCC SMD

2.1.4   Ease of Integration

- Mixed-Voltage Operation (5.0 V or 3.3 V for core and I/Os), with PCI-Compliant I/Os
- Up to 100% Resource Utilization and 100% Pin Locking
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Low Power Consumption
- IEEE Standard 1149.1 (JTAG) Boundary Scan Testing

2.2   Product Profile

The following table gives the features of the products.

Table 1 •   **Product profile**

Device	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
Capacity						
System Gates	3,000	6,000	14,000	24,000	36,000	54,000
SRAM Bits	–	–	–	–	–	2,560
Logic Modules						
Sequential	–	–	348	624	954	1,230
Combinatorial	295	547	336	608	912	1,184
Decode	–	–	–	–	24	24
Clock-to-Out	9.5 ns	9.5 ns	5.6 ns	6.1 ns	6.1 ns	6.3 ns
SRAM Modules (64x4 or 32x8)	–	–	–	–	–	10
Dedicated Flip-Flops	–	–	348	624	954	1,230

Table 1 •   **Product profile**

Device	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
Maximum Flip-Flops	147	273	516	928	1,410	1,822
Clocks	1	1	2	2	2	6
User I/O (maximum)	57	69	104	140	176	202
PCI	–	–	–	–	Yes	Yes
Boundary Scan Test (BST)	–	–	–	–	Yes	Yes
Packages (by pin count) PLCC PQFP VQFP TQFP CQFP PBGA CPGA	 44, 68 100 80 – – – –	 44, 68, 84 100 80 – – – –	 84 100, 144, 160 100 176 – – 132	 84 100, 160, 208 100 176 172 – –	 84 160, 208 – 176 – – –	 – 208, 240 – – 208, 256 272 –

3   40MX and 42MX FPGAs

3.1   General Description

Microsemi's 40MX and 42MX families offer a cost-effective design solution at 5V. The MX devices are single-chip solutions and provide high performance while shortening the system design and development cycle. MX devices can integrate and consolidate logic implemented in multiple PALs, CPLDs, and FPGAs. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

The MX device architecture is based on Microsemi's patented antifuse technology implemented in a 0.45µm triple-metal CMOS process. With capacities ranging from 3,000 to 54,000 system gates, the MX devices provide performance up to 250 MHz, are live on power-up and have one-fifth the standby power consumption of comparable FPGAs. MX FPGAs provide up to 202 user I/Os and are available in a wide variety of packages and speed grades.

A42MX24 and A42MX36 devices also feature multiPlex I/Os, which support mixed-voltage systems, enable programmable PCI, deliver high-performance operation at both 5.0V and 3.3V, and provide a low-power mode. The devices are fully compliant with the PCI local bus specification (version 2.1). They deliver 200 MHz on-chip operation and 6.1 ns clock-to-output performance.

The 42MX24 and 42MX36 devices include system-level features such as IEEE Standard 1149.1 (JTAG) Boundary Scan Testing and fast wide-decode modules. In addition, the A42MX36 device offers dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The storage elements can efficiently address applications requiring wide data path manipulation and can perform transformation functions such as those required for telecommunications, networking, and DSP.

All MX devices are fully tested over automotive and military temperature ranges. In addition, the largest member of the family, the A42MX36, is available in both CQ208 and CQ256 ceramic packages screened to MIL-STD-883 levels. For easy prototyping and conversion from plastic to ceramic, the CQ208 and PQ208 devices are pin-compatible.
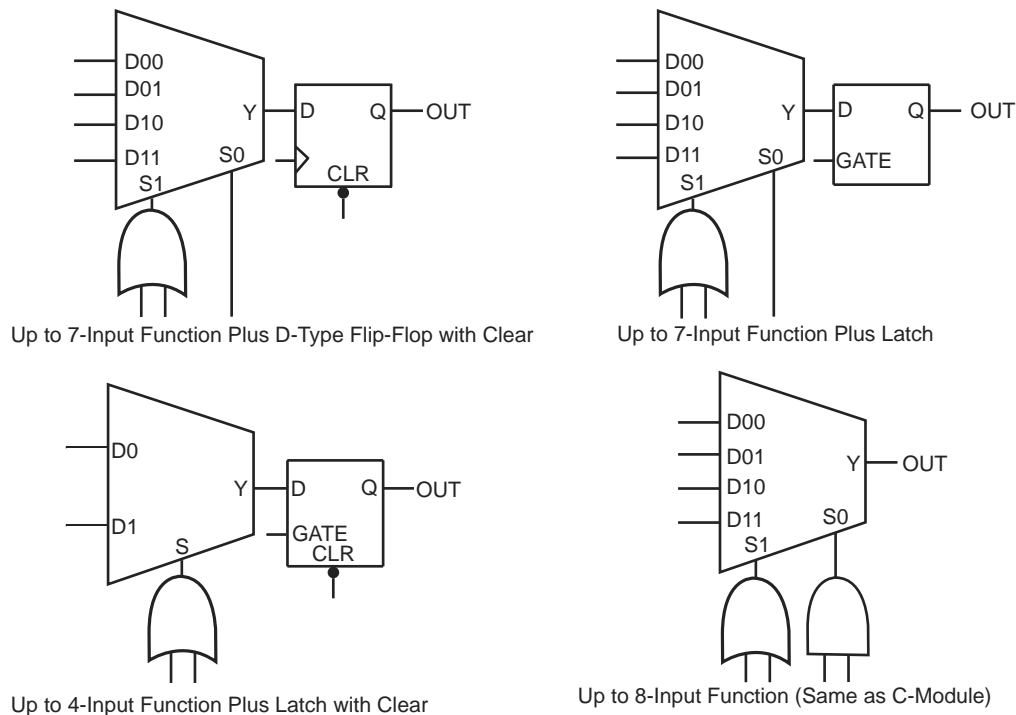
3.2   MX Architectural Overview

The MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within these families are composed of logic modules, I/O modules, routing resources and clock networks, which are the building blocks for fast logic designs. In addition, the A42MX36 device contains embedded dual-port SRAM modules, which are optimized for high-speed data path functions such as FIFOs, LIFOs and scratch pad memory. A42MX24 and A42MX36 also contain wide-decode modules.

3.2.1   Logic Modules

The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources.(see the following figure).

The logic module can implement the four basic logic functions (NAND, AND, OR and NOR) in gates of two, three, or four inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array; latches and flip-flops can be constructed from logic modules whenever required in the application.

Figure 4 •   **42MX S-Module Implementation**

Up to 7-Input Function Plus D-Type Flip-Flop with Clear

Up to 7-Input Function Plus Latch

Up to 4-Input Function Plus Latch with Clear

Up to 8-Input Function (Same as C-Module)

A42MX24 and A42MX36 devices contain D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry, providing a fast, wide-input AND function similar to that found in CPLD architectures (Figure 5, page 9). The D-module allows A42MX24 and A42MX36 devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin, and can also be fed back into the array to be incorporated into other logic.

3.2.2   **Dual-Port SRAM Modules**

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the A42MX36 dual-port SRAM block is shown in Figure 6, page 9.

The A42MX36 SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]), which are connected to segmented vertical routing tracks.

The A42MX36 dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring FIFO and LIFO queues. The ACTgen Macro Builder within Microsemi's designer software provides capability to quickly design memory functions with the SRAM blocks. Unused SRAM blocks can be used to implement registers for other user logic within the design.

f_{q2} = Average second routed array clock rate in MHz)

Table 7 • **Fixed Capacitance Values for MX FPGAs (pF)**

Device Type	r1 routed_Clk1	r2 routed_Clk2
A40MX02	41.4	N/A
A40MX04	68.6	N/A
A42MX09	118	118
A42MX16	165	165
A42MX24	185	185
A42MX36	220	220

3.4.6 Test Circuitry and Silicon Explorer II Probe

MX devices contain probing circuitry that provides built-in access to every node in a design, via the use of Silicon Explorer II. Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer software, allow users to examine any of the internal nets of the device while it is operating in a prototyping or a production system. The user can probe into an MX device without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle and providing a true representation of the device under actual functional situations.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

Silicon Explorer II is used to control the MODE, DCLK, SDI and SDO pins in MX devices to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the MODE pin is held HIGH.

Figure 12, page 16 illustrates the interconnection between Silicon Explorer II and 40MX devices, while Figure 13, page 17 illustrates the interconnection between Silicon Explorer II and 42MX devices

To allow for probing capabilities, the security fuses must not be programmed. (See User Security, page 12 for the security fuses of 40MX and 42MX devices). Table 8, page 17 summarizes the possible device configurations for probing.

PRA and PRB pins are dual-purpose pins. When the "Reserve Probe Pin" is checked in the Designer software, PRA and PRB pins are reserved as dedicated outputs for probing. If PRA and PRB pins are required as user I/Os to achieve successful layout and "Reserve Probe Pin" is checked, the layout tool will override the option and place user I/Os on PRA and PRB pins.

Figure 12 • **Silicon Explorer II Setup with 40MX**
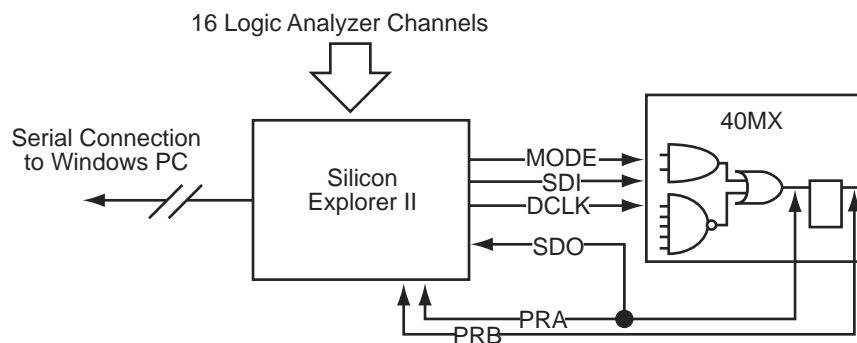
Figure 13 • **Silicon Explorer II Setup with 42MX**
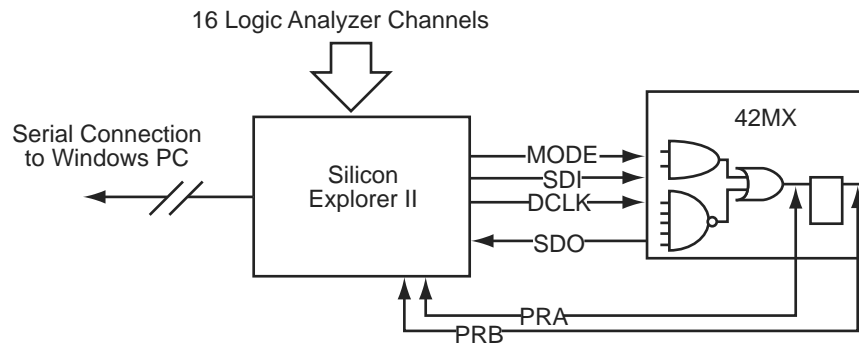
Table 8 • **Device Configuration Options for Probe Capability**

Security Fuse(s) Programmed	Mode	PRA, PRB[1]	SDI, SDO, DCLK[1]
No	LOW	User I/Os[2]	User I/Os[2]
No	HIGH	Probe Circuit Outputs	Probe Circuit Inputs
Yes	–	Probe Circuit Secured	Probe Circuit Secured

1. *Avoid using SDI, SDO, DCLK, PRA and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
2. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. See the Pin Descriptions, page 83 for information on unused I/O pins*

3.4.7   Design Consideration

It is recommended to use a series 70Ω termination resistor on every probe connector (SDI, SDO, MODE, DCLK, PRA and PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

3.4.8   IEEE Standard 1149.1 Boundary Scan Test (BST) Circuitry

42MX24 and 42MX36 devices are compatible with IEEE Standard 1149.1 (informally known as Joint Testing Action Group Standard or JTAG), which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic MX boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers and instruction register (Figure 14, page 18). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and some optional instructions. Table 9, page 18 describes the ports that control JTAG testing, while Table 10, page 18 describes the test instructions supported by these MX devices.

Each test section is accessed through the TAP, which has four associated pins: TCK (test clock input), TDI and TDO (test data input and output), and TMS (test mode selector).

The TAP controller is a four-bit state machine. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles.

42MX24 and 42MX36 devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

Figure 20 • **42MX Timing Model (SRAM Functions)**
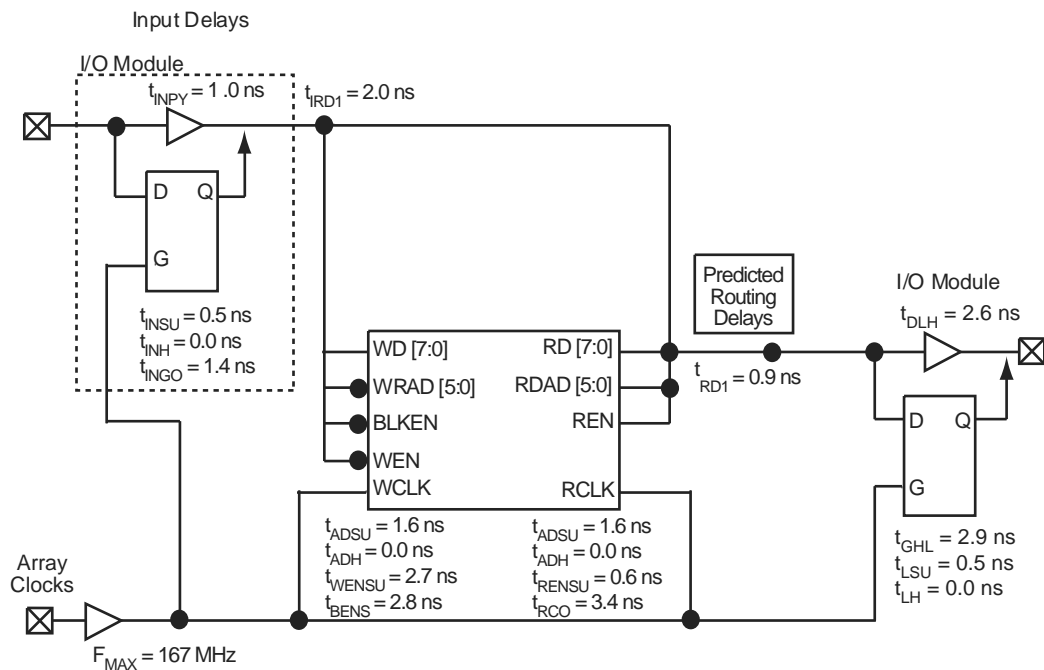
Note: Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions.

3.10.1 Parameter Measurement

The following figures show parameter measurement details.

Figure 21 • **Output Buffer Delays**
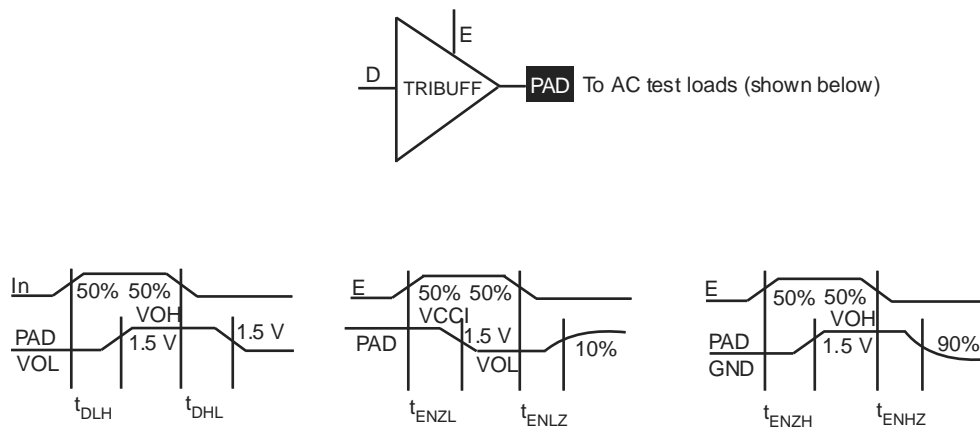
3.10.2 Sequential Module Timing Characteristics

The following figure shows sequential module timing characteristics.

Figure 25 • **Flip-Flops and Latches**

(Positive Edge-Triggered)
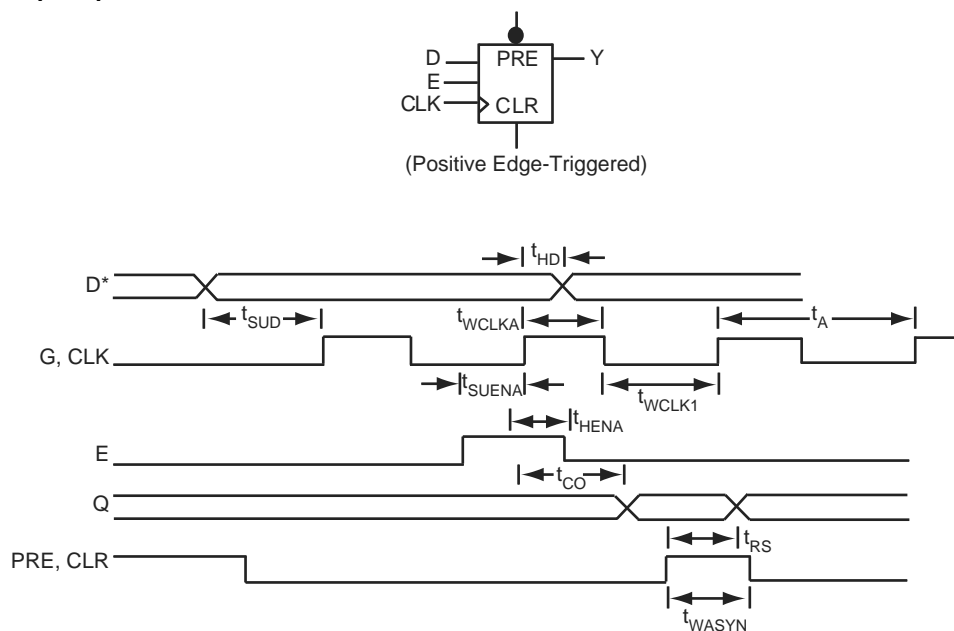
Note: *D represents all data functions involving A, B, and S for multiplexed flip-flops.

3.10.3 Sequential Timing Characteristics

The following figures show sequential timing characteristics.

Figure 26 • **Input Buffer Latches**
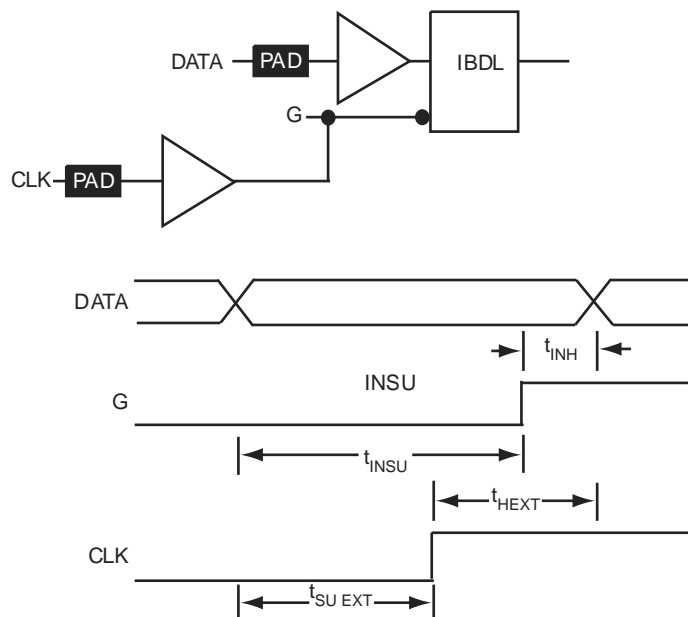
Figure 33 • **42MX SRAM Asynchronous Read Operation—Type 2 (Write Address Controlled)**
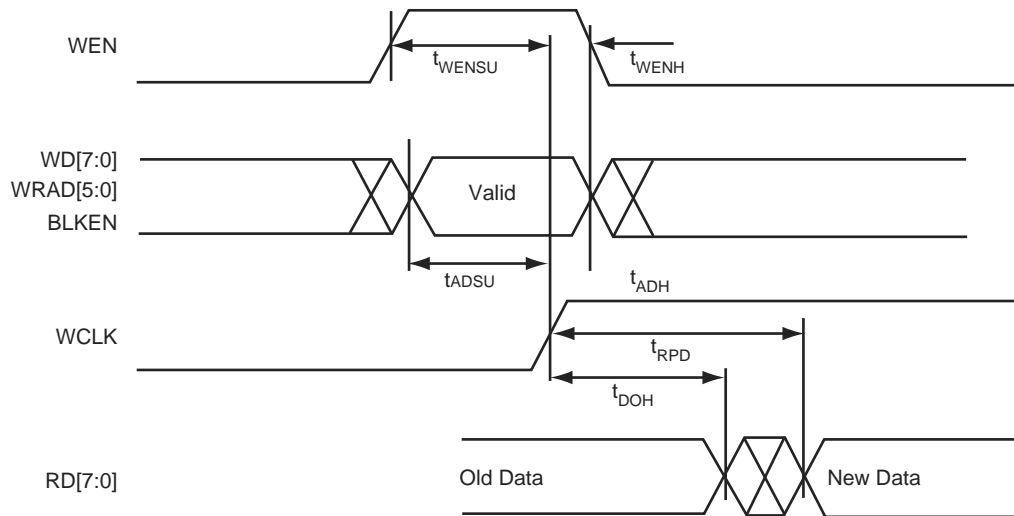
3.10.7 Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution, which is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi's patented antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 μm lithography, offer nominal levels of 100 Ω resistance and 7.0 fF capacitance per antifuse.

MX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90 percent of interconnects using only two antifuses.

3.11 Timing Characteristics

Device timing characteristics fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all MX devices. Internal routing delays are device-dependent; actual delays are not determined until after place-and-route of the user's design is complete. Delay values may then be determined by using the Designer software utility or by performing simulation with post-layout delays.

3.11.1 Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment in Microsemi's Designer software prior to placement and routing. Up to 6% of the nets in a design may be designated as critical.

3.11.2 Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks add

Table 33 • **Timing Parameters for 33 MHz PCI**

Symbol	Parameter	PCI Min.	Max.	A42MX24 Min.	Max.	A42MX36 Min.	Max.	Units
$t_{SU(PTP)}$	Input Set-Up Time to CLK—Point-to-Point	10, 12[2]	–	1.5	–	1.5	–	ns
t_H	Input Hold to CLK	0	–	0	–	0	–	ns

1. TOFF is system dependent. MX PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.
2. REQ# and GNT# are point-to-point signals and have different output valid delay and input setup times than do bussed signals. GNT# has a setup of 10; REW# has a setup of 12.

3.11.6.1   Timing Characteristics

The following tables list the timing characteristics.

Table 34 • **A40MX02 Timing Characteristics (Nominal 5.0 V Operation)**
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description	–3 Speed Min.	Max.	–2 Speed Min.	Max.	–1 Speed Min.	Max.	Std Speed Min.	Max.	–F Speed Min.	Max.	Units
Logic Module Propagation Delays											
t_{PD1} Single Module		1.2		1.4		1.6		1.9		2.7	ns
t_{PD2} Dual-Module Macros		2.7		3.1		3.5		4.1		5.7	ns
t_{CO} Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{GO} Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{RS} Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays[1]											
t_{RD1} FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.8	ns
t_{RD2} FO = 2 Routing Delay		1.8		2.1		2.4		2.8		3.9	ns
t_{RD3} FO = 3 Routing Delay		2.3		2.7		3.0		3.6		5.0	ns
t_{RD4} FO = 4 Routing Delay		2.9		3.3		3.7		4.4		6.1	ns
t_{RD8} FO = 8 Routing Delay		4.9		5.7		6.5		7.6		10.6	ns
Logic Module Sequential Timing[2]											
t_{SUD} Flip-Flop (Latch) Data Input Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t_{HD}[3] Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA} Flip-Flop (Latch) Enable Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t_{HENA} Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA} Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t_{WASYN} Flip-Flop (Latch) Asynchronous Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t_A Flip-Flop Clock Input Period	4.8		5.6		6.3		7.5		10.4		ns
f_{MAX} Flip-Flop (Latch) Clock Frequency (FO = 128)		181		168		154		134		80	MHz

Table 36 • **A40MX04 Timing Characteristics (Nominal 5.0 V Operation)** *(continued)***(Worst-Case Commercial Conditions, VCC = 4.75 V, TJ = 70°C)**

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
CMOS Output Module Timing[1]												
t_{DLH}	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t_{DHL}	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZH}	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZL}	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t_{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer utility from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading

Table 37 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCC = 3.0 V, TJ = 70°C)**

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
Logic Module Propagation Delays												
t_{PD1}	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t_{PD2}	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t_{CO}	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t_{GO}	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays[1]												
t_{RD1}	FO = 1 Routing Delay		1.9		2.2		2.5		3.0		4.2	ns
t_{RD2}	FO = 2 Routing Delay		2.7		3.1		3.5		4.1		5.7	ns
t_{RD3}	FO = 3 Routing Delay		3.4		3.9		4.4		5.2		7.3	ns
t_{RD4}	FO = 4 Routing Delay		4.1		4.8		5.4		6.3		8.9	ns
t_{RD8}	FO = 8 Routing Delay		7.1		8.1		9.2		10.9		15.2	ns
Logic Module Sequential Timing[2]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	4.3		5.0		5.6		6.6		9.2		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	4.3		5.0		5.6		6.6		9.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns

Clock signal to shift the Boundary Scan Test (BST) data into the device. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

TDI, I/OTest Data In

Serial data input for BST instructions and data. Data is shifted in on the rising edge of TCK. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

TDO, I/OTest Data Out

Serial data output for BST instructions and test data. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

TMS, I/OTest Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI and TDO pins are boundary scan pins. Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications. IEEE JTAG specification recommends a 10kΩ pull-up resistor on the pin. BST pins are only available in A42MX24 and A42MX36 devices.

VCC, Supply Voltage

Input supply voltage for 40MX devices

VCCA, Supply Voltage

Supply voltage for array in 42MX devices

VCCI, Supply Voltage

Supply voltage for I/Os in 42MX devices

WD, I/OWide Decode Output

When a wide decode module is used in a 42MX device this pin can be used as a dedicated output from the wide decode module. This direct connection eliminates additional interconnect delays associated with regular logic modules. To implement the direct I/O connection, connect an output buffer of any type to the output of the wide decode macro and place this output on one of the reserved WD pins.

4 Package Pin Assignments

The following figures and tables give the details of the package pin assignments.

Figure 38 • **PL44**


```
1 44

44-Pin
PLCC
```
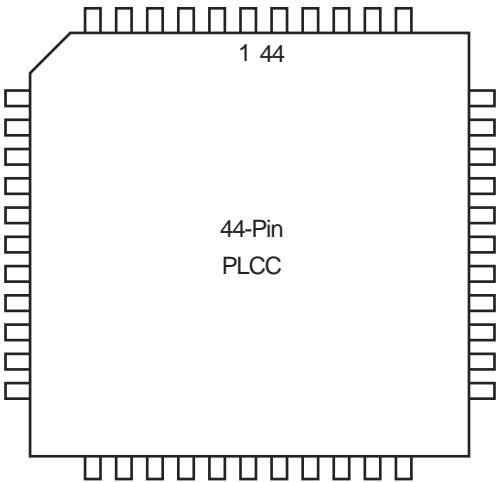
Table 47 • **PL44**

PL44		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
1	I/O	I/O
2	I/O	I/O
3	VCC	VCC
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	GND	GND
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	VCC	VCC
15	I/O	I/O
16	VCC	VCC
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O

Table 48 • **PL68**

PL68		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
24	I/O	I/O
25	VCC	VCC
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	VCC	VCC
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	GND	GND
50	I/O	I/O
51	I/O	I/O
52	CLK, I/O	CLK, I/O
53	I/O	I/O
54	MODE	MODE
55	VCC	VCC
56	SDI, I/O	SDI, I/O
57	DCLK, I/O	DCLK, I/O
58	PRA, I/O	PRA, I/O
59	PRB, I/O	PRB, I/O
60	I/O	I/O

Table 49 • **PL84**

PL84				
Pin Number	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
10	I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O
11	I/O	I/O	I/O	I/O
12	NC	MODE	MODE	MODE
13	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	I/O	I/O	I/O	I/O
18	GND	I/O	I/O	I/O
19	GND	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	VCCA	VCCI	VCCI
23	I/O	VCCI	VCCA	VCCA
24	I/O	I/O	I/O	I/O
25	VCC	I/O	I/O	I/O
26	VCC	I/O	I/O	I/O
27	I/O	I/O	I/O	I/O
28	I/O	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	I/O	I/O	I/O	I/O
31	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	VCC	I/O	I/O	I/O
34	I/O	I/O	I/O	TMS, I/O
35	I/O	I/O	I/O	TDI, I/O
36	I/O	I/O	I/O	WD, I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	WD, I/O
39	I/O	I/O	I/O	WD, I/O
40	GND	I/O	I/O	I/O
41	I/O	I/O	I/O	I/O
42	I/O	I/O	I/O	I/O
43	I/O	VCCA	VCCA	VCCA
44	I/O	I/O	I/O	WD, I/O
45	I/O	I/O	I/O	WD, I/O
46	VCC	I/O	I/O	WD, I/O

Table 49 •   **PL84**

PL84				
Pin Number	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
47	I/O	I/O	I/O	WD, I/O
48	I/O	I/O	I/O	I/O
49	I/O	GND	GND	GND
50	I/O	I/O	I/O	WD, I/O
51	I/O	I/O	I/O	WD, I/O
52	I/O	SDO, I/O	SDO, I/O	SDO, TDO, I/O
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	GND	I/O	I/O	I/O
61	GND	I/O	I/O	I/O
62	I/O	I/O	I/O	TCK, I/O
63	I/O	LP	LP	LP
64	CLK, I/O	VCCA	VCCA	VCCA
65	I/O	VCCI	VCCI	VCCI
66	MODE	I/O	I/O	I/O
67	VCC	I/O	I/O	I/O
68	VCC	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	GND	GND	GND
71	I/O	I/O	I/O	I/O
72	SDI, I/O	I/O	I/O	I/O
73	DCLK, I/O	I/O	I/O	I/O
74	PRA, I/O	I/O	I/O	I/O
75	PRB, I/O	I/O	I/O	I/O
76	I/O	SDI, I/O	SDI, I/O	SDI, I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	WD, I/O
79	I/O	I/O	I/O	WD, I/O
80	I/O	I/O	I/O	WD, I/O
81	I/O	PRA, I/O	PRA, I/O	PRA, I/O
82	GND	I/O	I/O	I/O
83	I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O

Table 51 • **PQ144**

PQ144	
Pin Number	**A42MX09 Function**
43	I/O
44	GNDQ
45	GNDI
46	NC
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	VCC
55	VCCI
56	NC
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	GND
65	GNDI
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	SDO
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	GNDQ

Table 58 • **CQ208**

CQ208	
Pin Number	**A42MX36 Function**
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	I/O
125	I/O
126	GND
127	I/O
128	TCK, I/O
129	LP
130	VCCA
131	GND
132	VCCI
133	VCCA
134	I/O
135	I/O
136	VCCA
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
T19	I/O
T20	I/O
U1	I/O
U2	I/O
U3	I/O
U4	I/O
U5	VCCI
U6	WD, I/O
U7	I/O
U8	I/O
U9	WD, I/O
U10	VCCA
U11	VCCI
U12	I/O
U13	I/O
U14	QCLKB, I/O
U15	I/O
U16	VCCI
U17	I/O
U18	GND
U19	I/O
U20	I/O
V1	I/O
V2	I/O
V3	GND
V4	GND
V5	I/O
V6	I/O
V7	I/O
V8	WD, I/O
V9	I/O
V10	I/O
V11	I/O
V12	I/O
V13	WD, I/O
V14	I/O
V15	WD, I/O