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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	72
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-plg84

Figure 8 • **Clock Networks of 42MX Devices**
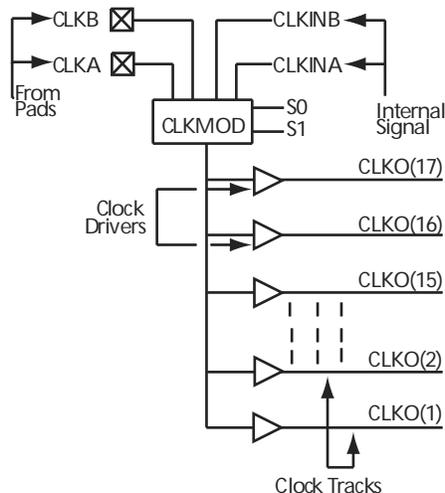
Figure 9 • **Quadrant Clock Network of A42MX36 Devices**
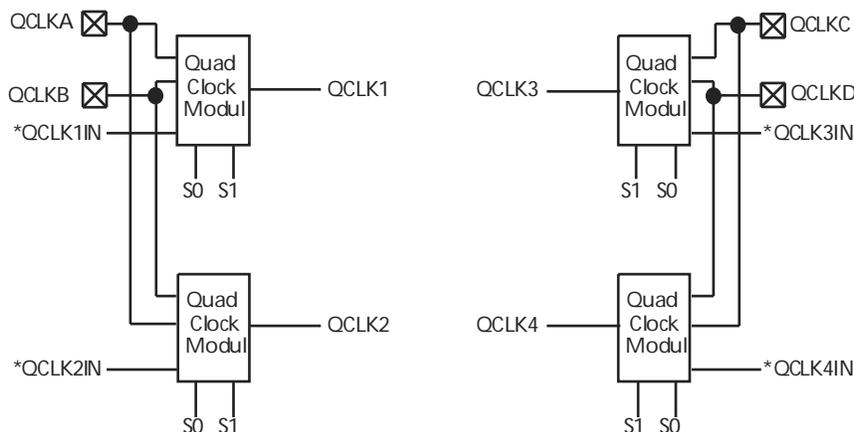
Note: *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

3.2.5   MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 10, page 12 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (See the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 10, page 12). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. See the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 μA.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 11, page 12). When the PCI fuse is not programmed, the output drive is standard.

3.8.1 3.3 V LVTTL Electrical Specifications

Table 19 • **3.3V LVTTL Electrical Specifications**

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH[1]	IOH = −4 mA	2.15		2.15		2.4		2.4		V
VOL[1]	IOL = 6 mA		0.4		0.4		0.48		0.48	V
VIL		−0.3	0.8	−0.3	0.8	−0.3	0.8	−0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX)		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL			−10		−10		−10		−10	µA
IIH			−10		−10		−10		−10	µA
Input Transition Time, T_R and T_F			500		500		500		500	ns
C_{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC[2]	A40MX02, A40MX04	3		25		10		25		mA
	A42MX09	5		25		25		25		mA
	A42MX16	6		25		25		25		mA
	A42MX24, A42MX36	15		25		25		25		mA
Low-Power Mode Standby Current	42MX devices only	0.5		ICC - 5.0		ICC - 5.0		ICC - 5.0		mA
IIO, I/O source sink current	Can be derived from the *IBIS model* (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCC/VCCI = min.
2. All outputs unloaded. All inputs = VCC/VCCI or GND.

3.9 Mixed 5.0 V / 3.3 V Operating Conditions (for 42MX Devices Only)

Table 20 • **Absolute Maximum Ratings***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	−0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	−0.5 to +7.0	V
VI	Input Voltage	−0.5 to VCCA +0.5	V
VO	Output Voltage	−0.5 to VCCI + 0.5	V
t_{STG}	Storage Temperature	−65 to +150	°C

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device

reliability. Devices should not be operated outside the recommended operating conditions.

Table 21 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCCA	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI	3.14 to 3.47	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

Table 35 • **A40MX02 Timing Characteristics (Nominal 3.3 V Operation)** *(continued)*
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
CMOS Output Module Timing[4]												
t_{DLH}	Data-to-Pad HIGH		5.5		6.4		7.2		8.5		11.9	ns
t_{DHL}	Data-to-Pad LOW		4.8		5.5		6.2		7.3		10.2	ns
t_{ENZH}	Enable Pad Z to HIGH		4.7		5.5		6.2		7.3		10.2	ns
t_{ENZL}	Enable Pad Z to LOW		6.8		7.9		8.9		10.5		14.7	ns
t_{ENHZ}	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9	ns
t_{ENLZ}	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7	ns
d_{TLH}	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro
4. Delays based on 35 pF loading

Table 36 • **A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions,**
VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
Logic Module Propagation Delays												
t_{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t_{PD2}	Dual-Module Macros		2.3		3.1		3.5		4.1		5.7	ns
t_{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays[1]												
t_{RD1}	FO = 1 Routing Delay		1.2		1.6		1.8		2.1		3.0	ns
t_{RD2}	FO = 2 Routing Delay		1.9		2.2		2.5		2.9		4.1	ns
t_{RD3}	FO = 3 Routing Delay		2.4		2.8		3.2		3.7		5.2	ns
t_{RD4}	FO = 4 Routing Delay		2.9		3.4		3.9		4.5		6.3	ns
t_{RD8}	FO = 8 Routing Delay		5.0		5.8		6.6		7.8		10.9	ns
Logic Module Sequential Timing[2]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	3.1		3.5		4.0		4.7		6.6		ns

Table 36 • **A40MX04 Timing Characteristics (Nominal 5.0 V Operation)** *(continued)*(**Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C)**

Parameter / Description		−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[1]												
t$_{DLH}$	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t$_{DHL}$	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t$_{ENZH}$	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t$_{ENZL}$	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t$_{ENLZ}$	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d$_{TLH}$	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d$_{THL}$	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer utility from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading

Table 37 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCC = 3.0 V, T$_J$ = 70°C)**

Parameter / Description		−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t$_{PD1}$	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t$_{PD2}$	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t$_{CO}$	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t$_{GO}$	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t$_{RS}$	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays[1]												
t$_{RD1}$	FO = 1 Routing Delay		1.9		2.2		2.5		3.0		4.2	ns
t$_{RD2}$	FO = 2 Routing Delay		2.7		3.1		3.5		4.1		5.7	ns
t$_{RD3}$	FO = 3 Routing Delay		3.4		3.9		4.4		5.2		7.3	ns
t$_{RD4}$	FO = 4 Routing Delay		4.1		4.8		5.4		6.3		8.9	ns
t$_{RD8}$	FO = 8 Routing Delay		7.1		8.1		9.2		10.9		15.2	ns
Logic Module Sequential Timing[2]												
t$_{SUD}$	Flip-Flop (Latch) Data Input Set-Up	4.3		5.0		5.6		6.6		9.2		ns
t$_{HD}$[3]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	4.3		5.0		5.6		6.6		9.2		ns
t$_{HENA}$	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns

Table 38 • **A42MX09 Timing Characteristics (Nominal 5.0 V Operation)** *(continued)***(Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing[5]												
t$_{DLH}$	Data-to-Pad HIGH		2.5		2.7		3.1		3.6		5.1	ns
t$_{DHL}$	Data-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t$_{ENZH}$	Enable Pad Z to HIGH		2.6		2.9		3.3		3.9		5.5	ns
t$_{ENZL}$	Enable Pad Z to LOW		2.9		3.2		3.7		4.3		6.1	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		4.9		5.4		6.2		7.3		10.2	ns
t$_{ENLZ}$	Enable Pad LOW to Z		5.3		5.9		6.7		7.9		11.1	ns
t$_{GLH}$	G-to-Pad HIGH		2.6		2.9		3.3		3.8		5.3	ns
t$_{GHL}$	G-to-Pad LOW		2.6		2.9		3.3		3.8		5.3	ns
t$_{LSU}$	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t$_{LH}$	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{LCO}$	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.2		5.8		6.6		7.7		10.8	ns
t$_{ACO}$	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.4		8.2		9.3		10.9		15.3	ns
d$_{TLH}$	Capacity Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF
d$_{THL}$	Capacity Loading, HIGH to LOW		0.04		0.04		0.04		0.05		0.07	ns/pF

Table 39 • **A42MX09 Timing Characteristics (Nominal 3.3 V Operation)** *(continued)***(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{RD4}$	FO = 4 Routing Delay		1.9		2.1		2.4		2.9		4.0	ns
t$_{RD8}$	FO = 8 Routing Delay		3.2		3.6		4.1		4.8		6.7	ns
Logic Module Sequential Timing [3, 4]												
t$_{SUD}$	Flip-Flop (Latch) Data Input Set-Up	0.5		0.5		0.6		0.7		0.9		ns
t$_{HD}$	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t$_{HENA}$	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	4.7		5.3		6.0		7.0		9.8		ns
t$_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	6.2		6.9		7.8		9.2		12.9		ns
t$_A$	Flip-Flop Clock Input Period	5.0		5.6		6.2		7.1		9.9		ns
t$_{INH}$	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
t$_{OUTH}$	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{OUTSU}$	Output Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
f$_{MAX}$	Flip-Flop (Latch) Clock Frequency		161		146		135		117		70	MHz

Table 41 • **A42MX16 Timing Characteristics (Nominal 3.3 V Operation)** *(continued)***(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)**

Parameter / Description		−3 Speed Min.	−3 Speed Max.	−2 Speed Min.	−2 Speed Max.	−1 Speed Min.	−1 Speed Max.	Std Speed Min.	Std Speed Max.	−F Speed Min.	−F Speed Max.	Units
t$_{ACO}$	Array Clock-to-Out (Pad-to-Pad),64 Clock Loading		11.3		12.5		14.2		16.7		23.3	ns
d$_{TLH}$	Capacitive Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{THL}$	Capacitive Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

1. For dual-module macros use tPD1 + tRD1 + taped, to + tRD1 + taped, or tPD1 + tRD1 + tusk, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing ansalysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 42 • **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)**

Parameter / Description		−3 Speed Min.	−3 Speed Max.	−2 Speed Min.	−2 Speed Max.	−1 Speed Min.	−1 Speed Max.	Std Speed Min.	Std Speed Max.	−F Speed Min.	−F Speed Max.	Units
Logic Module Combinatorial Functions[1]												
t$_{PD}$	Internal Array Module Delay		1.2		1.3		1.5		1.8		2.5	ns
t$_{PDD}$	Internal Decode Module Delay		1.4		1.6		1.8		2.1		3.0	ns
Logic Module Predicted Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		0.8		0.9		1.0		1.2		1.7	ns
t$_{RD2}$	FO = 2 Routing Delay		1.0		1.2		1.3		1.5		2.1	ns
t$_{RD3}$	FO = 3 Routing Delay		1.3		1.4		1.6		1.9		2.6	ns
t$_{RD4}$	FO = 4 Routing Delay		1.5		1.7		1.9		2.2		3.1	ns
t$_{RD5}$	FO = 8 Routing Delay		2.4		2.7		3.0		3.6		5.0	ns
Logic Module Sequential Timing[3, 4]												
t$_{CO}$	Flip-Flop Clock-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t$_{GO}$	Latch Gate-to-Output		1.2		1.3		1.5		1.8		2.5	ns
t$_{SUD}$	Flip-Flop (Latch) Set-Up Time	0.3		0.4		0.4		0.5		0.7		ns
t$_{HD}$	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t$_{RO}$	Flip-Flop (Latch) Reset-to-Output		1.4		1.6		1.8		2.1		2.9	ns
t$_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	0.4		0.5		0.5		0.6		0.8		ns
t$_{HENA}$	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t$_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.3		6.5		9.0		ns

Table 42 • **A42MX24 Timing Characteristics (Nominal 5.0 V Operation)** *(continued)***(Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays[2]													
t$_{IRD1}$	FO = 1 Routing Delay			1.8		2.0		2.3		2.7		3.8	ns
t$_{IRD2}$	FO = 2 Routing Delay			2.1		2.3		2.6		3.1		4.3	ns
t$_{IRD3}$	FO = 3 Routing Delay			2.3		2.5		2.9		3.4		4.8	ns
t$_{IRD4}$	FO = 4 Routing Delay			2.5		2.8		3.2		3.7		5.2	ns
t$_{IRD8}$	FO = 8 Routing Delay			3.4		3.8		4.3		5.1		7.1	ns
Global Clock Network													
t$_{CKH}$	Input LOW to HIGH	FO = 32		2.6		2.9		3.3		3.9		5.4	ns
		FO = 486		2.9		3.2		3.6		4.3		5.9	ns
t$_{CKL}$	Input HIGH to LOW	FO = 32		3.7		4.1		4.6		5.4		7.6	ns
		FO = 486		4.3		4.7		5.4		6.3		8.8	ns
t$_{PWH}$	Minimum Pulse Width HIGH	FO = 32	2.2		2.4		2.7		3.2		4.5		ns
		FO = 486	2.4		2.6		3.0		3.5		4.9		ns
t$_{PWL}$	Minimum Pulse Width LOW	FO = 32	2.2		2.4		2.7		3.2		4.5		ns
		FO = 486	2.4		2.6		3.0		3.5		4.9		ns
t$_{CKSW}$	Maximum Skew	FO = 32		0.5		0.6		0.7		0.8		1.1	ns
		FO = 486		0.5		0.6		0.7		0.8		1.1	ns
t$_{SUEXT}$	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 486	0.0		0.0		0.0		0.0		0.0		ns
t$_{HEXT}$	Input Latch External Hold	FO = 32	2.8		3.1		3.5		4.1		5.7		ns
		FO = 486	3.3		3.7		4.2		4.9		6.9		ns
t$_P$	Minimum Period (1/f$_{MAX}$)	FO = 32	4.7		5.2		5.7		6.5		10.9		ns
		FO = 486	5.1		5.7		6.2		7.1		11.9		ns

Table 43 • **A42MX24 Timing Characteristics (Nominal 3.3 V Operation)** *(continued)***(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)**

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
TTL Output Module Timing[5] (continued)												
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.7		8.5		9.6		11.3		15.9	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		14.8		16.5		18.7		22.0		30.8	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.04		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		4.8		5.3		5.5		6.4		9.0	ns
t_{DHL}	Data-to-Pad LOW		3.5		3.9		4.1		4.9		6.8	ns
t_{ENZH}	Enable Pad Z to HIGH		3.6		4.0		4.5		5.3		7.4	ns
t_{ENZL}	Enable Pad Z to LOW		3.4		4.0		5.0		5.8		8.2	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.2		8.0		9.0		10.7		14.9	ns
t_{ENLZ}	Enable Pad LOW to Z		6.7		7.5		8.5		9.9		13.9	ns
t_{GLH}	G-to-Pad HIGH		6.8		7.6		8.6		10.1		14.2	ns
t_{GHL}	G-to-Pad LOW		6.8		7.6		8.6		10.1		14.2	ns
t_{LSU}	I/O Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.7		8.5		9.6		11.3		15.9	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		14.8		16.5		18.7		22.0		30.8	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.04		0.04		0.05		0.06		0.08	ns/pF
t_{HEXT}	Input Latch External Hold — FO = 32	3.9		4.3		4.9		5.7		8.1		ns
	FO = 486	4.6		5.2		5.8		6.9		9.6		ns
t_P	Minimum Period (1/f$_{MAX}$) — FO = 32	7.8		8.7		9.5		10.8		18.2		ns
	FO = 486	8.6		9.5		10.4		11.9		19.9		ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 44 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		3.5		3.9		4.5		5.2		7.3	ns
t_{DHL}	Data-to-Pad LOW		2.5		2.7		3.1		3.6		5.1	ns
t_{ENZH}	Enable Pad Z to HIGH		2.7		3.0		3.3		3.9		5.5	ns
t_{ENZL}	Enable Pad Z to LOW		2.9		3.3		3.7		4.3		6.1	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.3		5.8		6.6		7.8		10.9	ns
t_{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t_{GLH}	G-to-Pad HIGH		5.0		5.6		6.3		7.5		10.4	ns
t_{GHL}	G-to-Pad LOW		5.0		5.6		6.3		7.5		10.4	ns
t_{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 45 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
Logic Module Combinatorial Functions[1]												
t_{PD}	Internal Array Module Delay		1.9		2.1		2.3		2.7		3.8	ns
t_{PDD}	Internal Decode Module Delay		2.2		2.5		2.8		3.3		4.7	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.7	ns
t_{RD2}	FO = 2 Routing Delay		1.8		2.0		2.3		2.7		3.7	ns
t_{RD3}	FO = 3 Routing Delay		2.3		2.5		2.8		3.4		4.7	ns
t_{RD4}	FO = 4 Routing Delay		2.8		3.1		3.5		4.1		5.7	ns

Table 45 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation)** *(continued)***(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)**

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
Synchronous SRAM Operations (continued)												
t$_{ADH}$	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t$_{RENSU}$	Read Enable Set-Up	0.9		1.0		1.1		1.3		1.8		ns
t$_{RENH}$	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t$_{WENSU}$	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t$_{WENH}$	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{BENS}$	Block Enable Set-Up	3.9		4.3		4.9		5.7		8.0		ns
t$_{BENH}$	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations												
t$_{RPD}$	Asynchronous Access Time		11.3		12.6		14.3		16.8		23.5	ns
t$_{RDADV}$	Read Address Valid	12.3		13.7		15.5		18.2		25.5		ns
t$_{ADSU}$	Address/Data Set-Up Time	2.3		2.5		2.8		3.4		4.8		ns
t$_{ADH}$	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t$_{RENSUA}$	Read Enable Set-Up to Address Valid	0.9		1.0		1.1		1.3		1.8		ns
t$_{RENHA}$	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t$_{WENSU}$	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t$_{WENH}$	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{DOH}$	Data Out Hold Time		1.8		2.0		2.1		2.5		3.5	ns
Input Module Propagation Delays												
t$_{INPY}$	Input Data Pad-to-Y		1.4		1.6		1.8		2.1		3.0	ns
t$_{INGO}$	Input Latch Gate-to-Output		2.0		2.2		2.5		2.9		4.1	ns
t$_{INH}$	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t$_{ILA}$	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

4 Package Pin Assignments

The following figures and tables give the details of the package pin assignments.

Figure 38 • **PL44**
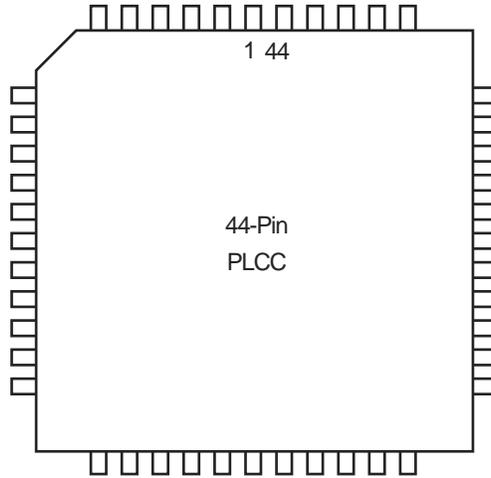
Table 47 • **PL44**

PL44		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
1	I/O	I/O
2	I/O	I/O
3	VCC	VCC
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	GND	GND
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	VCC	VCC
15	I/O	I/O
16	VCC	VCC
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O

Table 49 • **PL84**

PL84

Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
84	I/O	VCCA	VCCA	VCCA

Figure 41 • **PQ100**
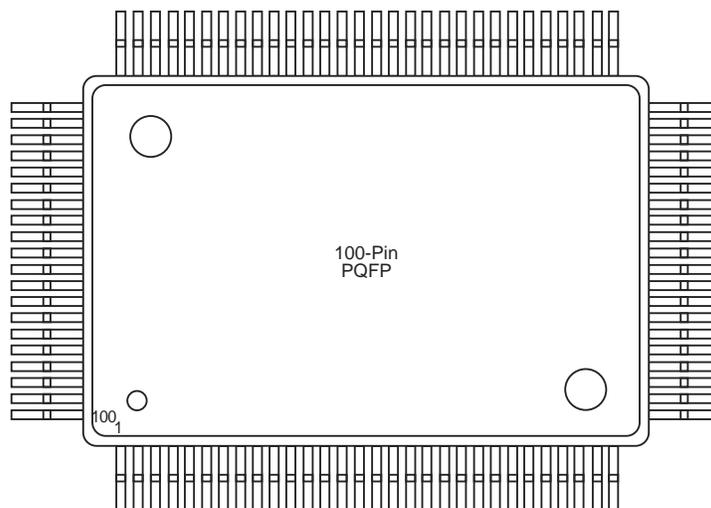
Table 50 • **PQ 100**

PQ100

Pin Number	A40MX02 Function	A40MX04 Function	A42MX09 Function	A42MX16 Function
1	NC	NC	I/O	I/O
2	NC	NC	DCLK, I/O	DCLK, I/O
3	NC	NC	I/O	I/O
4	NC	NC	MODE	MODE
5	NC	NC	I/O	I/O
6	PRB, I/O	PRB, I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	GND	GND
10	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O
13	GND	GND	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	VCCA	VCCA
17	I/O	I/O	VCCI	VCCA
18	I/O	I/O	I/O	I/O

Table 54 • **PQ240**

PQ240

Pin Number	A42MX36 Function
15	QCLKC, I/O
16	I/O
17	WD, I/O
18	WD, I/O
19	I/O
20	I/O
21	WD, I/O
22	WD, I/O
23	I/O
24	PRB, I/O
25	I/O
26	CLKB, I/O
27	I/O
28	GND
29	VCCA
30	VCCI
31	I/O
32	CLKA, I/O
33	I/O
34	PRA, I/O
35	I/O
36	I/O
37	WD, I/O
38	WD, I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	QCLKD, I/O
46	I/O
47	WD, I/O
48	WD, I/O
49	I/O
50	I/O
51	I/O

Table 56 • **VQ100**

VQ100		
Pin Number	**A42MX09 Function**	**A42MX16 Function**
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	VCCA	VCCA
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	GND	GND
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	SDO, I/O	SDO, I/O
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	GND	GND
56	I/O	I/O

Table 57 • **TQ176**

TQ176

Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
158	CLKB, I/O	CLKB, I/O	CLKB, I/O
159	I/O	I/O	I/O
160	PRB, I/O	PRB, I/O	PRB, I/O
161	NC	I/O	WD, I/O
162	I/O	I/O	WD, I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	NC	NC	WD, I/O
166	NC	I/O	WD, I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	I/O	I/O	I/O
170	NC	VCCI	VCCI
171	I/O	I/O	WD, I/O
172	I/O	I/O	WD, I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	DCLK, I/O	DCLK, I/O	DCLK, I/O
176	I/O	I/O	I/O

Figure 49 • **CQ208**
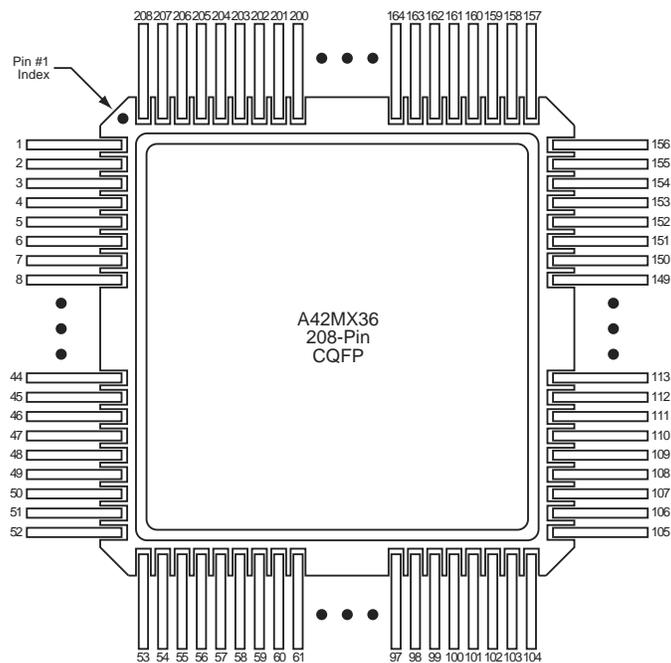
Table 61 • **PG132**

PG132	
Pin Number	**A42MX09 Function**
N10	I/O
M10	I/O
N11	I/O
L10	I/O
M11	I/O
N12	SDO
M12	I/O
L11	I/O
N13	I/O
M13	I/O
K11	I/O
L12	I/O
L13	I/O
K13	I/O
H10	I/O
J12	I/O
J13	I/O
H11	I/O
H12	I/O
H13	VKS
G13	VPP

Figure 53 • **CQ172**

Table 62 • **CQ172**

CQ172	
Pin Number	**A42MX16 Function**
1	MODE
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	GND
8	I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	I/O
17	GND
18	I/O
19	I/O
20	I/O