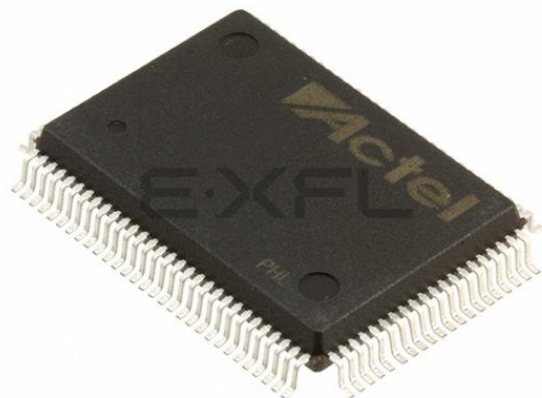




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

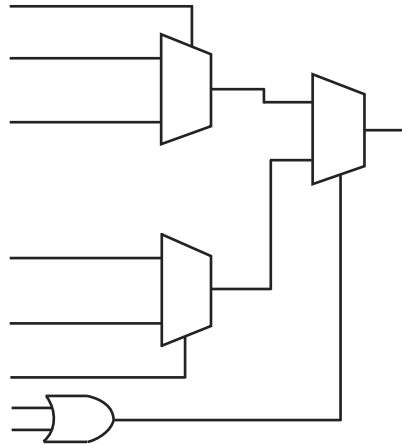
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	83
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-pqg100

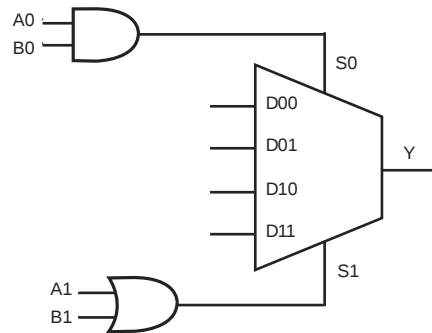
	VCCA = 3.0 V, T _J = 70°C)	79
Table 46	Configuration of Unused I/Os	84
Table 47	PL44	86
Table 48	PL68	88
Table 49	PL84	90
Table 50	PQ 100	93
Table 51	PQ144	97
Table 52	PQ160	102
Table 53	PQ208	107
Table 54	PQ240	113
Table 55	VQ80	120
Table 56	VQ100	123
Table 57	TQ176	126
Table 58	CQ208	132
Table 59	CQ256	138
Table 60	BG272	145
Table 61	PG132	153
Table 62	CQ172	158

Figure 2 • 42MX C-Module Implementation



The 42MX devices contain three types of logic modules: combinatorial (C-modules), sequential (S-modules) and decode (D-modules). The following figure illustrates the combinatorial logic module. The S-module, shown in Figure 4, page 8, implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D-flip-flop or a transparent latch. The S-module register can be bypassed so that it implements purely combinatorial logic.

Figure 3 • 42MX C-Module Implementation



Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 14 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCA (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V

Note: * Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

3.7.1 5 V TTL Electrical Specifications

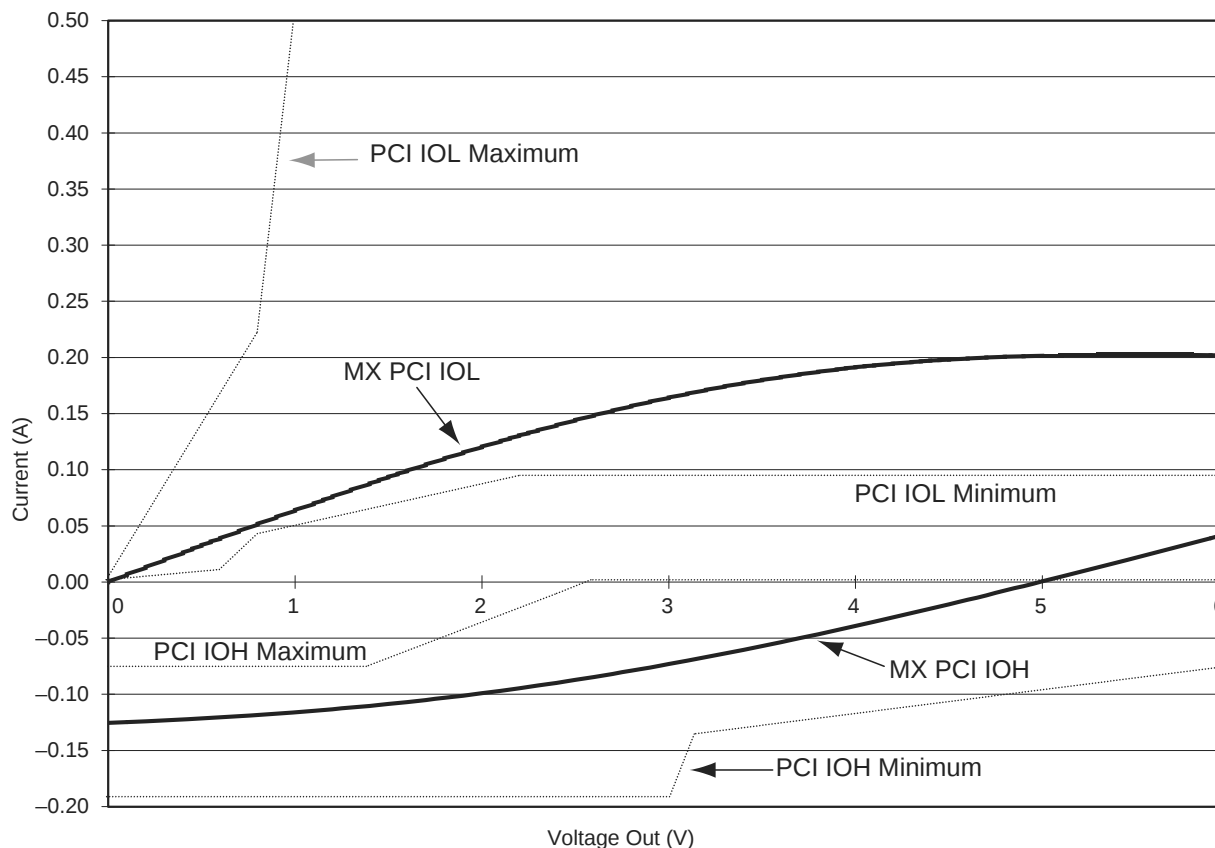
The following tables show 5 V TTL electrical specifications.

Table 15 • 5V TTL Electrical Specifications

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	IOH = –10 mA	2.4		2.4						V
	IOH = –4 mA					3.7		3.7		V
VOL ¹	IOL = 10 mA		0.5		0.5					V
	IOL = 6 mA					0.4		0.4		V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX) ²		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL	VIN = 0.5 V		–10		–10		–10		–10	μA
IIH	VIN = 2.7 V		–10		–10		–10		–10	μA
Input Transition Time, T_R and T_F			500		500		500		500	ns
C _{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC ³	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		20		25		25		25	mA
Low power mode Standby Current	42MX devices only		0.5		ICC – 5.0		ICC – 5.0		ICC – 5.0	mA
IIO, I/O source sink current	Can be derived from the <i>IBIS model</i> (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCC/VCCI = min

2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

Figure 16 • Typical Output Drive Characteristics (Based Upon Measured Data)

3.9.4 Junction Temperature (T_J)

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a(1)$$

EQ 4

where:

- T_a = Ambient Temperature
- ΔT = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$ (2)
- P = Power
- θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in Table 27, page 29.

3.9.5 Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc} , and the junction-to-ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates.

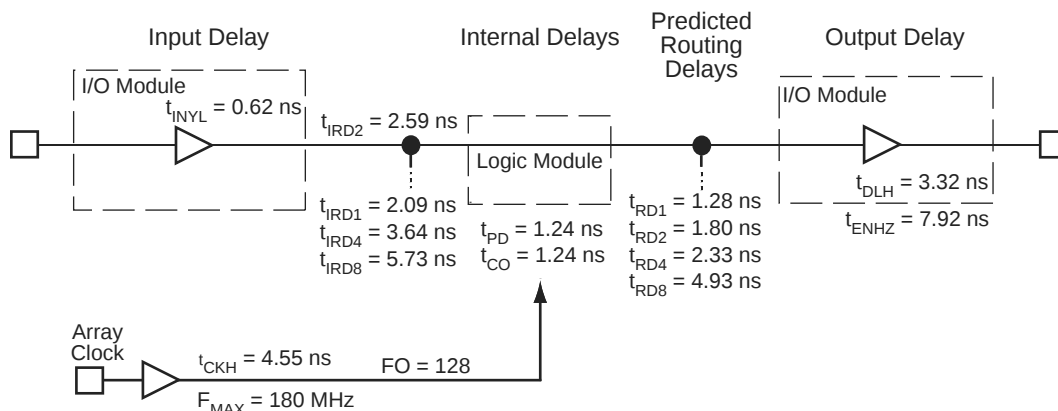
The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of θ_{ja} .

3.10 Timing Models

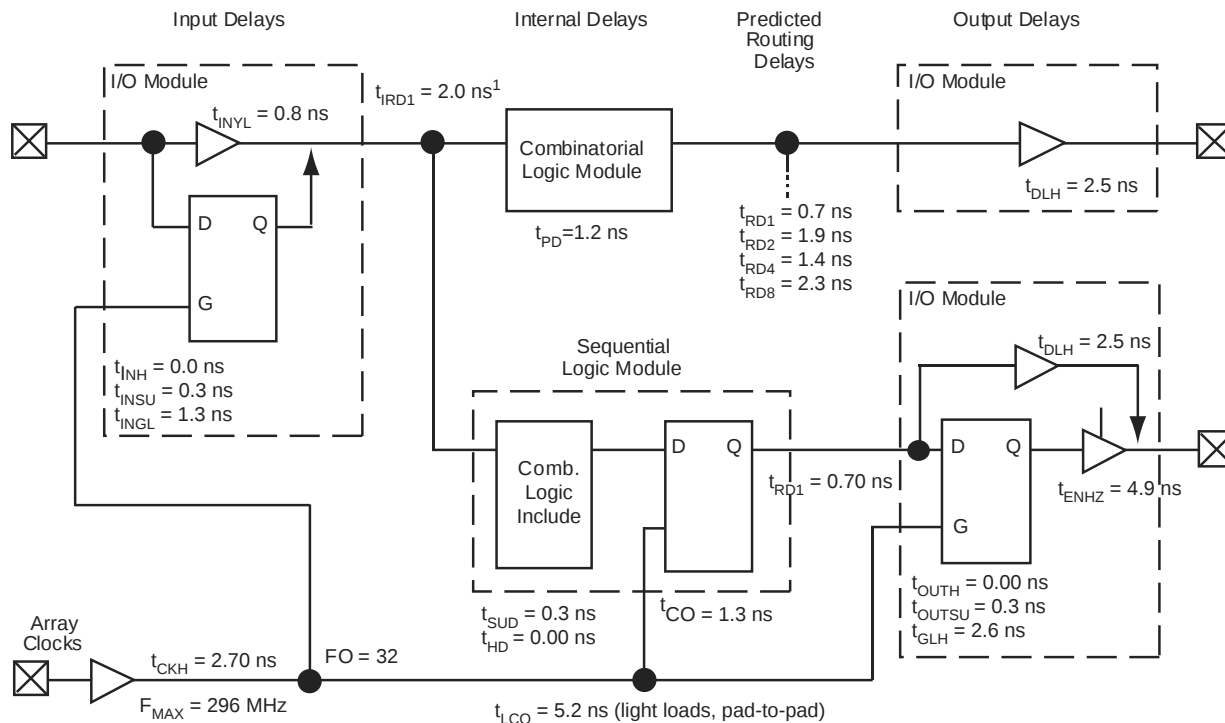
The following figures show various timing models.

Figure 17 • 40MX Timing Model*



Note: Values are shown for 40MX –3 speed devices at 5.0 V worst-case commercial conditions.

Figure 18 • 42MX Timing Model



Note: 1. Input module predicted routing delay

Note: 2. Values are shown for A42MX09 –3 at 5.0 V worst-case commercial conditions.

Table 33 • Timing Parameters for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{SU(PTP)}$	Input Set-Up Time to CLK—Point-to-Point	10, 12 ²	—	1.5	—	1.5	—	ns
t_H	Input Hold to CLK	0	—	0	—	0	—	ns

1. TOFF is system dependent. MX PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.
2. REQ# and GNT# are point-to-point signals and have different output valid delay and input setup times than do bussed signals. GNT# has a setup of 10; REW# has a setup of 12.

3.11.6.1 Timing Characteristics

The following tables list the timing characteristics.

Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation)
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t _{PD2}	Dual-Module Macros		2.7		3.1		3.5		4.1		5.7	ns
t _{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays ¹												
t _{RD1}	FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.8	ns
t _{RD2}	FO = 2 Routing Delay		1.8		2.1		2.4		2.8		3.9	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.7		3.0		3.6		5.0	ns
t _{RD4}	FO = 4 Routing Delay		2.9		3.3		3.7		4.4		6.1	ns
t _{RD8}	FO = 8 Routing Delay		4.9		5.7		6.5		7.6		10.6	ns
Logic Module Sequential Timing ²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t _A	Flip-Flop Clock Input Period	4.8		5.6		6.3		7.5		10.4		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		181		168		154		134		80	MHz

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _p	Minimum Period	FO = 16	6.5		7.5		8.5		10.1		14.1		ns
		FO = 128	6.8		7.8		8.9		10.4		14.6		
f _{MAX}	Maximum Frequency	FO = 16		113		105		96		83		50	MHz
		FO = 128		109		101		92		80		48	
TTL Output Module Timing ⁴													
t _{DLH}	Data-to-Pad HIGH			4.7		5.4		6.1		7.2		10.0	ns
t _{DHL}	Data-to-Pad LOW			5.6		6.4		7.3		8.6		12.0	ns
t _{ENZH}	Enable Pad Z to HIGH			5.2		6.0		6.8		8.1		11.3	ns
t _{ENZL}	Enable Pad Z to LOW			6.6		7.6		8.6		10.1		14.1	ns
t _{ENHZ}	Enable Pad HIGH to Z			11.1		12.8		14.5		17.1		23.9	ns
t _{ENLZ}	Enable Pad LOW to Z			8.2		9.5		10.7		12.6		17.7	ns
d _{TLH}	Delta LOW to HIGH			0.03		0.03		0.04		0.04		0.06	ns/pF
d _{THL}	Delta HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		3.3		3.8		4.3		5.0		7.0		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		3.3		3.8		4.3		5.0		7.0		ns
t _A	Flip-Flop Clock Input Period		4.8		5.6		6.3		7.5		10.4		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)			181		167		154		134		80	MHz
Input Module Propagation Delays													
t _{INyh}	Pad-to-Y HIGH			0.7		0.8		0.9		1.1		1.5	ns
t _{INyl}	Pad-to-Y LOW			0.6		0.7		0.8		1.0		1.3	ns
Input Module Predicted Routing Delays ¹													
t _{IRD1}	FO = 1 Routing Delay			2.1		2.4		2.2		3.2		4.5	ns
t _{IRD2}	FO = 2 Routing Delay			2.6		3.0		3.4		4.0		5.6	ns
t _{IRD3}	FO = 3 Routing Delay			3.1		3.6		4.1		4.8		6.7	ns
t _{IRD4}	FO = 4 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t _{IRD8}	FO = 8 Routing Delay			5.7		6.6		7.5		8.8		12.4	ns
Global Clock Network													
t _{CKH}	Input Low to HIGH	FO = 16		4.6		5.3		6.0		7.0		9.8	ns
		FO = 128		4.6		5.3		6.0		7.0		9.8	
t _{CKL}	Input High to LOW	FO = 16		4.8		5.6		6.3		7.4		10.4	ns
		FO = 128		4.8		5.6		6.3		7.4		10.4	
t _{PWH}	Minimum Pulse Width HIGH	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.1		3.6		5.1		
t _{PWL}	Minimum Pulse Width LOW	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.01		3.6		5.1		
t _{CKSW}	Maximum Skew	FO = 16		0.4		0.5		0.5		0.6		0.8	ns
		FO = 128		0.5		0.6		0.7		0.8		1.2	
t _P	Minimum Period	FO = 16	4.7		5.4		6.1		7.2		10.0		ns
		FO = 128	4.8		5.6		6.3		7.5		10.4		
f _{MAX}	Maximum Frequency	FO = 16		188		175		160		139		83	MHz
		FO = 128		181		168		154		134		80	
TTL Output Module Timing ⁴													
t _{DLH}	Data-to-Pad HIGH			3.3		3.8		4.3		5.1		7.2	ns
t _{DHL}	Data-to-Pad LOW			4.0		4.6		5.2		6.1		8.6	ns
t _{ENZH}	Enable Pad Z to HIGH			3.7		4.3		4.9		5.8		8.0	ns
t _{ENZL}	Enable Pad Z to LOW			4.7		5.4		6.1		7.2		10.1	ns
t _{ENHZ}	Enable Pad HIGH to Z			7.9		9.1		10.4		12.2		17.1	ns

Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t _{INYH}	Pad-to-Y HIGH			1.0		1.2		1.3		1.6		2.2	ns
t _{INYL}	Pad-to-Y LOW			0.8		0.9		1.0		1.2		1.7	ns
t _{INGH}	G to Y HIGH			1.3		1.4		1.6		1.9		2.7	ns
t _{INGL}	G to Y LOW			1.3		1.4		1.6		1.9		2.7	ns
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay			2.0		2.2		2.5		3.0		4.2	ns
t _{IRD2}	FO = 2 Routing Delay			2.3		2.5		2.9		3.4		4.7	ns
t _{IRD3}	FO = 3 Routing Delay			2.5		2.8		3.2		3.7		5.2	ns
t _{IRD4}	FO = 4 Routing Delay			2.8		3.1		3.5		4.1		5.7	ns
t _{IRD8}	FO = 8 Routing Delay			3.7		4.1		4.7		5.5		7.7	ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32		2.4		2.7		3.0		3.6		5.0	ns
		FO = 256		2.7		3.0		3.4		4.0		5.5	ns
t _{CKL}	Input HIGH to LOW	FO = 32		3.5		3.9		4.4		5.2		7.3	ns
		FO = 256		3.9		4.3		4.9		5.7		8.0	ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t _{CKSW}	Maximum Skew	FO = 32		0.3		0.3		0.4		0.5		0.6	ns
		FO = 256		0.3		0.3		0.4		0.5		0.6	ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	2.3		2.6		3.0		3.5		4.9		ns
		FO = 256	2.2		2.4		3.3		3.9		5.5		ns
t _P	Minimum Period	FO = 32	3.4		3.7		4.0		4.7		7.8		ns
		FO = 256	3.7		4.1		4.5		5.2		8.6		ns
f _{MAX}	Maximum Frequency	FO = 32		296		269		247		215		129	MHz
		FO = 256		268		244		224		195		117	MHz

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PWL}	Minimum Pulse Width LOW	FO = 32	3.2		3.5		4.0		4.7		6.6		ns
		FO = 384	3.7		4.1		4.6		5.4		7.6		ns
t _{CKSW}	Maximum Skew	FO = 32		0.3		0.4		0.4		0.5		0.7	ns
		FO = 384		0.3		0.4		0.4		0.5		0.7	ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 384	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	2.8		3.1		5.5		4.1		5.7		ns
		FO = 384	3.2		3.5		4.0		4.7		6.6		ns
t _P	Minimum Period	FO = 32	4.2		4.67		5.1		5.8		9.7		ns
		FO = 384	4.6		5.1		5.6		6.4		10.7		ns
f _{MAX}	Maximum Frequency	FO = 32		237		215		198		172		103	MHz
		FO = 384		215		195		179		156		94	MHz

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH	2.5		2.8		3.2		3.7		5.2		ns
t _{DHL}	Data-to-Pad LOW	3.0		3.3		3.7		4.4		6.1		ns
t _{ENZH}	Enable Pad Z to HIGH	2.7		3.0		3.4		4.0		5.6		ns
t _{ENZL}	Enable Pad Z to LOW	3.0		3.3		3.8		4.4		6.2		ns
t _{ENHZ}	Enable Pad HIGH to Z	5.4		6.0		6.8		8.0		11.2		ns
t _{ENLZ}	Enable Pad LOW to Z	5.0		5.6		6.3		7.4		10.4		ns
t _{GLH}	G-to-Pad HIGH	2.9		3.2		3.6		4.3		6.0		ns
t _{GHL}	G-to-Pad LOW	2.9		3.2		3.6		4.3		6.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading	5.7		6.3		7.1		8.4		11.9		ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading	8.0		8.9		10.1		11.9		16.7		ns
d _{TLH}	Capacitive Loading, LOW to HIGH	0.03		0.03		0.03		0.04		0.06		ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW	0.04		0.04		0.04		0.05		0.07		ns/pF

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		2.4		2.7		3.1		3.6		5.1	ns
t _{DHL}	Data-to-Pad LOW		2.8		3.2		3.6		4.2		5.9	ns
t _{ENZH}	Enable Pad Z to HIGH		2.5		2.8		3.2		3.8		5.3	ns
t _{ENZL}	Enable Pad Z to LOW		2.8		3.1		3.5		4.2		5.9	ns
t _{ENHZ}	Enable Pad HIGH to Z		5.2		5.7		6.5		7.6		10.7	ns
t _{ENLZ}	Enable Pad LOW to Z		4.8		5.3		6.0		7.1		9.9	ns
t _{GLH}	G-to-Pad HIGH		2.9		3.2		3.6		4.3		6.0	ns
t _{GHL}	G-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t _{LSU}	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.6		6.1		6.9		8.1		11.4	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.6		11.8		13.4		15.7		22.0	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay		2.6		2.9		3.2		3.8		5.3		ns
t _{IRD2}	FO = 2 Routing Delay		2.9		3.2		3.6		4.3		6.0		ns
t _{IRD3}	FO = 3 Routing Delay		3.2		3.6		4.0		4.8		6.6		ns
t _{IRD4}	FO = 4 Routing Delay		3.5		3.9		4.4		5.2		7.3		ns
t _{IRD8}	FO = 8 Routing Delay		4.8		5.3		6.1		7.1		10.0		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32	4.4		4.8		5.5		6.5		9.1		ns
		FO = 486	4.8		5.3		6.0		7.1		10.0		ns
t _{CKL}	Input HIGH to LOW	FO = 32	5.1		5.7		6.4		7.6		10.6		ns
		FO = 486	6.0		6.6		7.5		8.8		12.4		ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	3.0		3.3		3.8		4.5		6.3		ns
		FO = 486	3.3		3.7		4.2		4.9		6.9		ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	3.0		3.4		3.8		4.5		6.3		ns
		FO = 486	3.3		3.7		4.2		4.9		6.9		ns
t _{CKSW}	Maximum Skew	FO = 32	0.8		0.8		1.0		1.1		1.6		ns
		FO = 486	0.8		0.8		1.0		1.1		1.6		ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 486	0.0		0.0		0.0		0.0		0.0		ns
TTL Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH		3.4		3.8		4.3		5.0		7.1		ns
t _{DHL}	Data-to-Pad LOW		4.0		4.4		5.0		5.9		8.3		ns
t _{ENZH}	Enable Pad Z to HIGH		3.6		4.0		4.5		5.3		7.4		ns
t _{ENZL}	Enable Pad Z to LOW		3.9		4.4		5.0		5.8		8.2		ns
t _{ENHZ}	Enable Pad HIGH to Z		7.2		8.0		9.1		10.7		14.9		ns
t _{ENLZ}	Enable Pad LOW to Z		6.7		7.5		8.5		9.9		13.9		ns
t _{GLH}	G-to-Pad HIGH		4.8		5.3		6.0		7.2		10.0		ns
t _{GHL}	G-to-Pad LOW		4.8		5.3		6.0		7.2		10.0		ns
t _{LSU}	I/O Latch Output Set-Up		0.7		0.7		0.8		1.0		1.4		ns

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵ (continued)													
t _{LH}	I/O Latch Output Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d _{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH			4.8		5.3		5.5		6.4		9.0	ns
t _{DHL}	Data-to-Pad LOW			3.5		3.9		4.1		4.9		6.8	ns
t _{ENZH}	Enable Pad Z to HIGH			3.6		4.0		4.5		5.3		7.4	ns
t _{ENZL}	Enable Pad Z to LOW			3.4		4.0		5.0		5.8		8.2	ns
t _{ENHZ}	Enable Pad HIGH to Z			7.2		8.0		9.0		10.7		14.9	ns
t _{ENLZ}	Enable Pad LOW to Z			6.7		7.5		8.5		9.9		13.9	ns
t _{GLH}	G-to-Pad HIGH			6.8		7.6		8.6		10.1		14.2	ns
t _{GHL}	G-to-Pad LOW			6.8		7.6		8.6		10.1		14.2	ns
t _{LSU}	I/O Latch Set-Up		0.7		0.7		0.8		1.0		1.4		ns
t _{LH}	I/O Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d _{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
t _{HEXT}	Input Latch External Hold	FO = 32	3.9		4.3		4.9		5.7		8.1		ns
		FO = 486	4.6		5.2		5.8		6.9		9.6		ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	7.8		8.7		9.5		10.8		18.2		ns
		FO = 486	8.6		9.5		10.4		11.9		19.9		ns

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions ¹												
t _{PD}	Internal Array Module Delay		1.3		1.5		1.7		2.0		2.7	ns
t _{PDD}	Internal Decode Module Delay		1.6		1.8		2.0		2.4		3.3	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.2		1.4		2.0	ns
t _{RD2}	FO = 2 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t _{RD3}	FO =3 Routing Delay		1.6		1.8		2.0		2.4		3.4	ns
t _{RD4}	FO = 4 Routing Delay		2.0		2.2		2.5		2.9		4.1	ns
t _{RD5}	FO = 8 Routing Delay		3.3		3.7		4.2		4.9		6.9	ns
t _{RDD}	Decode-to-Output Routing Delay		0.3		0.4		0.4		0.5		0.7	ns
Logic Module Sequential Timing ^{3, 4}												
t _{CO}	Flip-Flop Clock-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t _{GO}	Latch Gate-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t _{SUD}	Flip-Flop (Latch) Set-Up Time	0.3		0.3		0.4		0.5		0.7		ns
t _{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RO}	Flip-Flop (Latch) Reset-to-Output		1.6		1.7		2.0		2.3		3.2	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.5		6.4		9.0		ns
Synchronous SRAM Operations												
t _{RC}	Read Cycle Time		6.8		7.5		8.5		10.0		14.0	ns
t _{WC}	Write Cycle Time		6.8		7.5		8.5		10.0		14.0	ns
t _{RCKHL}	Clock HIGH/LOW Time		3.4		3.8		4.3		5.0		7.0	ns
t _{RCO}	Data Valid After Clock HIGH/LOW		3.4		3.8		4.3		5.0		7.0	ns
t _{ADSU}	Address/Data Set-Up Time		1.6		1.8		2.0		2.4		3.4	ns
Synchronous SRAM Operations (continued)												
t _{ADH}	Address/Data Hold Time		0.0		0.0		0.0		0.0		0.0	ns
t _{RENSU}	Read Enable Set-Up		0.6		0.7		0.8		0.9		1.3	ns
t _{RENH}	Read Enable Hold		3.4		3.8		4.3		5.0		7.0	ns
t _{WENSU}	Write Enable Set-Up		2.7		3.0		3.4		4.0		5.6	ns
t _{WENH}	Write Enable Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{BENS}	Block Enable Set-Up		2.8		3.1		3.5		4.1		5.7	ns
t _{BENH}	Block Enable Hold		0.0		0.0		0.0		0.0		0.0	ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 635	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	2.8		3.2		3.6		4.2		5.9		ns
		FO = 635	3.3		3.7		4.2		4.9		6.9		ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	5.5		6.1		6.6		7.6		12.7		ns
		FO = 635	6.0		6.6		7.2		8.3		13.8		ns
f _{MAX}	Maximum Datapath Frequency	FO = 32		180		164		151		131		79	MHz
		FO = 635		166		151		139		121		73	MHz
TTL Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH			2.6		2.8		3.2		3.8		5.3	ns
t _{DHL}	Data-to-Pad LOW			3.0		3.3		3.7		4.4		6.2	ns
t _{ENZH}	Enable Pad Z to HIGH			2.7		3.0		3.3		3.9		5.5	ns
t _{ENZL}	Enable Pad Z to LOW			3.0		3.3		3.7		4.3		6.1	ns
t _{ENHZ}	Enable Pad HIGH to Z			5.3		5.8		6.6		7.8		10.9	ns

Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
117	GNDI
118	NC
119	I/O
120	I/O
121	I/O
122	I/O
123	PROBA
124	I/O
125	CLKA
126	VCC
127	VCCI
128	NC
129	I/O
130	CLKB
131	I/O
132	PROBB
133	I/O
134	I/O
135	I/O
136	GND
137	GNDI
138	NC
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	DCLK

Figure 43 • PQ160

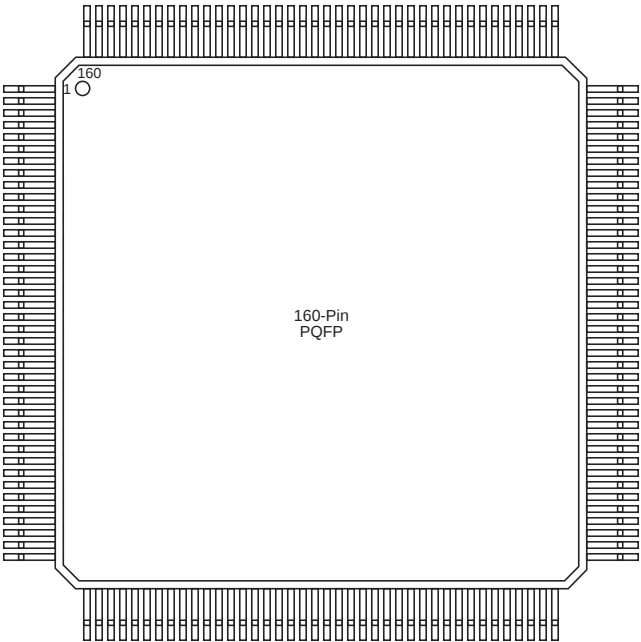


Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	I/O	I/O	I/O
2	DCLK, I/O	DCLK, I/O	DCLK, I/O
3	NC	I/O	I/O
4	I/O	I/O	WD, I/O
5	I/O	I/O	WD, I/O
6	NC	VCCI	VCCI
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	NC	I/O	I/O
11	GND	GND	GND
12	NC	I/O	I/O
13	I/O	I/O	WD, I/O
14	I/O	I/O	WD, I/O
15	I/O	I/O	I/O
16	PRB, I/O	PRB, I/O	PRB, I/O
17	I/O	I/O	I/O
18	CLKB, I/O	CLKB, I/O	CLKB, I/O
19	I/O	I/O	I/O
20	VCCA	VCCA	VCCA

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
200	I/O
201	I/O
202	I/O
203	I/O
204	I/O
205	I/O
206	VCCA
207	I/O
208	I/O
209	VCCA
210	VCCI
211	I/O
212	I/O
213	I/O
214	I/O
215	I/O
216	I/O
217	I/O
218	I/O
219	VCCA
220	I/O
221	I/O
222	I/O
223	I/O
224	I/O
225	I/O
226	I/O
227	VCCI
228	I/O
229	I/O
230	I/O
231	I/O
232	I/O
233	I/O
234	I/O
235	I/O
236	I/O

Table 62 • CQ172

60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	GND
66	VCC
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	GND
76	I/O
77	I/O
78	I/O
79	I/O
80	VCCI
81	I/O
82	I/O
83	I/O
84	I/O
85	SDO
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	GND