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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 83 |
| Number of Gates | 24000 |
| Voltage - Supply | 3V ~ 3.6V, 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-PQFP (20x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-pqg100a |

- The Transient Current, page 13 is new (SAR 36930).
- Package names were revised according to standards established in *Package Mechanical Drawings* (SAR 34774)

## 1.7 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document

- In Table 20, page 23, the limits in VI were changed from -0.5 to VCCI + 0.5 to -0.5 to VCCA + 0.5

In Table 22, page 25, $V_{OH}$ was changed from 3.7 to 2.4 for the min in industrial and military. $V_{IH}$ had $V_{CCI}$ and that was changed to VCCA

## 1.8 Revision 6.0

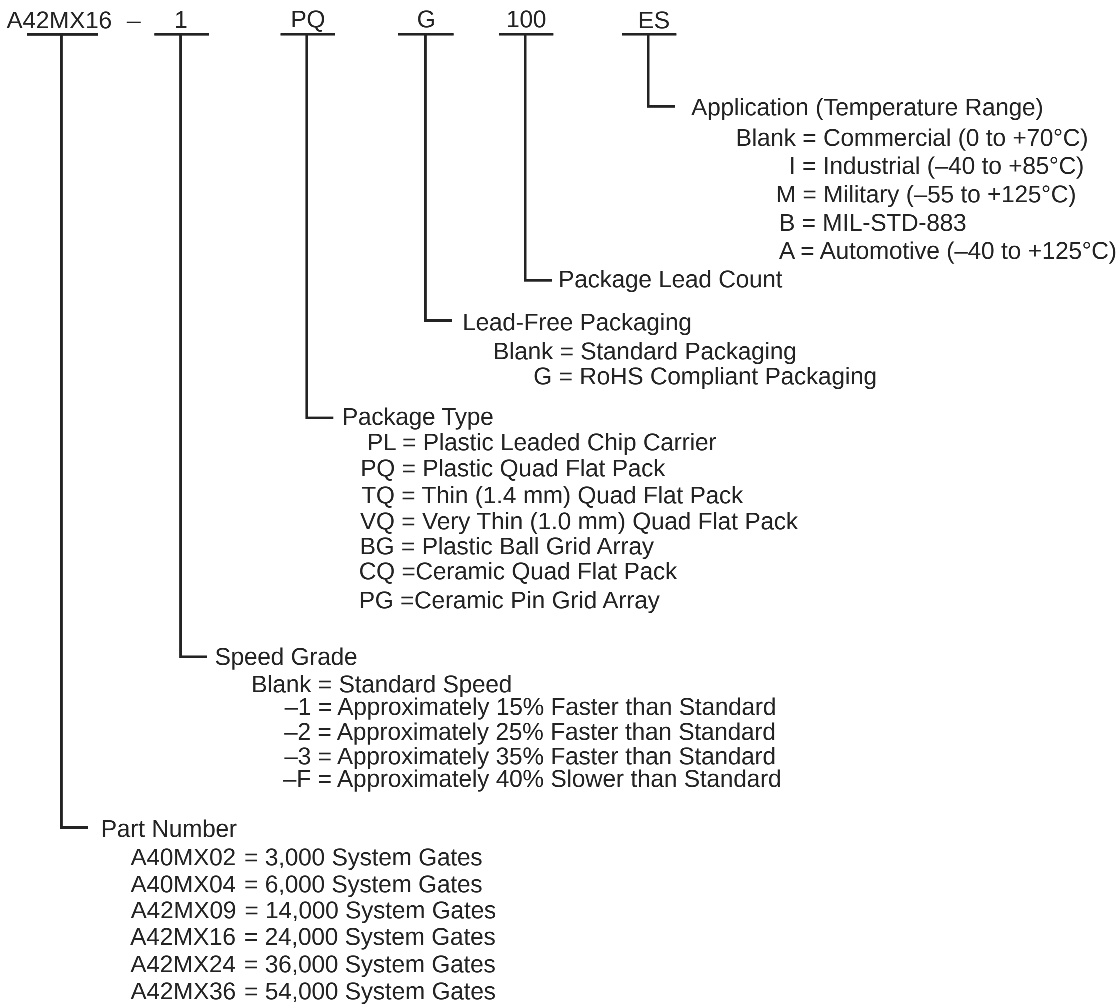
The following is a summary of the changes in revision 6.0 of this document.

- The Ease of Integration, page 1 was updated
- The Temperature Grade Offerings, page 5 is new
- The Speed Grade Offerings, page 5 is new
- The General Description, page 6 was updated
- The MultiPlex I/O Modules, page 11 was updated
- The User Security, page 12 was updated
- Table 6, page 13 was updated
- The Power Dissipation, page 14 was updated.
- The Static Power Component, page 14 was updated
- The Equivalent Capacitance, page 15 was updated
- Figure 13, page 17 was updated
- Table 10, page 18 was updated.
- Figure 14, page 18 was updated.
- Table 11, page 19 was updated.

## 2.3 Ordering Information

The following figure shows ordering information.All the following tables show plastic and ceramic device resources, temperature and speed grade offerings.

***Figure 1 •*** **Ordering Information**



## 2.6 Temperature Grade Offerings

*Table 4 •* **Temperature Grade Offerings**

| Package | A40MX02 | A40MX04 | A42MX09 | A42MX16 | A42MX24 | A42MX36 |
|---|---|---|---|---|---|---|
| PLCC 44 | C, I, M | C, I, M | | | | |
| PLCC 68 | C, I, A, M | C, I, M | | | | |
| PLCC 84 | | C, I, A, M | C, I, A, M | C, I, M | C, I, M | |
| PQFP 100 | C, I, A, M | C, I, A, M | C, I, A, M | C, I, M | | |
| PQFP 144 | | | C | | | |
| PQFP 160 | | | C, I, A, M | C, I, M | C, I, A, M | |
| PQFP 208 | | | | C, I, A, M | C, I, A, M | C, I, A, M |
| PQFP 240 | | | | | | C, I, A, M |
| VQFP 80 | C, I, A, M | C, I, A, M | | | | |
| VQFP 100 | | | C, I, A, M | C, I, A, M | | |
| TQFP 176 | | | C, I, A, M | C, I, A, M | C, I, A, M | |
| PBGA 272 | | | | | | C, I, M |
| CQFP 172 | | | | C, M, B | | |
| CQFP 208 | | | | | | C, M, B |
| CQFP 256 | | | | | | C, M, B |
| CPGA 132 | | | C, M, B | | | |

**Note:** C = Commercial
I = Industrial
A = Automotive
M = Military
B = MIL-STD-883 Class B

## 2.7 Speed Grade Offerings

*Table 5 •* **Speed Grade Offerings**

| | – F | Std | –1 | –2 | –3 |
|---|---|---|---|---|---|
| C | P | P | P | P | P |
| I | | P | P | P | P |
| A | | P | | | |
| M | | P | P | | |
| B | | P | P | | |

**Note:** See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local *Microsemi Sales representative* for device availability.

### 3.3.7 Low Power Mode

42MX devices have been designed with a Low Power Mode. This feature, activated with setting the special LP pin to HIGH for a period longer than 800 ns, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when exiting Low Power Mode. I/Os can be driven during LP mode, and clock pins should be driven HIGH or LOW and should not float to avoid drawing current. To exit LP mode, the LP pin must be pulled LOW for over 200 µs to allow for charge pumps to power up, and device initialization will begin.

## 3.4 Power Dissipation

The general power consumption of MX devices is made up of static and dynamic power and can be expressed with the following equation.

### 3.4.1 General Power Equation

$$P = [ICCstandby + ICCactive]*VCCI + IOL*VOL*N + IOH*(VCCI - VOH)*M$$

**EQ 1**

where:

- ICCstandby is the current flowing when no inputs or outputs are changing.
- ICCactive is the current flowing due to CMOS switching.
- IOL, IOH are TTL sink/source currents.
- VOL, VOH are TTL level output voltages.
- N equals the number of outputs driving TTL loads to VOL.
- M equals the number of outputs driving TTL loads to VOH.

Accurate values for N and M are difficult to determine because they depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

### 3.4.2 Static Power Component

The static power due to standby current is typically a small component of the overall power consumption. Standby power is calculated for commercial, worst-case conditions. The static power dissipation by TTL loads depends on the number of outputs driving, and on the DC load current. For instance, a 32-bit bus sinking 4mA at 0.33V will generate 42mW with all outputs driving LOW, and 140mW with all outputs driving HIGH. The actual dissipation will average somewhere in between, as I/Os switch states with time.

### 3.4.3 Active Power Component

Power dissipation in CMOS devices is usually dominated by the dynamic power dissipation. Dynamic power consumption is frequency-dependent and is a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitances due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

The power dissipated by a CMOS circuit can be expressed by the equation:

$$Power(\mu W) = C_{EQ} * VCCA2 * F(1)$$

**EQ 2**

where:

- $C_{EQ}$ = Equivalent capacitance expressed in picofarads (pF)

***Table 23* • DC Specification (5.0 V PCI Signaling)[1]**

| Symbol | Parameter | Condition | PCI Min. | PCI Max. | MX Min. | MX Max. | Units |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Pin Capacitance | | | 10 | — | 10 | pF |
| $C_{CLK}$ | CLK Pin Capacitance | | 5 | 12 | — | 10 | pF |
| $L_{PIN}$ | Pin Inductance | | | 20 | — | < 8 nH[4] | nH |

1. PCI Local Bus Specification, Version 2.1, Section 4.2.1.1.
2. Maximum rating for VCCI –0.5 V to 7.0 V
3. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V.
4. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

***Table 24* • AC Specifications (5.0V PCI Signaling)[*]**

| Symbol | Parameter | Condition | PCI Min. | PCI Max. | MX Min. | MX Max. | Units |
|---|---|---|---|---|---|---|---|
| ICL | Low Clamp Current | –5 < VIN ≤ –1 | –25 + (VIN +1) /0.015 | | –60 | –10 | mA |
| Slew (r) | Output Rise Slew Rate | 0.4 V to 2.4 V load | 1 | 5 | 1.8 | 2.8 | V/ns |
| Slew (f) | Output Fall Slew Rate | 2.4 V to 0.4 V load | 1 | 5 | 2.8 | 4.3 | V/ns |

**Note:** *PCI Local Bus Specification, Version 2.1, Section 4.2.1.2.

A sample calculation of the absolute maximum power dissipation allowed for a TQ176 package at commercial temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction} \;\; \text{temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient} \;\; \text{temp} \cdot (°\text{C})}{\theta_{ja}(°(\text{C}/\text{W}))} = \frac{150°\text{C} - 70°\text{C}}{(28°\text{C})/\text{W}} = 2.86\text{W}$$

**EQ 5**

The maximum power dissipation for military-grade devices is a function of $\theta_{jc}$. A sample calculation of the absolute maximum power dissipation allowed for CQFP 208-pin package at military temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction} \;\; \text{temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient} \;\; \text{temp} \cdot (°\text{C})}{\theta_{jc}(°(\text{C}/\text{W}))} = \frac{150°\text{C} - 125°\text{C}}{(6.3°\text{C})/\text{W}} = 3.97\text{W}$$

**EQ 6**

***Table 27 •*** **Package Thermal Characteristics**

| | | | $\theta_{ja}$ | | | |
|---|---|---|---|---|---|---|
| **Plastic Packages** | **Pin Count** | $\theta_{jc}$ | **Still Air** | **1.0 m/s 200 ft/min.** | **2.5 m/s 500 ft/min.** | **Units** |
| Plastic Quad Flat Pack | 100 | 12.0 | 27.8 | 23.4 | 21.2 | °C/W |
| Plastic Quad Flat Pack | 144 | 10.0 | 26.2 | 22.8 | 21.1 | °C/W |
| Plastic Quad Flat Pack | 160 | 10.0 | 26.2 | 22.8 | 21.1 | °C/W |
| Plastic Quad Flat Pack | 208 | 8.0 | 26.1 | 22.5 | 20.8 | °C/W |
| Plastic Quad Flat Pack | 240 | 8.5 | 25.6 | 22.3 | 20.8 | °C/W |
| Plastic Leaded Chip Carrier | 44 | 16.0 | 20.0 | 24.5 | 22.0 | °C/W |
| Plastic Leaded Chip Carrier | 68 | 13.0 | 25.0 | 21.0 | 19.4 | °C/W |
| Plastic Leaded Chip Carrier | 84 | 12.0 | 22.5 | 18.9 | 17.6 | °C/W |
| Thin Plastic Quad Flat Pack | 176 | 11.0 | 24.7 | 19.9 | 18.0 | °C/W |
| Very Thin Plastic Quad Flat Pack | 80 | 12.0 | 38.2 | 31.9 | 29.4 | °C/W |
| Very Thin Plastic Quad Flat Pack | 100 | 10.0 | 35.3 | 29.4 | 27.1 | °C/W |
| Plastic Ball Grid Array | 272 | 3.0 | 18.3 | 14.9 | 13.9 | °C/W |
| **Ceramic Packages** | | | | | | |
| Ceramic Pin Grid Array | 132 | 4.8 | 25.0 | 20.6 | 18.7 | °C/W |
| Ceramic Quad Flat Pack | 208 | 2.0 | 22.0 | 19.8 | 18.0 | °C/W |
| Ceramic Quad Flat Pack | 256 | 2.0 | 20.0 | 16.5 | 15.0 | °C/W |

**Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| **CMOS Output Module Timing[5]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 2.4 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 2.9 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 2.7 | | 2.9 | | 3.3 | | 3.9 | | 5.5 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 2.9 | | 3.2 | | 3.7 | | 4.3 | | 6.1 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 4.9 | | 5.4 | | 6.2 | | 7.3 | | 10.2 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.3 | | 5.9 | | 6.7 | | 7.9 | | 11.1 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | 4.2 | | 4.6 | | 5.2 | | 6.1 | | 8.6 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | 4.2 | | 4.6 | | 5.2 | | 6.1 | | 8.6 | ns |
| $t_{LSU}$ | I/O Latch Set-Up | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{LH}$ | I/O Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 5.2 | | 5.8 | | 6.6 | | 7.7 | | 10.8 | ns |
| $t_{ACO}$ | Array Clock-to-Out ( Pad-to-Pad), 64 Clock Loading | | 7.4 | | 8.2 | | 9.3 | | 10.9 | | 15.3 | ns |
| $d_{TLH}$ | Capacity Loading, LOW to HIGH | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.06 | ns/pF |
| $d_{THL}$ | Capacity Loading, HIGH to LOW | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

**Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| **Logic Module Propagation Delays[1]** | | | | | | | | | | | | |
| $t_{PD1}$ | Single Module | | 1.6 | | 1.8 | | 2.1 | | 2.5 | | 3.5 | ns |
| $t_{CO}$ | Sequential Clock-to-Q | | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 3.8 | ns |
| $t_{GO}$ | Latch G-to-Q | | 1.7 | | 1.9 | | 2.1 | | 2.5 | | 3.5 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset-to-Q | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| **Logic Module Predicted Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 1.0 | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.3 | ns |

**Table 41 • A42MX16 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 5.3 | | 5.9 | | 6.7 | | 7.8 | | 11.0 | | ns |
| | | FO = 384 | 6.2 | | 6.9 | | 7.9 | | 9.2 | | 12.9 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | ns |
| | | FO = 384 | | 2.2 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 384 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 3.9 | | 4.3 | | 4.9 | | 5.7 | | 8.0 | | ns |
| | | FO = 384 | 4.5 | | 4.9 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_P$ | Minimum Period | FO = 32 | 7.0 | | 7.8 | | 8.4 | | 9.7 | | 16.2 | | ns |
| | | FO = 384 | 7.7 | | 8.6 | | 9.3 | | 10.7 | | 17.8 | | ns |
| $f_{MAX}$ | Maximum Frequency | FO = 32 | | 142 | | 129 | | 119 | | 103 | | 62 | MHz |
| | | FO = 384 | | 129 | | 117 | | 108 | | 94 | | 56 | MHz |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 3.5 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 4.1 | | 4.6 | | 5.2 | | 6.1 | | 8.6 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.8 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 4.2 | | 4.6 | | 5.3 | | 6.2 | | 8.7 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.6 | | 8.4 | | 9.5 | | 11.2 | | 15.7 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 7.0 | | 7.8 | | 8.8 | | 10.4 | | 14.5 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | | 8.0 | | 8.9 | | 10.1 | | 11.9 | | 16.7 | ns |
| $t_{ACO}$ | Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | | 11.3 | | 12.5 | | 14.2 | | 16.7 | | 23.3 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| $d_{THL}$ | Capacitive Loading, HIGH to LOW | | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.10 | ns/pF |
| **CMOS Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 4.5 | | 5.0 | | 5.6 | | 6.6 | | 9.3 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 3.4 | | 3.8 | | 4.3 | | 5.1 | | 7.1 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.8 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 4.2 | | 4.6 | | 5.3 | | 6.2 | | 8.7 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.6 | | 8.4 | | 9.5 | | 11.2 | | 15.7 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 7.0 | | 7.8 | | 8.8 | | 10.4 | | 14.5 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 7.1 | | 7.9 | | 8.9 | | 10.5 | | 14.7 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 7.1 | | 7.9 | | 8.9 | | 10.5 | | 14.7 | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | | 8.0 | | 8.9 | | 10.1 | | 11.9 | | 16.7 | ns |

**Table 43 •** **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Input Module Predicted Routing Delays[2]** | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.6 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 2.9 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 3.2 | | 3.6 | | 4.0 | | 4.8 | | 6.6 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 3.5 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 4.8 | | 5.3 | | 6.1 | | 7.1 | | 10.0 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 32<br>FO = 486 | | 4.4<br>4.8 | | 4.8<br>5.3 | | 5.5<br>6.0 | | 6.5<br>7.1 | | 9.1<br>10.0 | ns<br>ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 32<br>FO = 486 | | 5.1<br>6.0 | | 5.7<br>6.6 | | 6.4<br>7.5 | | 7.6<br>8.8 | | 10.6<br>12.4 | ns<br>ns |
| $t_{PWH}$ | Minimum Pulse<br>Width HIGH | FO = 32<br>FO = 486 | 3.0<br>3.3 | | 3.3<br>3.7 | | 3.8<br>4.2 | | 4.5<br>4.9 | | 6.3<br>6.9 | | ns<br>ns |
| $t_{PWL}$ | Minimum Pulse<br>Width LOW | FO = 32<br>FO = 486 | 3.0<br>3.3 | | 3.4<br>3.7 | | 3.8<br>4.2 | | 4.5<br>4.9 | | 6.3<br>6.9 | | ns<br>ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32<br>FO = 486 | | 0.8<br>0.8 | | 0.8<br>0.8 | | 1.0<br>1.0 | | 1.1<br>1.1 | | 1.6<br>1.6 | ns<br>ns |
| $t_{SUEXT}$ | Input Latch External<br>Set-Up | FO = 32<br>FO = 486 | 0.0<br>0.0 | | 0.0<br>0.0 | | 0.0<br>0.0 | | 0.0<br>0.0 | | 0.0<br>0.0 | | ns<br>ns |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.1 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 4.0 | | 4.4 | | 5.0 | | 5.9 | | 8.3 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.4 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 3.9 | | 4.4 | | 5.0 | | 5.8 | | 8.2 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.2 | | 8.0 | | 9.1 | | 10.7 | | 14.9 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 6.7 | | 7.5 | | 8.5 | | 9.9 | | 13.9 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| $t_{LSU}$ | I/O Latch Output Set-Up | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |

***Table 45 •*** **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RD5}$ | FO = 8 Routing Delay | | 4.6 | | 5.2 | | 5.8 | | 6.9 | | 9.6 | ns |
| $t_{RDD}$ | Decode-to-Output Routing Delay | | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | ns |
| **Logic Module Sequential Timing[3, 4]** | | | | | | | | | | | | |
| $t_{CO}$ | Flip-Flop Clock-to-Output | | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{GO}$ | Latch Gate-to-Output | | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{SUD}$ | Flip-Flop (Latch) Set-Up Time | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 0.9 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RO}$ | Flip-Flop (Latch) Reset-to-Output | | 2.2 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 1.0 | | 1.1 | | 1.2 | | 1.4 | | 2.0 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.6 | | 5.2 | | 5.8 | | 6.9 | | 9.6 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 6.1 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | | ns |
| **Synchronous SRAM Operations** | | | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 9.5 | | 10.5 | | 11.9 | | 14.0 | | 19.6 | | ns |
| $t_{WC}$ | Write Cycle Time | 9.5 | | 10.5 | | 11.9 | | 14.0 | | 19.6 | | ns |
| $t_{RCKHL}$ | Clock HIGH/LOW Time | 4.8 | | 5.3 | | 6.0 | | 7.0 | | 9.8 | | ns |
| $t_{RCO}$ | Data Valid After Clock HIGH/LOW | | 4.8 | | 5.3 | | 6.0 | | 7.0 | | 9.8 | ns |
| $t_{ADSU}$ | Address/Data Set-Up Time | 2.3 | | 2.5 | | 2.8 | | 3.4 | | 4.8 | | ns |

***Table 50 •*** **PQ 100**

| **PQ100** | | | | |
|---|---|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** | **A42MX09 Function** | **A42MX16 Function** |
| 19 | VCC | $V_{CC}$ | I/O | I/O |
| 20 | I/O | I/O | I/O | I/O |
| 21 | I/O | I/O | I/O | I/O |
| 22 | I/O | I/O | GND | GND |
| 23 | I/O | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O | I/O |
| 27 | NC | NC | I/O | I/O |
| 28 | NC | NC | I/O | I/O |
| 29 | NC | NC | I/O | I/O |
| 30 | NC | NC | I/O | I/O |
| 31 | NC | I/O | I/O | I/O |
| 32 | NC | I/O | I/O | I/O |
| 33 | NC | I/O | I/O | I/O |
| 34 | I/O | I/O | GND | GND |
| 35 | I/O | I/O | I/O | I/O |
| 36 | GND | GND | I/O | I/O |
| 37 | GND | GND | I/O | I/O |
| 38 | I/O | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O | I/O |
| 40 | I/O | I/O | VCCA | VCCA |
| 41 | I/O | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O | I/O |
| 43 | VCC | VCC | I/O | I/O |
| 44 | VCC | VCC | I/O | I/O |
| 45 | I/O | I/O | I/O | I/O |
| 46 | I/O | I/O | GND | GND |
| 47 | I/O | I/O | I/O | I/O |
| 48 | NC | I/O | I/O | I/O |
| 49 | NC | I/O | I/O | I/O |
| 50 | NC | I/O | I/O | I/O |
| 51 | NC | NC | I/O | I/O |
| 52 | NC | NC | SDO, I/O | SDO, I/O |
| 53 | NC | NC | I/O | I/O |
| 54 | NC | NC | I/O | I/O |
| 55 | NC | NC | I/O | I/O |

***Table 50 •*** **PQ 100**

| **PQ100** | | | | |
|---|---|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** | **A42MX09 Function** | **A42MX16 Function** |
| 93 | VCC | VCC | I/O | I/O |
| 94 | VCC | VCC | PRB, I/O | PRB, I/O |
| 95 | NC | I/O | I/O | I/O |
| 96 | NC | I/O | GND | GND |
| 97 | NC | I/O | I/O | I/O |
| 98 | SDI, I/O | SDI, I/O | I/O | I/O |
| 99 | DCLK, I/O | DCLK, I/O | I/O | I/O |
| 100 | PRA, I/O | PRA, I/O | I/O | I/O |

***Table 51 •*** **PQ144**

| **PQ144** | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| 80 | GNDI |
| 81 | NC |
| 82 | I/O |
| 83 | I/O |
| 84 | I/O |
| 85 | I/O |
| 86 | I/O |
| 87 | I/O |
| 88 | VKS |
| 89 | VPP |
| 90 | VCC |
| 91 | VCCI |
| 92 | NC |
| 93 | VSV |
| 94 | I/O |
| 95 | I/O |
| 96 | I/O |
| 97 | I/O |
| 98 | I/O |
| 99 | I/O |
| 100 | GND |
| 101 | GNDI |
| 102 | NC |
| 103 | I/O |
| 104 | I/O |
| 105 | I/O |
| 106 | I/O |
| 107 | I/O |
| 108 | I/O |
| 109 | I/O |
| 110 | SDI |
| 111 | I/O |
| 112 | I/O |
| 113 | I/O |
| 114 | I/O |
| 115 | I/O |
| 116 | GNDQ |

***Table 52 •*** **PQ160**

| **PQ160** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 21 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 22 | I/O | I/O | I/O |
| 23 | PRA, I/O | PRA, I/O | PRA, I/O |
| 24 | NC | I/O | WD, I/O |
| 25 | I/O | I/O | WD, I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | NC | I/O | I/O |
| 29 | I/O | I/O | WD, I/O |
| 30 | GND | GND | GND |
| 31 | NC | I/O | WD, I/O |
| 32 | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O |
| 35 | NC | VCCI | VCCI |
| 36 | I/O | I/O | WD, I/O |
| 37 | I/O | I/O | WD, I/O |
| 38 | SDI, I/O | SDI, I/O | SDI, I/O |
| 39 | I/O | I/O | I/O |
| 40 | GND | GND | GND |
| 41 | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | GND | GND | GND |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | GND | GND | GND |
| 50 | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O |
| 52 | NC | I/O | I/O |
| 53 | I/O | I/O | I/O |
| 54 | NC | VCCA | VCCA |
| 55 | I/O | I/O | I/O |
| 56 | I/O | I/O | I/O |
| 57 | VCCA | VCCA | VCCA |

***Table 52 •*** **PQ160**

| **PQ160** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 132 | I/O | I/O | I/O |
| 133 | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O |
| 135 | NC | VCCA | VCCA |
| 136 | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O |
| 138 | NC | VCCA | VCCA |
| 139 | VCCI | VCCI | VCCI |
| 140 | GND | GND | GND |
| 141 | NC | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | I/O | I/O | I/O |
| 144 | I/O | I/O | I/O |
| 145 | GND | GND | GND |
| 146 | NC | I/O | I/O |
| 147 | I/O | I/O | I/O |
| 148 | I/O | I/O | I/O |
| 149 | I/O | I/O | I/O |
| 150 | NC | VCCA | VCCA |
| 151 | NC | I/O | I/O |
| 152 | NC | I/O | I/O |
| 153 | NC | I/O | I/O |
| 154 | NC | I/O | I/O |
| 155 | GND | GND | GND |
| 156 | I/O | I/O | I/O |
| 157 | I/O | I/O | I/O |
| 158 | I/O | I/O | I/O |
| 159 | MODE | MODE | MODE |
| 160 | GND | GND | GND |

***Table 53 •*** **PQ208**

| **PQ208** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX16 Function** | **A42MX24 Function** | **A42MX36 Function** |
| 58 | I/O | WD, I/O | WD, I/O |
| 59 | I/O | I/O | I/O |
| 60 | VCCI | VCCI | VCCI |
| 61 | NC | I/O | I/O |
| 62 | NC | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | I/O | I/O | I/O |
| 65 | I/O | I/O | QCLKA, I/O |
| 66 | I/O | WD, I/O | WD, I/O |
| 67 | NC | WD, I/O | WD, I/O |
| 68 | NC | I/O | I/O |
| 69 | I/O | I/O | I/O |
| 70 | I/O | WD, I/O | WD, I/O |
| 71 | I/O | WD, I/O | WD, I/O |
| 72 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | GND | GND | GND |
| 79 | VCCA | VCCA | VCCA |
| 80 | NC | VCCI | VCCI |
| 81 | I/O | I/O | I/O |
| 82 | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | WD, I/O | WD, I/O |
| 86 | I/O | WD, I/O | WD, I/O |
| 87 | I/O | I/O | I/O |
| 88 | I/O | I/O | I/O |
| 89 | NC | I/O | I/O |
| 90 | NC | I/O | I/O |
| 91 | I/O | I/O | QCLKB, I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | WD, I/O | WD, I/O |
| 94 | I/O | WD, I/O | WD, I/O |

***Figure 47 •*** **VQ100**

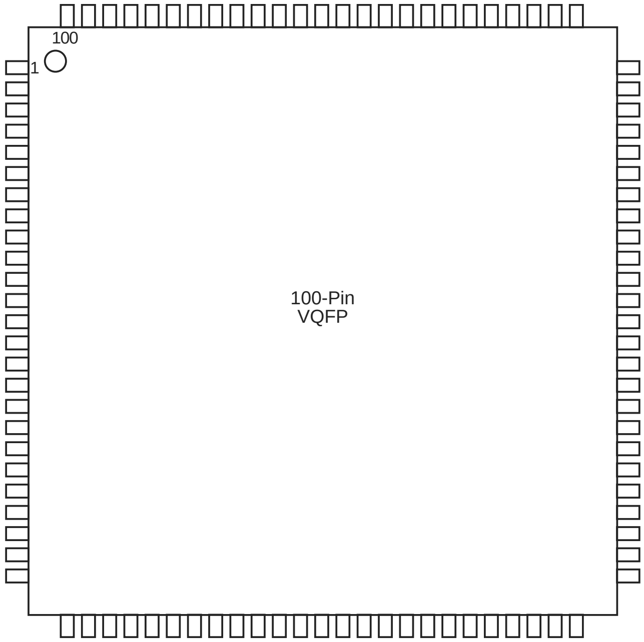



***Table 56 •*** **VQ100**

| **VQ100** | | |
|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** |
| 1 | I/O | I/O |
| 2 | MODE | MODE |
| 3 | I/O | I/O |
| 4 | I/O | I/O |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | GND | GND |
| 8 | I/O | I/O |
| 9 | I/O | I/O |
| 10 | I/O | I/O |
| 11 | I/O | I/O |
| 12 | I/O | I/O |
| 13 | I/O | I/O |
| 14 | VCCA | NC |
| 15 | VCCI | VCCI |
| 16 | I/O | I/O |
| 17 | I/O | I/O |
| 18 | I/O | I/O |
| 19 | I/O | I/O |
| 20 | GND | GND |

***Table 57 •*** **TQ176**

| **TQ176** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 121 | NC | NC | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | NC | I/O | I/O |
| 125 | NC | I/O | I/O |
| 126 | NC | NC | I/O |
| 127 | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O |
| 129 | I/O | I/O | I/O |
| 130 | I/O | I/O | I/O |
| 131 | I/O | I/O | I/O |
| 132 | I/O | I/O | I/O |
| 133 | GND | GND | GND |
| 134 | I/O | I/O | I/O |
| 135 | SDI, I/O | SDI, I/O | SDI, I/O |
| 136 | NC | I/O | I/O |
| 137 | I/O | I/O | WD, I/O |
| 138 | I/O | I/O | WD, I/O |
| 139 | I/O | I/O | I/O |
| 140 | NC | VCCI | VCCI |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | NC | I/O | I/O |
| 144 | NC | I/O | WD, I/O |
| 145 | NC | NC | WD, I/O |
| 146 | I/O | I/O | I/O |
| 147 | NC | I/O | I/O |
| 148 | I/O | I/O | I/O |
| 149 | I/O | I/O | I/O |
| 150 | I/O | I/O | WD, I/O |
| 151 | NC | I/O | WD, I/O |
| 152 | PRA, I/O | PRA, I/O | PRA, I/O |
| 153 | I/O | I/O | I/O |
| 154 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 155 | VCCA | VCCA | VCCA |
| 156 | GND | GND | GND |
| 157 | I/O | I/O | I/O |

***Table 58 •*** **CQ208**

| **CQ208** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 37 | I/O |
| 38 | I/O |
| 39 | I/O |
| 40 | I/O |
| 41 | I/O |
| 42 | I/O |
| 43 | I/O |
| 44 | I/O |
| 45 | I/O |
| 46 | I/O |
| 47 | I/O |
| 48 | I/O |
| 49 | I/O |
| 50 | I/O |
| 51 | I/O |
| 52 | GND |
| 53 | GND |
| 54 | TMS, I/O |
| 55 | TDI, I/O |
| 56 | I/O |
| 57 | WD, I/O |
| 58 | WD, I/O |
| 59 | I/O |
| 60 | VCCI |
| 61 | I/O |
| 62 | I/O |
| 63 | I/O |
| 64 | I/O |
| 65 | QCLKA, I/O |
| 66 | WD, I/O |
| 67 | WD, I/O |
| 68 | I/O |
| 69 | I/O |
| 70 | WD, I/O |
| 71 | WD, I/O |
| 72 | I/O |
| 73 | I/O |

***Table 60 •*** **BG272**

| BG272 | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| Y13 | I/O |
| Y14 | I/O |
| Y15 | I/O |
| Y16 | I/O |
| Y17 | I/O |
| Y18 | WD, I/O |
| Y19 | GND |
| Y20 | GND |

***Figure 52 •*** **PG132**

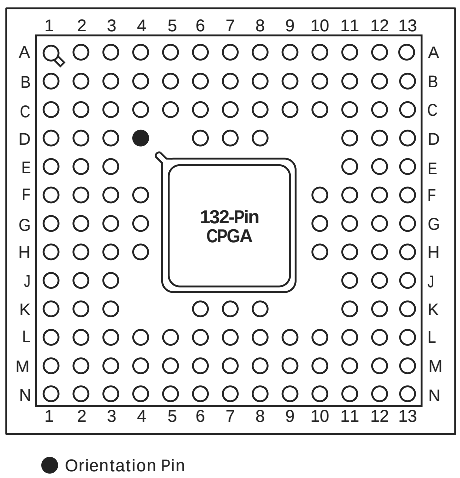



***Table 61 •*** **PG132**

| PG132 | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| – | PMPOUT |
| B2 | I/O |
| A1 | MODE |
| B1 | I/O |
| D3 | I/O |
| C2 | I/O |
| C1 | I/O |
| D2 | I/O |
| D1 | I/O |
| E2 | I/O |
| E1 | I/O |
| F3 | I/O |