



Welcome to [E·XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	125
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-pqg160a

Contents

1	Revision History	1
1.1	Revision 15.0	1
1.2	Revision 14.0	1
1.3	Revision 13.0	1
1.4	Revision 12.0	1
1.5	Revision 11.0	1
1.6	Revision 10.0	1
1.7	Revision 9.0	2
1.8	Revision 6.0	2
2	40MX and 42MX FPGA Families	1
2.1	Features	1
2.1.1	High Capacity	1
2.1.2	High Performance	1
2.1.3	HiRel Features	1
2.1.4	Ease of Integration	1
2.2	Product Profile	1
2.3	Ordering Information	3
2.4	Plastic Device Resources	4
2.5	Ceramic Device Resources	4
2.6	Temperature Grade Offerings	5
2.7	Speed Grade Offerings	5
3	40MX and 42MX FPGAs	6
3.1	General Description	6
3.2	MX Architectural Overview	6
3.2.1	Logic Modules	6
3.2.2	Dual-Port SRAM Modules	8
3.2.3	Routing Structure	9
3.2.4	Clock Networks	10
3.2.5	MultiPlex I/O Modules	11
3.3	Other Architectural Features	12
3.3.1	Performance	12
3.3.2	User Security	12
3.3.3	Programming	12
3.3.4	Power Supply	13
3.3.5	Power-Up/Down in Mixed-Voltage Mode	13
3.3.6	Transient Current	13
3.3.7	Low Power Mode	14
3.4	Power Dissipation	14
3.4.1	General Power Equation	14
3.4.2	Static Power Component	14
3.4.3	Active Power Component	14
3.4.4	Equivalent Capacitance	15
3.4.5	C _{EQ} Values for Microsemi MX FPGAs	15
3.4.6	Test Circuitry and Silicon Explorer II Probe	16
3.4.7	Design Consideration	17
3.4.8	IEEE Standard 1149.1 Boundary Scan Test (BST) Circuitry	17
3.4.9	JTAG Mode Activation	19
3.4.10	TRST Pin and TAP Controller Reset	19

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- Table 15, page 21 is edited to add the footnote, $V_{IH}(\text{Min})$ is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 22, page 25 is edited to add the footnote, $V_{IH}(\text{Min})$ is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 23, page 25 is edited to add the footnote, $V_{IH}(\text{Min})$ is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

1.2 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Added CQFP package information for A42MX16 device in Product Profile, page 1 and Ceramic Device Resources, page 4 (SAR 79522).
- Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in Temperature Grade Offerings, page 5 (SAR 79519)
- Changed Silicon Sculptor II to Silicon Sculptor in Programming, page 12 (SAR 38754)
- Added Figure 53, page 158 CQ172 package (SAR 79522).

1.3 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Added Figure 42, page 97 PQ144 Package for A42MX09 device (SAR 69776)
- Added Figure 52, page 153 PQ132 Package for A42MX09 device (SAR 69776)

1.4 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Added information on power-up behavior for A42MX24 and A42MX36 devices to the Power Supply, page 13 (SAR 42096)
- Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793)

1.5 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- The FuseLock logo and accompanying text was removed from the User Security, page 12. This marking is no longer used on Microsemi devices (PCN 0915)
- The Development Tool Support, page 19 was updated (SAR 38512)

1.6 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- Ordering Information, page 3 was updated to include lead-free package ordering codes (SAR 21968)
- The User Security, page 12 was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673)

2.4 Plastic Device Resources

Table 2 • Plastic Device Resources

Device	User I/Os											
	PLCC 44-Pin	PLCC 68-Pin	PLCC 84-Pin	PQFP 100-Pin	PQFP 144- Pin	PQFP 160-Pin	PQFP 208- Pin	PQFP 240-Pin	VQFP 80-Pin	VQFP 100- Pin	TQFP 176- Pin	PBGA 272- Pin
A40MX02	34	57	–	57	–	–	–	–	57	–	–	–
A40MX04	34	57	69	69	–	–	–	–	69	–	–	–
A42MX09	–	–	72	83	95	101	–	–	–	83	104	–
A42MX16	–	–	72	83	–	125	140	–	–	83	140	–
A42MX24	–	–	72	–	–	125	176	–	–	–	150	–
A42MX36	–	–	–	–	–	–	176	202	–	–	–	202

Note: Package Definitions: PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array

2.5 Ceramic Device Resources

Table 3 • Ceramic Device Resources

Device	User I/Os			
	CPGA 132-Pin	CQFP 172-Pin	CQFP 208-Pin	CQFP 256-Pin
A42MX09	95			
A42MX16		131		
A42MX36			176	202

Note: Package Definitions: CQFP = Ceramic Quad Flat Pack

3 40MX and 42MX FPGAs

3.1 General Description

Microsemi's 40MX and 42MX families offer a cost-effective design solution at 5V. The MX devices are single-chip solutions and provide high performance while shortening the system design and development cycle. MX devices can integrate and consolidate logic implemented in multiple PALs, CPLDs, and FPGAs. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

The MX device architecture is based on Microsemi's patented antifuse technology implemented in a 0.45µm triple-metal CMOS process. With capacities ranging from 3,000 to 54,000 system gates, the MX devices provide performance up to 250 MHz, are live on power-up and have one-fifth the standby power consumption of comparable FPGAs. MX FPGAs provide up to 202 user I/Os and are available in a wide variety of packages and speed grades.

A42MX24 and A42MX36 devices also feature multiPlex I/Os, which support mixed-voltage systems, enable programmable PCI, deliver high-performance operation at both 5.0V and 3.3V, and provide a low-power mode. The devices are fully compliant with the PCI local bus specification (version 2.1). They deliver 200 MHz on-chip operation and 6.1 ns clock-to-output performance.

The 42MX24 and 42MX36 devices include system-level features such as IEEE Standard 1149.1 (JTAG) Boundary Scan Testing and fast wide-decode modules. In addition, the A42MX36 device offers dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The storage elements can efficiently address applications requiring wide data path manipulation and can perform transformation functions such as those required for telecommunications, networking, and DSP.

All MX devices are fully tested over automotive and military temperature ranges. In addition, the largest member of the family, the A42MX36, is available in both CQ208 and CQ256 ceramic packages screened to MIL-STD-883 levels. For easy prototyping and conversion from plastic to ceramic, the CQ208 and PQ208 devices are pin-compatible.

3.2 MX Architectural Overview

The MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within these families are composed of logic modules, I/O modules, routing resources and clock networks, which are the building blocks for fast logic designs. In addition, the A42MX36 device contains embedded dual-port SRAM modules, which are optimized for high-speed data path functions such as FIFOs, LIFOs and scratch pad memory. A42MX24 and A42MX36 also contain wide-decode modules.

3.2.1 Logic Modules

The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources.(see the following figure).

The logic module can implement the four basic logic functions (NAND, AND, OR and NOR) in gates of two, three, or four inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array; latches and flip-flops can be constructed from logic modules whenever required in the application.

3.9.3 Output Drive Characteristics for 3.3 V PCI Signaling

Table 25 • DC Specification (3.3 V PCI Signaling)¹

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
VCCI	Supply Voltage for I/Os		3.0	3.6	3.0	3.6 ²	V
VIH	Input High Voltage		0.5	VCC + 0.5	0.5	VCCI + 0.3	V
VIL	Input Low Voltage		−0.5	0.8	−0.3	0.8	V
IIH	Input High Leakage Current	VIN = 2.7 V		70		10	μA
IIL	Input Leakage Current			−70		−10	μA
VOH	Output High Voltage	IOUT = −2 mA	0.9		3.3		V
VOL	Output Low Voltage	IOUT = 3 mA, 6 mA		0.1		0.1 VCCI	V
CIN	Input Pin Capacitance			10		10	pF
CLK	CLK Pin Capacitance		5	12		10	pF
L _{PIN}	Pin Inductance			20		< 8 nH ³	nH

1. PCI Local Bus Specification, Version 2.1, Section 4.2.2.1.

2. Maximum rating for VCCI −0.5 V to 7.0V.

3. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

Table 26 • AC Specifications for (3.3 V PCI Signaling)*

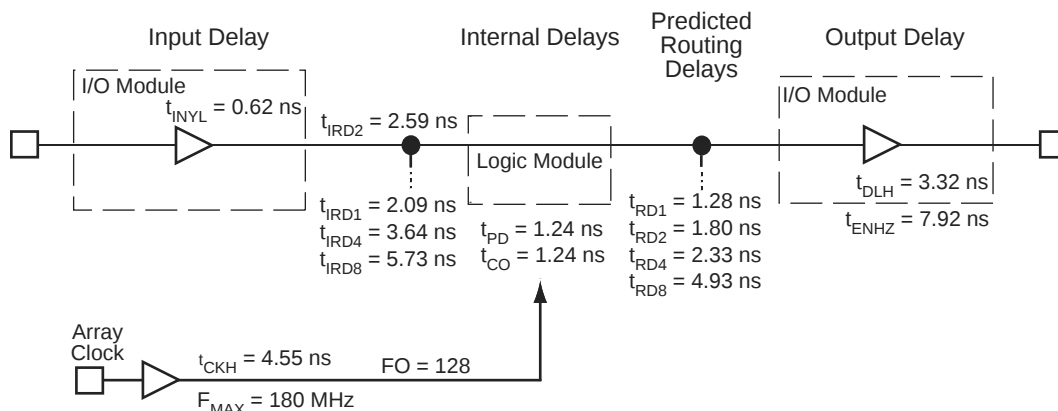
Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
ICL	Low Clamp Current	−5 < VIN ≤ −1	−25 + (VIN + 1) / 0.015		−60	−10	mA
Slew (r)	Output Rise Slew Rate	0.2 V to 0.6 V load	1	4	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	0.6 V to 0.2 V load	1	4	2.8	4.0	V/ns

Note: *PCI Local Bus Specification, Version 2.1, Section 4.2.2.2.

3.10 Timing Models

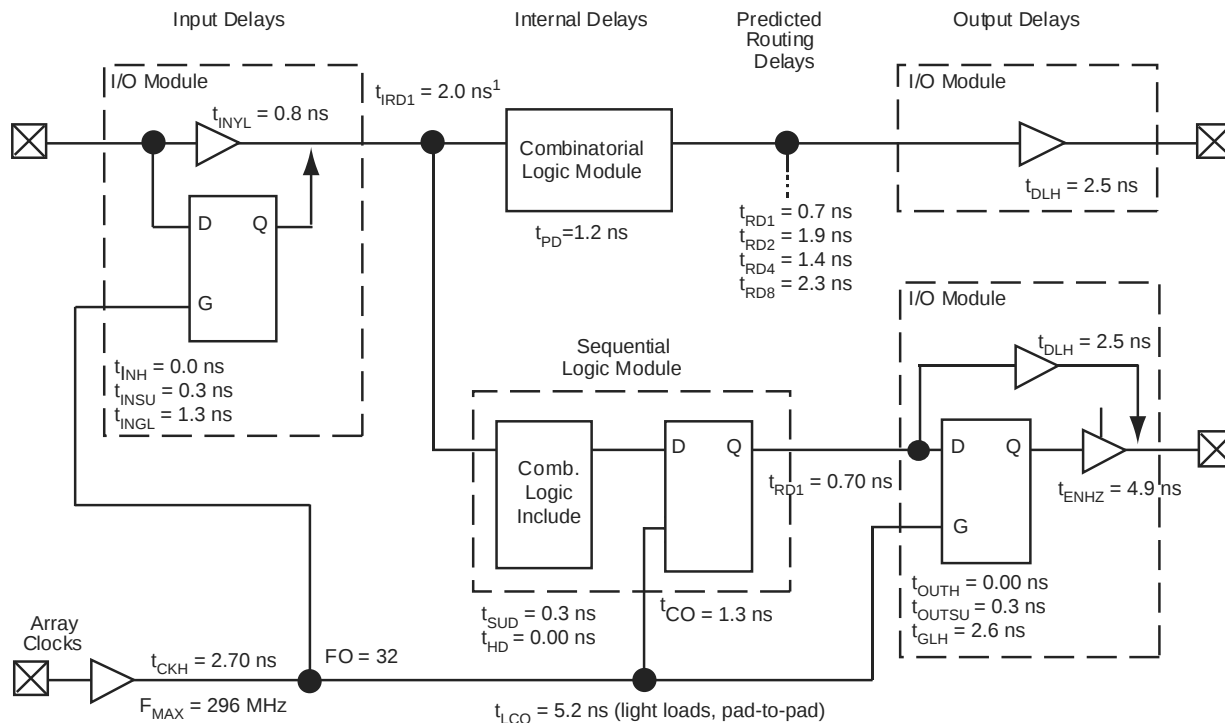
The following figures show various timing models.

Figure 17 • 40MX Timing Model*



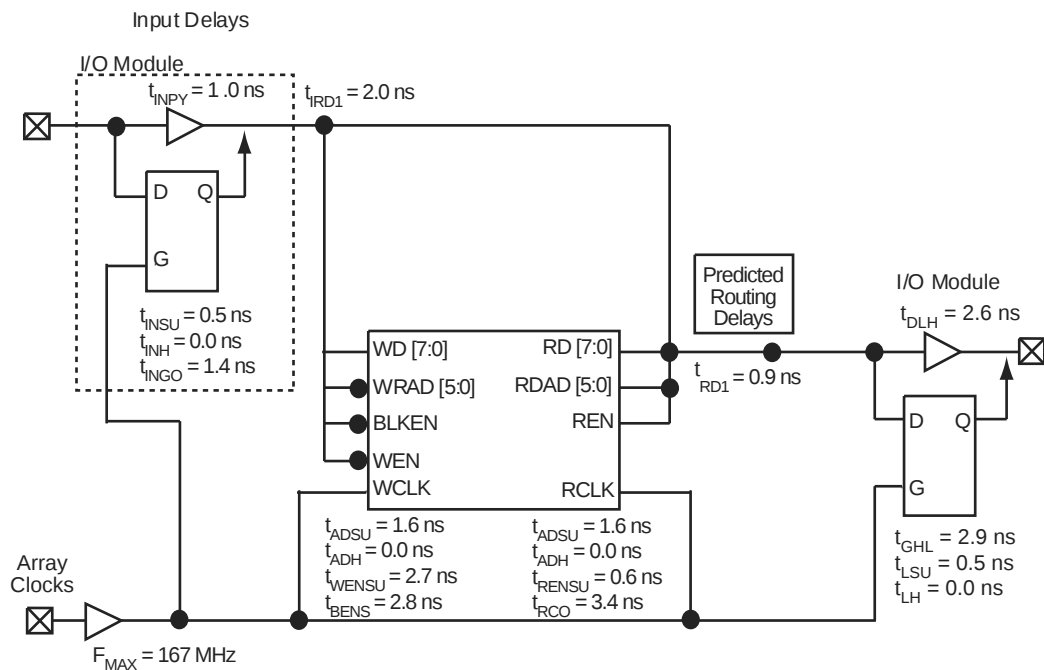
Note: Values are shown for 40MX –3 speed devices at 5.0 V worst-case commercial conditions.

Figure 18 • 42MX Timing Model



Note: 1. Input module predicted routing delay

Note: 2. Values are shown for A42MX09 –3 at 5.0 V worst-case commercial conditions.

Figure 20 • 42MX Timing Model (SRAM Functions)

Note: Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions.

3.10.1 Parameter Measurement

The following figures show parameter measurement details.

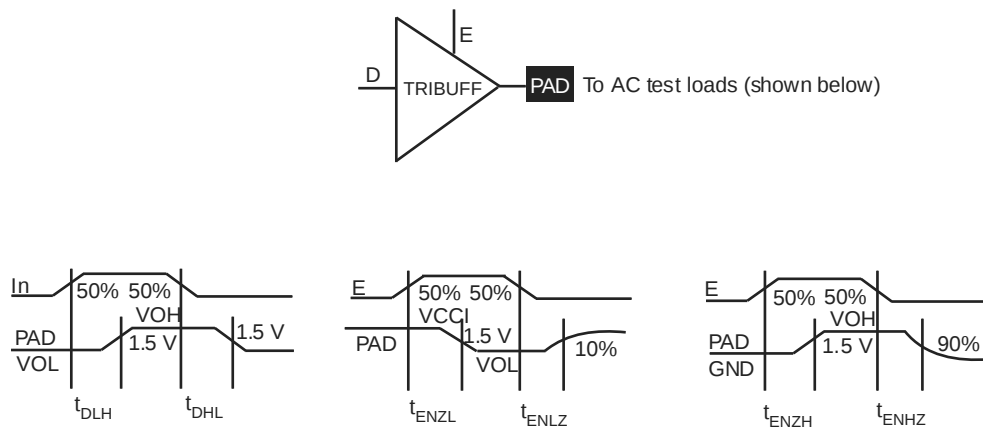
Figure 21 • Output Buffer Delays

Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH		3.3		3.8		4.3		5.1		7.2	ns
t _{DHL}	Data-to-Pad LOW		4.0		4.6		5.2		6.1		8.6	ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.3		4.9		5.8		8.0	ns
t _{ENZL}	Enable Pad Z to LOW		4.7		5.4		6.1		7.2		10.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.1	ns
t _{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{THL}	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t _{DHL}	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t _{ENZH}	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t _{ENZL}	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t _{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t _{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d _{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35pF loading

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t _{PD2}	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t _{CO}	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t _{GO}	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays ¹												

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RD1}	FO = 1 Routing Delay			2.0		2.2		2.5		3.0		4.2	ns
t _{RD2}	FO = 2 Routing Delay			2.7		3.1		3.5		4.1		5.7	ns
t _{RD3}	FO = 3 Routing Delay			3.4		3.9		4.4		5.2		7.3	ns
t _{RD4}	FO = 4 Routing Delay			4.2		4.8		5.4		6.3		8.9	ns
t _{RD8}	FO = 8 Routing Delay			7.1		8.2		9.2		10.9		15.2	ns
Logic Module Sequential Timing²													
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		4.3		4.9		5.6		6.6		9.2		ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		4.3		4.9		5.6		6.6		9.2		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		4.6		5.3		6.0		7.0		9.8		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		4.6		5.3		6.0		7.0		9.8		ns
t _A	Flip-Flop Clock Input Period		6.8		7.8		8.9		10.4		14.6		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)			109		101		92		80		48	MHz
Input Module Propagation Delays													
t _{INYH}	Pad-to-Y HIGH			1.0		1.1		1.3		1.5		2.1	ns
t _{INYL}	Pad-to-Y LOW			0.9		1.0		1.1		1.3		1.9	ns
Input Module Predicted Routing Delays¹													
t _{IRD1}	FO = 1 Routing Delay			2.9		3.4		3.8		4.5		6.3	ns
t _{IRD2}	FO = 2 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t _{IRD3}	FO = 3 Routing Delay			4.4		5.0		5.7		6.7		9.4	ns
t _{IRD4}	FO = 4 Routing Delay			5.1		5.9		6.7		7.8		11.0	ns
t _{IRD8}	FO = 8 Routing Delay			8.0		9.26		10.5		12.6		17.3	ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 16		6.4		7.4		8.3		9.8		13.7	ns
		FO = 128		6.4		7.4		8.3		9.8		13.7	
t _{CKL}	Input HIGH to LOW	FO = 16		6.7		7.8		8.8		10.4		14.5	ns
		FO = 128		6.7		7.8		8.8		10.4		14.5	
t _{PWH}	Minimum Pulse Width HIGH	FO = 16	3.1		3.6		4.1		4.8		6.7		ns
		FO = 128	3.3		3.8		4.3		5.1		7.1		
t _{PWL}	Minimum Pulse Width LOW	FO = 16	3.1		3.6		4.1		4.8		6.7		ns
		FO = 128	3.3		3.8		4.3		5.1		7.1		
t _{CKSW}	Maximum Skew	FO = 16		0.6		0.6		0.7		0.8		1.2	ns
		FO = 128		0.8		0.9		1.0		1.2		1.6	

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{THL}	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RD4}	FO = 4 Routing Delay	1.9		2.1		2.4		2.9		4.0		ns
t _{RD8}	FO = 8 Routing Delay	3.2		3.6		4.1		4.8		6.7		ns
Logic Module Sequential Timing ^{3, 4}												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.5		0.5		0.6		0.7		0.9		ns
t _{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.7		5.3		6.0		7.0		9.8		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.2		6.9		7.8		9.2		12.9		ns
t _A	Flip-Flop Clock Input Period	5.0		5.6		6.2		7.1		9.9		ns
t _{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
t _{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{OUTSU}	Output Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency	161		146		135		117		70		MHz

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays												
t _{INPY}	Input Data Pad-to-Y		1.0		1.1		1.3		1.5		2.1	ns
t _{INGO}	Input Latch Gate-to-Output		1.3		1.4		1.6		1.9		2.6	ns
t _{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{ILA}	Latch Active Pulse Width	4.7		5.2		5.9		6.9		9.7		ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions ¹												
t _{PD}	Internal Array Module Delay		1.3		1.5		1.7		2.0		2.7	ns
t _{PDD}	Internal Decode Module Delay		1.6		1.8		2.0		2.4		3.3	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.2		1.4		2.0	ns
t _{RD2}	FO = 2 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t _{RD3}	FO =3 Routing Delay		1.6		1.8		2.0		2.4		3.4	ns
t _{RD4}	FO = 4 Routing Delay		2.0		2.2		2.5		2.9		4.1	ns
t _{RD5}	FO = 8 Routing Delay		3.3		3.7		4.2		4.9		6.9	ns
t _{RDD}	Decode-to-Output Routing Delay		0.3		0.4		0.4		0.5		0.7	ns
Logic Module Sequential Timing ^{3, 4}												
t _{CO}	Flip-Flop Clock-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t _{GO}	Latch Gate-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t _{SUD}	Flip-Flop (Latch) Set-Up Time	0.3		0.3		0.4		0.5		0.7		ns
t _{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RO}	Flip-Flop (Latch) Reset-to-Output		1.6		1.7		2.0		2.3		3.2	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.5		6.4		9.0		ns
Synchronous SRAM Operations												
t _{RC}	Read Cycle Time		6.8		7.5		8.5		10.0		14.0	ns
t _{WC}	Write Cycle Time		6.8		7.5		8.5		10.0		14.0	ns
t _{RCKHL}	Clock HIGH/LOW Time		3.4		3.8		4.3		5.0		7.0	ns
t _{RCO}	Data Valid After Clock HIGH/LOW		3.4		3.8		4.3		5.0		7.0	ns
t _{ADSU}	Address/Data Set-Up Time		1.6		1.8		2.0		2.4		3.4	ns
Synchronous SRAM Operations (continued)												
t _{ADH}	Address/Data Hold Time		0.0		0.0		0.0		0.0		0.0	ns
t _{RENSU}	Read Enable Set-Up		0.6		0.7		0.8		0.9		1.3	ns
t _{RENH}	Read Enable Hold		3.4		3.8		4.3		5.0		7.0	ns
t _{WENSU}	Write Enable Set-Up		2.7		3.0		3.4		4.0		5.6	ns
t _{WENH}	Write Enable Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{BENS}	Block Enable Set-Up		2.8		3.1		3.5		4.1		5.7	ns
t _{BENH}	Block Enable Hold		0.0		0.0		0.0		0.0		0.0	ns

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description	–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{ACO} Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.9		12.1		13.7		16.1		22.5	ns
d _{TLH} Capacitive Loading, LOW to HIGH		0.10		0.11		0.12		0.14		0.20	ns/pF
d _{THL} Capacitive Loading, HIGH to LOW		0.10		0.11		0.12		0.14		0.20	ns/pF
CMOS Output Module Timing⁵											
t _{DLH} Data-to-Pad HIGH		4.9		5.5		6.2		7.3		10.3	ns
t _{DHL} Data-to-Pad LOW		3.4		3.8		4.3		5.1		7.1	ns
t _{ENZH} Enable Pad Z to HIGH		3.7		4.1		4.7		5.5		7.7	ns
t _{ENZL} Enable Pad Z to LOW		4.1		4.6		5.2		6.1		8.5	ns
t _{ENHZ} Enable Pad HIGH to Z		7.4		8.2		9.3		10.9		15.3	ns
t _{ENLZ} Enable Pad LOW to Z		6.9		7.6		8.7		10.2		14.3	ns
t _{GLH} G-to-Pad HIGH		7.0		7.8		8.9		10.4		14.6	ns
t _{GHL} G-to-Pad LOW		7.0		7.8		8.9		10.4		14.6	ns
t _{LSU} I/O Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t _{LH} I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO} I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.9		8.8		10.0		11.8		16.5	ns

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

3.12 Pin Descriptions

This section lists the pin descriptions for 40MX and 42MX series FPGAs.

CLK/A/B, I/O Global Clock

Clock inputs for clock distribution networks. CLK is for 40MX while CLKA and CLKB are for 42MX devices. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK, I/O Diagnostic Clock

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND, Ground

Input LOW supply voltage.

I/O, Input/Output

Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
21	CLKA, I/O	CLKA, I/O	CLKA, I/O
22	I/O	I/O	I/O
23	PRA, I/O	PRA, I/O	PRA, I/O
24	NC	I/O	WD, I/O
25	I/O	I/O	WD, I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	NC	I/O	I/O
29	I/O	I/O	WD, I/O
30	GND	GND	GND
31	NC	I/O	WD, I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	VCCI	VCCI
36	I/O	I/O	WD, I/O
37	I/O	I/O	WD, I/O
38	SDI, I/O	SDI, I/O	SDI, I/O
39	I/O	I/O	I/O
40	GND	GND	GND
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	GND	GND	GND
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	NC	I/O	I/O
53	I/O	I/O	I/O
54	NC	VCCA	VCCA
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	VCCA	VCCA	VCCA

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
169	I/O	WD, I/O	WD, I/O
170	I/O	I/O	I/O
171	NC	I/O	QCLKD, I/O
172	I/O	I/O	I/O
173	I/O	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	I/O	WD, I/O	WD, I/O
177	I/O	WD, I/O	WD, I/O
178	PRA, I/O	PRA, I/O	PRA, I/O
179	I/O	I/O	I/O
180	CLKA, I/O	CLKA, I/O	CLKA, I/O
181	NC	I/O	I/O
182	NC	VCCI	VCCI
183	VCCA	VCCA	VCCA
184	GND	GND	GND
185	I/O	I/O	I/O
186	CLKB, I/O	CLKB, I/O	CLKB, I/O
187	I/O	I/O	I/O
188	PRB, I/O	PRB, I/O	PRB, I/O
189	I/O	I/O	I/O
190	I/O	WD, I/O	WD, I/O
191	I/O	WD, I/O	WD, I/O
192	I/O	I/O	I/O
193	NC	I/O	I/O
194	NC	WD, I/O	WD, I/O
195	NC	WD, I/O	WD, I/O
196	I/O	I/O	QCLKC, I/O
197	NC	I/O	I/O
198	I/O	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	NC	I/O	I/O
202	VCCI	VCCI	VCCI
203	I/O	WD, I/O	WD, I/O
204	I/O	WD, I/O	WD, I/O
205	I/O	I/O	I/O

Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
47	I/O	I/O	TDI, I/O
48	I/O	I/O	I/O
49	I/O	I/O	WD, I/O
50	I/O	I/O	WD, I/O
51	I/O	I/O	I/O
52	NC	VCCI	VCCI
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	NC	I/O	WD, I/O
56	I/O	I/O	WD, I/O
57	NC	NC	I/O
58	I/O	I/O	I/O
59	I/O	I/O	WD, I/O
60	I/O	I/O	WD, I/O
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65	I/O	I/O	I/O
66	NC	I/O	I/O
67	GND	GND	GND
68	VCCA	VCCA	VCCA
69	I/O	I/O	WD, I/O
70	I/O	I/O	WD, I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	NC	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	NC	NC	WD, I/O
78	NC	I/O	WD, I/O
79	I/O	I/O	I/O
80	NC	I/O	I/O
81	I/O	I/O	I/O
82	NC	VCCI	VCCI
83	I/O	I/O	I/O

Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
158	CLKB, I/O	CLKB, I/O	CLKB, I/O
159	I/O	I/O	I/O
160	PRB, I/O	PRB, I/O	PRB, I/O
161	NC	I/O	WD, I/O
162	I/O	I/O	WD, I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	NC	NC	WD, I/O
166	NC	I/O	WD, I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	I/O	I/O	I/O
170	NC	VCCI	VCCI
171	I/O	I/O	WD, I/O
172	I/O	I/O	WD, I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	DCLK, I/O	DCLK, I/O	DCLK, I/O
176	I/O	I/O	I/O

Figure 49 • CQ208

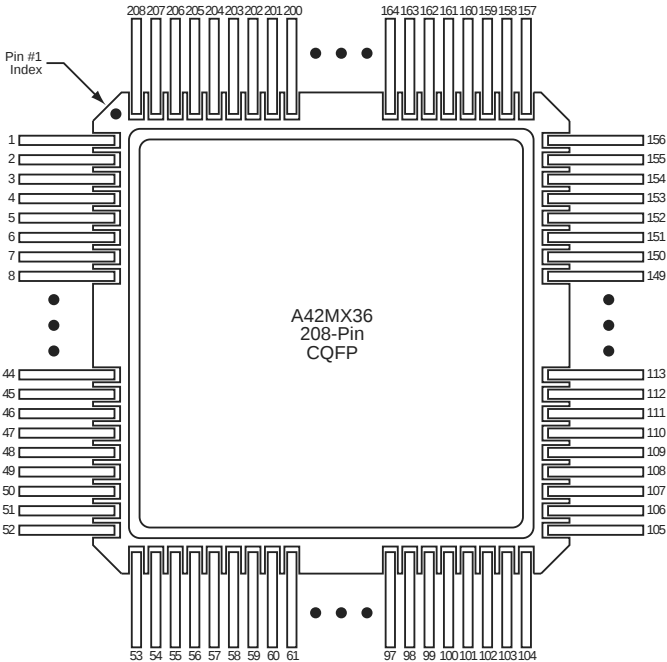


Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
59	I/O
60	VCCA
61	GND
62	GND
63	NC
64	NC
65	NC
66	I/O
67	SDO, TDO, I/O
68	I/O
69	WD, I/O
70	WD, I/O
71	I/O
72	VCCI
73	I/O
74	I/O
75	I/O
76	WD, I/O
77	GND
78	WD, I/O
79	I/O
80	QCLKB, I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	WD, I/O
88	WD, I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	VCCI

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
207	I/O
208	I/O
209	QCLKC, I/O
210	I/O
211	WD, I/O
212	WD, I/O
213	I/O
214	I/O
215	WD, I/O
216	WD, I/O
217	I/O
218	PRB, I/O
219	I/O
220	CLKB, I/O
221	I/O
222	GND
223	GND
224	VCCA
225	VCCI
226	I/O
227	CLKA, I/O
228	I/O
229	PRA, I/O
230	I/O
231	I/O
232	WD, I/O
233	WD, I/O
234	I/O
235	I/O
236	I/O
237	I/O
238	I/O
239	I/O
240	QCLKD, I/O
241	I/O
242	WD, I/O
243	GND