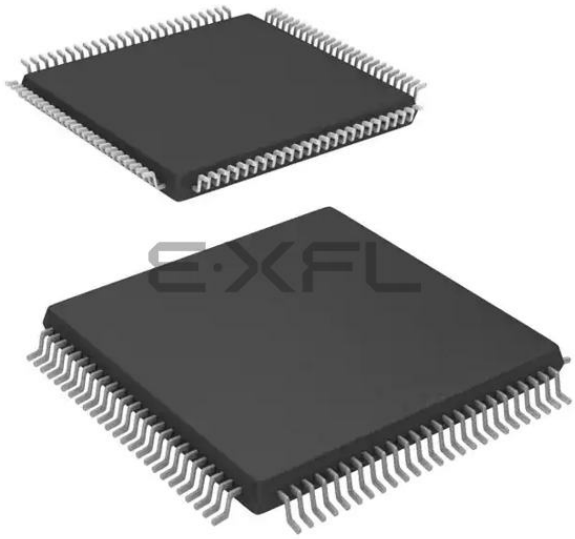

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

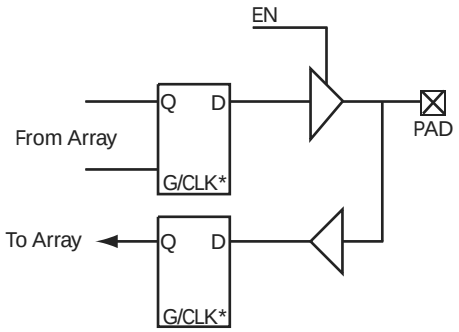
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	83
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx16-vq100a

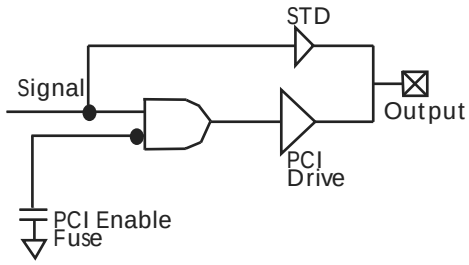
Designer software development tools provide a design library of I/O macro functions that can implement all I/O configurations supported by the MX FPGAs.

Figure 10 • **42MX I/O Module**



Note: **Can be configured as a Latch or D Flip-Flop (Using C-Module)*

Figure 11 • **PCI Output Structure of A42MX24 and A42MX36 Devices**



3.3 Other Architectural Features

The following sections cover other architectural features of 40MX and 42MX FPGAs.

3.3.1 Performance

MX devices can operate with internal clock frequencies of 250 MHz, enabling fast execution of complex logic functions. MX devices are live on power-up and do not require auxiliary configuration devices and thus are an optimal platform to integrate the functionality contained in multiple programmable logic devices. In addition, designs that previously would have required a gate array to meet performance can be integrated into an MX device with improvements in cost and time-to-market. Using timing-driven place-and-route (TDPR) tools, designers can achieve highly deterministic device performance.

3.3.2 User Security

Microsemi FuseLock provides robust security against design theft. Special security fuses are hidden in the fabric of the device and protect against unauthorized users attempting to access the programming and/or probe interfaces. It is virtually impossible to identify or bypass these fuses without damaging the device, making Microsemi antifuse FPGAs protected with the highest level of security available from both invasive and noninvasive attacks.

Special security fuses in 40MX devices include the Probe Fuse and Program Fuse. The former disables the probing circuitry while the latter prohibits further programming of all fuses, including the Probe Fuse. In 42MX devices, there is the Security Fuse which, when programmed, both disables the probing circuitry and prohibits further programming of the device.

3.3.3 Programming

Device programming is supported through the Silicon Sculptor series of programmers. Silicon Sculptor is a compact, robust, single-site and multi-site device programmer for the PC. With standalone software, Silicon Sculptor is designed to allow concurrent programming of multiple units from the same PC.

Figure 22 • **AC Test Loads**

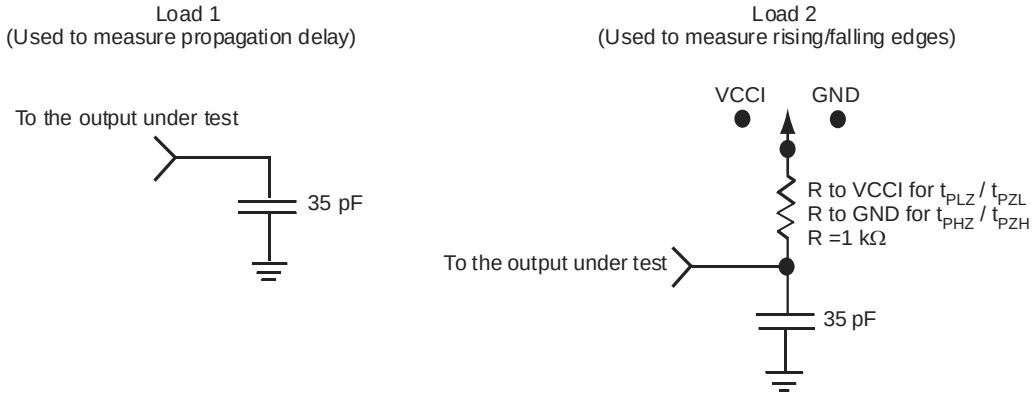


Figure 23 • **Input Buffer Delays**

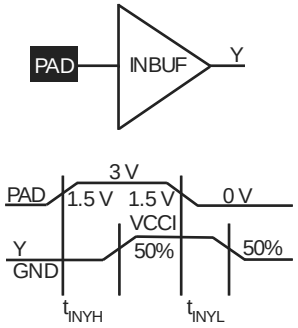


Figure 24 • **Module Delays**

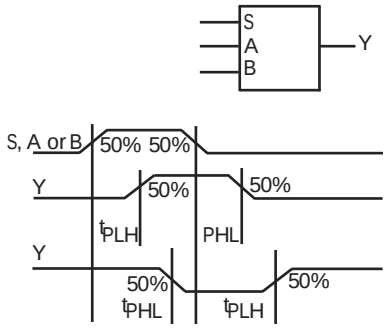
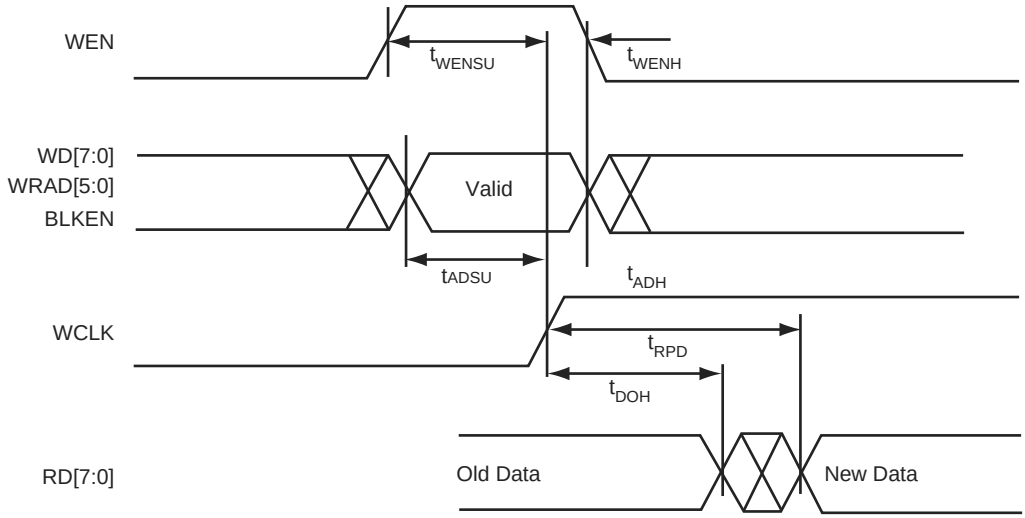


Figure 33 • **42MX SRAM Asynchronous Read Operation—Type 2 (Write Address Controlled)**



3.10.7 Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution, which is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi's patented antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 µm lithography, offer nominal levels of 100 Ω resistance and 7.0 fF capacitance per antifuse.

MX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90 percent of interconnects using only two antifuses.

3.11 Timing Characteristics

Device timing characteristics fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all MX devices. Internal routing delays are device-dependent; actual delays are not determined until after place-and-route of the user's design is complete. Delay values may then be determined by using the Designer software utility or by performing simulation with post-layout delays.

3.11.1 Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment in Microsemi's Designer software prior to placement and routing. Up to 6% of the nets in a design may be designated as critical.

3.11.2 Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks add

Table 34 • **A40MX02 Timing Characteristics (Nominal 5.0 V Operation) *(continued)***
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			0.7		0.8		0.9		1.1		1.5	ns
t_{INYL}	Pad-to-Y LOW			0.6		0.7		0.8		1.0		1.3	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO = 1 Routing Delay			2.1		2.4		2.2		3.2		4.5	ns
t_{IRD2}	FO = 2 Routing Delay			2.6		3.0		3.4		4.0		5.6	ns
t_{IRD3}	FO = 3 Routing Delay			3.1		3.6		4.1		4.8		6.7	ns
t_{IRD4}	FO = 4 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t_{IRD8}	FO = 8 Routing Delay			5.7		6.6		7.5		8.8		12.4	ns
Global Clock Network													
t_{CKH}	Input Low to HIGH	FO = 16		4.6		5.3		6.0		7.0		9.8	ns
		FO = 128		4.6		5.3		6.0		7.0		9.8	
t_{CKL}	Input High to LOW	FO = 16		4.8		5.6		6.3		7.4		10.4	ns
		FO = 128		4.8		5.6		6.3		7.4		10.4	
t_{PWH}	Minimum Pulse Width HIGH	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.1		3.6		5.1		
t_{PWL}	Minimum Pulse Width LOW	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.01		3.6		5.1		
t_{CKSW}	Maximum Skew	FO = 16		0.4		0.5		0.5		0.6		0.8	ns
		FO = 128		0.5		0.6		0.7		0.8		1.2	
t_P	Minimum Period	FO = 16	4.7		5.4		6.1		7.2		10.0		ns
		FO = 128	4.8		5.6		6.3		7.5		10.4		
f_{MAX}	Maximum Frequency	FO = 16		188		175		160		139		83	MHz
		FO = 128		181		168		154		134		80	

Table 35 • **A40MX02 Timing Characteristics (Nominal 3.3 V Operation) *(continued)***
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_P	Minimum Period	FO = 16	6.5		7.5		8.5		10.1		14.1		ns
		FO = 128	6.8		7.8		8.9		10.4		14.6		
f_{MAX}	Maximum Frequency	FO = 16		113		105		96		83		50	MHz
		FO = 128		109		101		92		80		48	
TTL Output Module Timing[4]													
t_{DLH}	Data-to-Pad HIGH			4.7		5.4		6.1		7.2		10.0	ns
t_{DHL}	Data-to-Pad LOW			5.6		6.4		7.3		8.6		12.0	ns
t_{ENZH}	Enable Pad Z to HIGH			5.2		6.0		6.8		8.1		11.3	ns
t_{ENZL}	Enable Pad Z to LOW			6.6		7.6		8.6		10.1		14.1	ns
t_{ENHZ}	Enable Pad HIGH to Z			11.1		12.8		14.5		17.1		23.9	ns
t_{ENLZ}	Enable Pad LOW to Z			8.2		9.5		10.7		12.6		17.7	ns
d_{TLH}	Delta LOW to HIGH			0.03		0.03		0.04		0.04		0.06	ns/pF
d_{THL}	Delta HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF

Table 35 • **A40MX02 Timing Characteristics (Nominal 3.3 V Operation) *(continued)***
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[4]												
t_{DLH}	Data-to-Pad HIGH		5.5		6.4		7.2		8.5		11.9	ns
t_{DHL}	Data-to-Pad LOW		4.8		5.5		6.2		7.3		10.2	ns
t_{ENZH}	Enable Pad Z to HIGH		4.7		5.5		6.2		7.3		10.2	ns
t_{ENZL}	Enable Pad Z to LOW		6.8		7.9		8.9		10.5		14.7	ns
t_{ENHZ}	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9	ns
t_{ENLZ}	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7	ns
d_{TLH}	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro
4. Delays based on 35 pF loading

Table 36 • **A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t_{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t_{PD2}	Dual-Module Macros		2.3		3.1		3.5		4.1		5.7	ns
t_{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays[1]												
t_{RD1}	FO = 1 Routing Delay		1.2		1.6		1.8		2.1		3.0	ns
t_{RD2}	FO = 2 Routing Delay		1.9		2.2		2.5		2.9		4.1	ns
t_{RD3}	FO = 3 Routing Delay		2.4		2.8		3.2		3.7		5.2	ns
t_{RD4}	FO = 4 Routing Delay		2.9		3.4		3.9		4.5		6.3	ns
t_{RD8}	FO = 8 Routing Delay		5.0		5.8		6.6		7.8		10.9	ns
Logic Module Sequential Timing[2]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	3.1		3.5		4.0		4.7		6.6		ns

Table 38 • **A42MX09 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.5		4.9		5.6		6.6		9.2		ns
t_A	Flip-Flop Clock Input Period	3.5		3.8		4.3		5.1		7.1		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Set-Up	0.3		0.3		0.4		0.4		0.6		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.3		0.3		0.4		0.4		0.6		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		268		244		224		195		117	MHz

Table 39 • **A42MX09 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RD4}	FO = 4 Routing Delay		1.9		2.1		2.4		2.9		4.0	ns
t_{RD8}	FO = 8 Routing Delay		3.2		3.6		4.1		4.8		6.7	ns
Logic Module Sequential Timing [3, 4]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.5		0.5		0.6		0.7		0.9		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.7		5.3		6.0		7.0		9.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.2		6.9		7.8		9.2		12.9		ns
t_A	Flip-Flop Clock Input Period	5.0		5.6		6.2		7.1		9.9		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		161		146		135		117		70	MHz

Table 43 • **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Sequential Timing[3, 4]												
t_{CO}	Flip-Flop Clock-to-Output		2.1		2.0		2.3		2.7		3.7	ns
t_{GO}	Latch Gate-to-Output		3.4		1.9		2.1		2.5		3.4	ns
t_{SUD}	Flip-Flop (Latch) Set-Up Time	0.4		0.5		0.6		0.7		0.9		ns
t_{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		2.0		2.2		2.5		2.9		4.1	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.2		5.8		6.9		9.6		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.1		6.8		7.7		9.0		12.6		ns
Input Module Propagation Delays												
t_{INPY}	Input Data Pad-to-Y		1.4		1.6		1.8		2.2		3.0	ns
t_{INGO}	Input Latch Gate-to-Output		1.8		1.9		2.2		2.6		3.6	ns
t_{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t_{ILA}	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

Table 44 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		3.5		3.9		4.5		5.2		7.3	ns
t_{DHL}	Data-to-Pad LOW		2.5		2.7		3.1		3.6		5.1	ns
t_{ENZH}	Enable Pad Z to HIGH		2.7		3.0		3.3		3.9		5.5	ns
t_{ENZL}	Enable Pad Z to LOW		2.9		3.3		3.7		4.3		6.1	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.3		5.8		6.6		7.8		10.9	ns
t_{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t_{GLH}	G-to-Pad HIGH		5.0		5.6		6.3		7.5		10.4	ns
t_{GHL}	G-to-Pad LOW		5.0		5.6		6.3		7.5		10.4	ns
t_{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 45 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Combinatorial Functions[1]												
t_{PD}	Internal Array Module Delay		1.9		2.1		2.3		2.7		3.8	ns
t_{PDD}	Internal Decode Module Delay		2.2		2.5		2.8		3.3		4.7	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.7	ns
t_{RD2}	FO = 2 Routing Delay		1.8		2.0		2.3		2.7		3.7	ns
t_{RD3}	FO = 3 Routing Delay		2.3		2.5		2.8		3.4		4.7	ns
t_{RD4}	FO = 4 Routing Delay		2.8		3.1		3.5		4.1		5.7	ns

Table 45 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RD5}	FO = 8 Routing Delay		4.6		5.2		5.8		6.9		9.6	ns
t_{RDD}	Decode-to-Output Routing Delay		0.5		0.5		0.6		0.7		1.0	ns
Logic Module Sequential Timing[3, 4]												
t_{CO}	Flip-Flop Clock-to-Output		1.8		2.0		2.3		2.7		3.7	ns
t_{GO}	Latch Gate-to-Output		1.8		2.0		2.3		2.7		3.7	ns
t_{SUD}	Flip-Flop (Latch) Set-Up Time	0.4		0.5		0.6		0.7		0.9		ns
t_{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		2.2		2.4		2.7		3.2		4.5	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	1.0		1.1		1.2		1.4		2.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.2		5.8		6.9		9.6		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.1		6.8		7.7		9.0		12.6		ns
Synchronous SRAM Operations												
t_{RC}	Read Cycle Time	9.5		10.5		11.9		14.0		19.6		ns
t_{WC}	Write Cycle Time	9.5		10.5		11.9		14.0		19.6		ns
t_{RCKHL}	Clock HIGH/LOW Time	4.8		5.3		6.0		7.0		9.8		ns
t_{RCO}	Data Valid After Clock HIGH/LOW		4.8		5.3		6.0		7.0		9.8	ns
t_{ADSU}	Address/Data Set-Up Time	2.3		2.5		2.8		3.4		4.8		ns

Table 45 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations (continued)												
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Set-Up	0.9		1.0		1.1		1.3		1.8		ns
t_{RENH}	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t_{WENSU}	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Set-Up	3.9		4.3		4.9		5.7		8.0		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations												
t_{RPD}	Asynchronous Access Time		11.3		12.6		14.3		16.8		23.5	ns
t_{RDADV}	Read Address Valid	12.3		13.7		15.5		18.2		25.5		ns
t_{ADSU}	Address/Data Set-Up Time	2.3		2.5		2.8		3.4		4.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RENSUA}	Read Enable Set-Up to Address Valid	0.9		1.0		1.1		1.3		1.8		ns
t_{RENHA}	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t_{WENSU}	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.8		2.0		2.1		2.5		3.5	ns
Input Module Propagation Delays												
t_{INPY}	Input Data Pad-to-Y		1.4		1.6		1.8		2.1		3.0	ns
t_{INGO}	Input Latch Gate-to-Output		2.0		2.2		2.5		2.9		4.1	ns
t_{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t_{ILA}	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

Table 49 • **PL84**

PL84				
Pin Number	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
47	I/O	I/O	I/O	WD, I/O
48	I/O	I/O	I/O	I/O
49	I/O	GND	GND	GND
50	I/O	I/O	I/O	WD, I/O
51	I/O	I/O	I/O	WD, I/O
52	I/O	SDO, I/O	SDO, I/O	SDO, TDO, I/O
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	GND	I/O	I/O	I/O
61	GND	I/O	I/O	I/O
62	I/O	I/O	I/O	TCK, I/O
63	I/O	LP	LP	LP
64	CLK, I/O	VCCA	VCCA	VCCA
65	I/O	VCCI	VCCI	VCCI
66	MODE	I/O	I/O	I/O
67	VCC	I/O	I/O	I/O
68	VCC	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	GND	GND	GND
71	I/O	I/O	I/O	I/O
72	SDI, I/O	I/O	I/O	I/O
73	DCLK, I/O	I/O	I/O	I/O
74	PRA, I/O	I/O	I/O	I/O
75	PRB, I/O	I/O	I/O	I/O
76	I/O	SDI, I/O	SDI, I/O	SDI, I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	WD, I/O
79	I/O	I/O	I/O	WD, I/O
80	I/O	I/O	I/O	WD, I/O
81	I/O	PRA, I/O	PRA, I/O	PRA, I/O
82	GND	I/O	I/O	I/O
83	I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O

Table 54 • **PQ240**

PQ240	
Pin Number	**A42MX36 Function**
89	VCCI
90	VCCA
91	LP
92	TCK, I/O
93	I/O
94	GND
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	VCCI
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	VCCA
119	GND
120	GND
121	GND
122	I/O
123	SDO, TDO, I/O
124	I/O
125	WD, I/O

Table 54 • **PQ240**

PQ240	
Pin Number	**A42MX36 Function**
163	WD, I/O
164	WD, I/O
165	I/O
166	QCLKA, I/O
167	I/O
168	I/O
169	I/O
170	I/O
171	I/O
172	VCCI
173	I/O
174	WD, I/O
175	WD, I/O
176	I/O
177	I/O
178	TDI, I/O
179	TMS, I/O
180	GND
181	VCCA
182	GND
183	I/O
184	I/O
185	I/O
186	I/O
187	I/O
188	I/O
189	I/O
190	I/O
191	I/O
192	VCCI
193	I/O
194	I/O
195	I/O
196	I/O
197	I/O
198	I/O
199	I/O

Figure 47 • **VQ100**

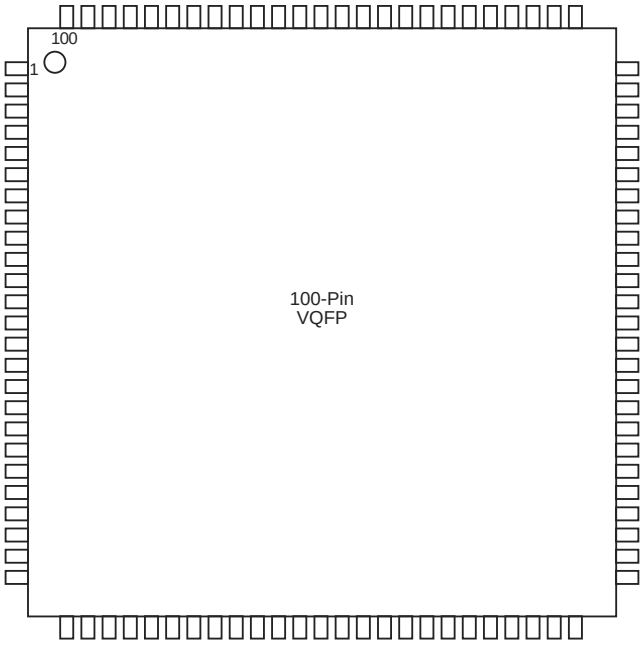


Table 56 • **VQ100**

VQ100		
Pin Number	**A42MX09 Function**	**A42MX16 Function**
1	I/O	I/O
2	MODE	MODE
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	GND
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	VCCA	NC
15	VCCI	VCCI
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	GND	GND

Table 57 • **TQ176**

TQ176			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
84	I/O	I/O	WD, I/O
85	I/O	I/O	WD, I/O
86	NC	I/O	I/O
87	SDO, I/O	SDO, I/O	SDO, TDO, I/O
88	I/O	I/O	I/O
89	GND	GND	GND
90	I/O	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	NC	NC	I/O
102	I/O	I/O	I/O
103	NC	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	GND	GND	GND
107	NC	I/O	I/O
108	NC	I/O	TCK, I/O
109	LP	LP	LP
110	VCCA	VCCA	VCCA
111	GND	GND	GND
112	VCCI	VCCI	VCCI
113	VCCA	VCCA	VCCA
114	NC	I/O	I/O
115	NC	I/O	I/O
116	NC	VCCA	VCCA
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
Y13	I/O
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	WD, I/O
Y19	GND
Y20	GND

Figure 52 • **PG132**

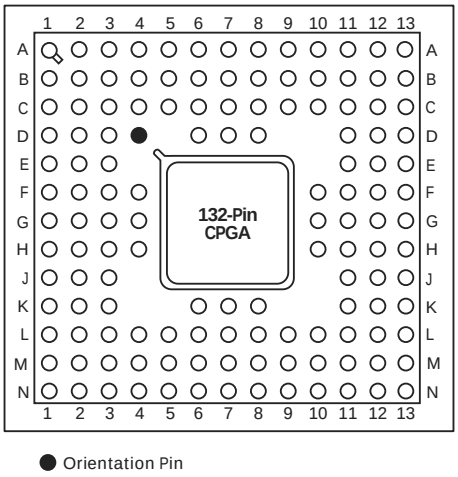


Table 61 • **PG132**

PG132	
Pin Number	**A42MX09 Function**
–	PMPOUT
B2	I/O
A1	MODE
B1	I/O
D3	I/O
C2	I/O
C1	I/O
D2	I/O
D1	I/O
E2	I/O
E1	I/O
F3	I/O

Table 61 • **PG132**

PG132	
Pin Number	**A42MX09 Function**
B3	I/O
A2	I/O
C3	DCLK
B5	GNDA
E12	GNDA
J2	GNDA
M9	GNDA
B9	GNDI
C5	GNDI
E11	GNDI
F4	GNDI
J3	GNDI
J11	GNDI
L5	GNDI
L9	GNDI
C9	GNDQ
E3	GNDQ
K12	GNDQ
D7	VCCA
G3	VCCA
G10	VCCA
L7	VCCA
C7	VCCI
G2	VCCI
G11	VCCI
K7	VCCI

Table 62 • **CQ172**

138	I/O
139	I/O
140	I/O
141	GND
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	PROBA
149	I/O
150	CLKA
151	VCC
152	GND
153	I/O
154	CLKB
155	I/O
156	PROBB
157	I/O
158	I/O
159	I/O
160	I/O
161	GND
162	I/O
163	I/O
164	I/O
165	I/O
166	VCCI
167	I/O
168	I/O
169	I/O
170	I/O
171	DCLK