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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	72
Number of Gates	36000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx24-1plg84

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2.4 Plastic Device Resources

Table 2 • Plastic Device Resources

Device	User I/Os											
	PLCC 44-Pin	PLCC 68-Pin	PLCC 84-Pin	PQFP 100-Pin	PQFP 144- Pin	PQFP 160-Pin	PQFP 208- Pin	PQFP 240-Pin	VQFP 80-Pin	VQFP 100- Pin	TQFP 176- Pin	PBGA 272- Pin
A40MX02	34	57	–	57	–	–	–	–	57	–	–	–
A40MX04	34	57	69	69	–	–	–	–	69	–	–	–
A42MX09	–	–	72	83	95	101	–	–	–	83	104	–
A42MX16	–	–	72	83	–	125	140	–	–	83	140	–
A42MX24	–	–	72	–	–	125	176	–	–	–	150	–
A42MX36	–	–	–	–	–	–	176	202	–	–	–	202

Note: Package Definitions: PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array

2.5 Ceramic Device Resources

Table 3 • Ceramic Device Resources

Device	User I/Os			
	CPGA 132-Pin	CQFP 172-Pin	CQFP 208-Pin	CQFP 256-Pin
A42MX09	95			
A42MX16		131		
A42MX36			176	202

Note: Package Definitions: CQFP = Ceramic Quad Flat Pack

3 40MX and 42MX FPGAs

3.1 General Description

Microsemi's 40MX and 42MX families offer a cost-effective design solution at 5V. The MX devices are single-chip solutions and provide high performance while shortening the system design and development cycle. MX devices can integrate and consolidate logic implemented in multiple PALs, CPLDs, and FPGAs. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

The MX device architecture is based on Microsemi's patented antifuse technology implemented in a 0.45µm triple-metal CMOS process. With capacities ranging from 3,000 to 54,000 system gates, the MX devices provide performance up to 250 MHz, are live on power-up and have one-fifth the standby power consumption of comparable FPGAs. MX FPGAs provide up to 202 user I/Os and are available in a wide variety of packages and speed grades.

A42MX24 and A42MX36 devices also feature multiPlex I/Os, which support mixed-voltage systems, enable programmable PCI, deliver high-performance operation at both 5.0V and 3.3V, and provide a low-power mode. The devices are fully compliant with the PCI local bus specification (version 2.1). They deliver 200 MHz on-chip operation and 6.1 ns clock-to-output performance.

The 42MX24 and 42MX36 devices include system-level features such as IEEE Standard 1149.1 (JTAG) Boundary Scan Testing and fast wide-decode modules. In addition, the A42MX36 device offers dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The storage elements can efficiently address applications requiring wide data path manipulation and can perform transformation functions such as those required for telecommunications, networking, and DSP.

All MX devices are fully tested over automotive and military temperature ranges. In addition, the largest member of the family, the A42MX36, is available in both CQ208 and CQ256 ceramic packages screened to MIL-STD-883 levels. For easy prototyping and conversion from plastic to ceramic, the CQ208 and PQ208 devices are pin-compatible.

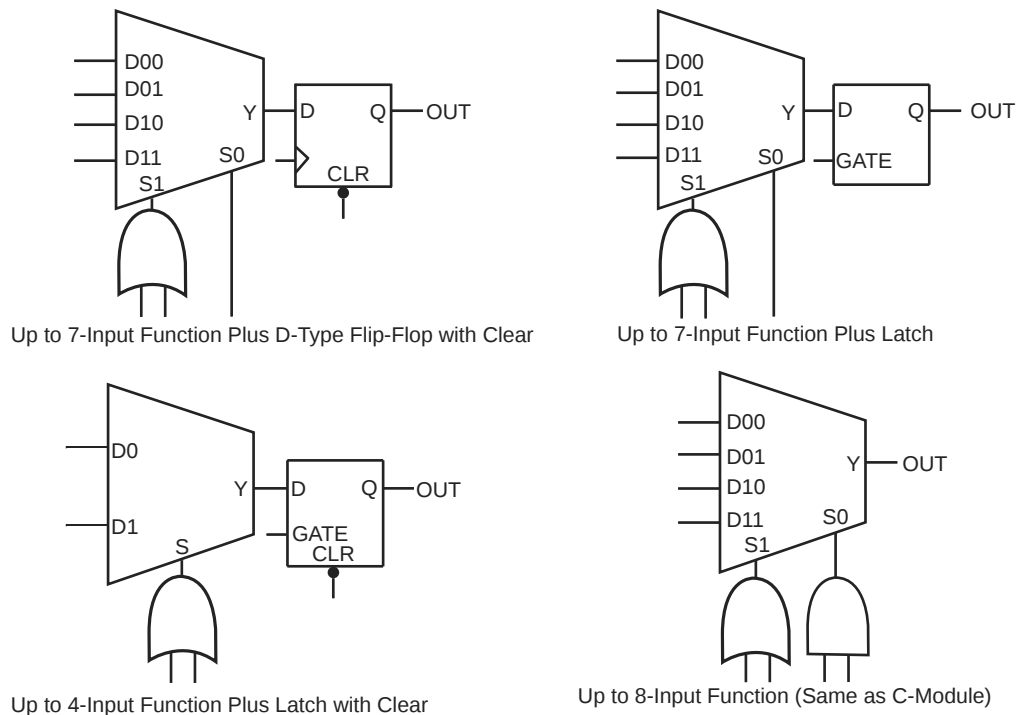
3.2 MX Architectural Overview

The MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within these families are composed of logic modules, I/O modules, routing resources and clock networks, which are the building blocks for fast logic designs. In addition, the A42MX36 device contains embedded dual-port SRAM modules, which are optimized for high-speed data path functions such as FIFOs, LIFOs and scratch pad memory. A42MX24 and A42MX36 also contain wide-decode modules.

3.2.1 Logic Modules

The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources.(see the following figure).

The logic module can implement the four basic logic functions (NAND, AND, OR and NOR) in gates of two, three, or four inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array; latches and flip-flops can be constructed from logic modules whenever required in the application.

Figure 4 • 42MX S-Module Implementation

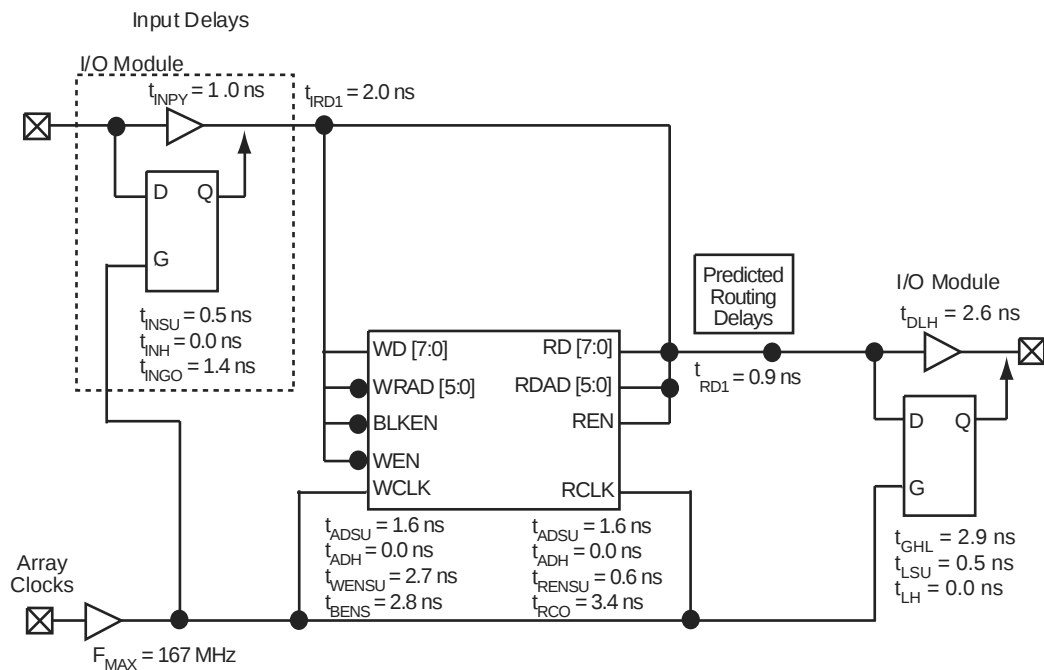
A42MX24 and A42MX36 devices contain D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry, providing a fast, wide-input AND function similar to that found in CPLD architectures (Figure 5, page 9). The D-module allows A42MX24 and A42MX36 devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin, and can also be fed back into the array to be incorporated into other logic.

3.2.2 Dual-Port SRAM Modules

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the A42MX36 dual-port SRAM block is shown in Figure 6, page 9.

The A42MX36 SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]), which are connected to segmented vertical routing tracks.

The A42MX36 dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring FIFO and LIFO queues. The ACTgen Macro Builder within Microsemi's designer software provides capability to quickly design memory functions with the SRAM blocks. Unused SRAM blocks can be used to implement registers for other user logic within the design.

Figure 20 • 42MX Timing Model (SRAM Functions)

Note: Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions.

3.10.1 Parameter Measurement

The following figures show parameter measurement details.

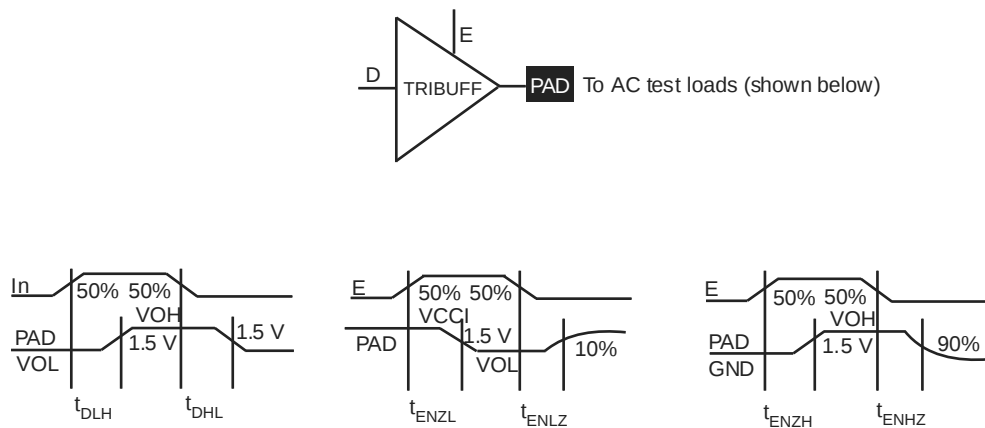
Figure 21 • Output Buffer Delays

Table 33 • Timing Parameters for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{SU(PTP)}$	Input Set-Up Time to CLK—Point-to-Point	10, 12 ²	—	1.5	—	1.5	—	ns
t_H	Input Hold to CLK	0	—	0	—	0	—	ns

1. TOFF is system dependent. MX PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.
2. REQ# and GNT# are point-to-point signals and have different output valid delay and input setup times than do bussed signals. GNT# has a setup of 10; REW# has a setup of 12.

3.11.6.1 Timing Characteristics

The following tables list the timing characteristics.

Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation)
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t _{PD2}	Dual-Module Macros		2.7		3.1		3.5		4.1		5.7	ns
t _{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays ¹												
t _{RD1}	FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.8	ns
t _{RD2}	FO = 2 Routing Delay		1.8		2.1		2.4		2.8		3.9	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.7		3.0		3.6		5.0	ns
t _{RD4}	FO = 4 Routing Delay		2.9		3.3		3.7		4.4		6.1	ns
t _{RD8}	FO = 8 Routing Delay		4.9		5.7		6.5		7.6		10.6	ns
Logic Module Sequential Timing ²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t _A	Flip-Flop Clock Input Period	4.8		5.6		6.3		7.5		10.4		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		181		168		154		134		80	MHz

Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t _{INYH}	Pad-to-Y HIGH			1.0		1.2		1.3		1.6		2.2	ns
t _{INYL}	Pad-to-Y LOW			0.8		0.9		1.0		1.2		1.7	ns
t _{INGH}	G to Y HIGH			1.3		1.4		1.6		1.9		2.7	ns
t _{INGL}	G to Y LOW			1.3		1.4		1.6		1.9		2.7	ns
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay			2.0		2.2		2.5		3.0		4.2	ns
t _{IRD2}	FO = 2 Routing Delay			2.3		2.5		2.9		3.4		4.7	ns
t _{IRD3}	FO = 3 Routing Delay			2.5		2.8		3.2		3.7		5.2	ns
t _{IRD4}	FO = 4 Routing Delay			2.8		3.1		3.5		4.1		5.7	ns
t _{IRD8}	FO = 8 Routing Delay			3.7		4.1		4.7		5.5		7.7	ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32		2.4		2.7		3.0		3.6		5.0	ns
		FO = 256		2.7		3.0		3.4		4.0		5.5	ns
t _{CKL}	Input HIGH to LOW	FO = 32		3.5		3.9		4.4		5.2		7.3	ns
		FO = 256		3.9		4.3		4.9		5.7		8.0	ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t _{CKSW}	Maximum Skew	FO = 32		0.3		0.3		0.4		0.5		0.6	ns
		FO = 256		0.3		0.3		0.4		0.5		0.6	ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	2.3		2.6		3.0		3.5		4.9		ns
		FO = 256	2.2		2.4		3.3		3.9		5.5		ns
t _P	Minimum Period	FO = 32	3.4		3.7		4.0		4.7		7.8		ns
		FO = 256	3.7		4.1		4.5		5.2		8.6		ns
f _{MAX}	Maximum Frequency	FO = 32		296		269		247		215		129	MHz
		FO = 256		268		244		224		195		117	MHz

Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		2.5		2.7		3.1		3.6		5.1	ns
t _{DHL}	Data-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t _{ENZH}	Enable Pad Z to HIGH		2.6		2.9		3.3		3.9		5.5	ns
t _{ENZL}	Enable Pad Z to LOW		2.9		3.2		3.7		4.3		6.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		4.9		5.4		6.2		7.3		10.2	ns
t _{ENLZ}	Enable Pad LOW to Z		5.3		5.9		6.7		7.9		11.1	ns
t _{GLH}	G-to-Pad HIGH		2.6		2.9		3.3		3.8		5.3	ns
t _{GHL}	G-to-Pad LOW		2.6		2.9		3.3		3.8		5.3	ns
t _{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.2		5.8		6.6		7.7		10.8	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.4		8.2		9.3		10.9		15.3	ns
d _{TLH}	Capacity Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF
d _{THL}	Capacity Loading, HIGH to LOW		0.04		0.04		0.04		0.05		0.07	ns/pF

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		3.5		3.9		4.5		5.2		7.3	ns
t _{DHL}	Data-to-Pad LOW		2.5		2.7		3.1		3.6		5.1	ns
t _{ENZH}	Enable Pad Z to HIGH		2.7		3.0		3.3		3.9		5.5	ns
t _{ENZL}	Enable Pad Z to LOW		2.9		3.3		3.7		4.3		6.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		5.3		5.8		6.6		7.8		10.9	ns
t _{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t _{GLH}	G-to-Pad HIGH		5.0		5.6		6.3		7.5		10.4	ns
t _{GHL}	G-to-Pad LOW		5.0		5.6		6.3		7.5		10.4	ns
t _{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions ¹												
t _{PD}	Internal Array Module Delay		1.9		2.1		2.3		2.7		3.8	ns
t _{PDD}	Internal Decode Module Delay		2.2		2.5		2.8		3.3		4.7	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.7	ns
t _{RD2}	FO = 2 Routing Delay		1.8		2.0		2.3		2.7		3.7	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.5		2.8		3.4		4.7	ns
t _{RD4}	FO = 4 Routing Delay		2.8		3.1		3.5		4.1		5.7	ns

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay		2.8		3.1		3.5		4.1		5.7		ns
t _{IRD2}	FO = 2 Routing Delay		3.2		3.5		4.1		4.8		6.7		ns
t _{IRD3}	FO = 3 Routing Delay		3.7		4.1		4.7		5.5		7.7		ns
t _{IRD4}	FO = 4 Routing Delay		4.2		4.6		5.3		6.2		8.7		ns
t _{IRD8}	FO = 8 Routing Delay		6.1		6.8		7.7		9.0		12.6		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32	4.6		5.1		5.7		6.7		9.3		ns
		FO = 635	5.0		5.6		6.3		7.4		10.3		ns
t _{CKL}	Input HIGH to LOW	FO = 32	5.3		5.9		6.7		7.8		11.0		ns
		FO = 635	6.8		7.6		8.6		10.1		14.1		ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	2.5		2.7		3.1		3.6		5.1		ns
		FO = 635	2.8		3.1		3.5		4.1		5.7		ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	2.5		2.7		3.1		3.6		5.1		ns
		FO = 635	2.8		3.1		3.5		4.1		5.7		ns
t _{CKSW}	Maximum Skew	FO = 32	1.0		1.2		1.3		1.5		2.2		ns
		FO = 635	1.0		1.2		1.3		1.5		2.2		ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 635	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	4.0		4.4		5.0		5.9		8.2		ns
		FO = 635	4.6		5.2		5.9		6.9		9.6		ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	9.2		10.2		11.1		12.7		21.2		ns
		FO = 635	9.9		11.0		12.0		13.8		23.0		ns
f _{MAX}	Maximum Datapath Frequency	FO = 32	108		98		90		79		47		MHz
		FO = 635	100		91		83		73		44		MHz
TTL Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH		3.6		4.0		4.5		5.3		7.4		ns
t _{DHL}	Data-to-Pad LOW		4.2		4.6		5.2		6.2		8.6		ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.2		4.7		5.5		7.7		ns
t _{ENZL}	Enable Pad Z to LOW		4.1		4.6		5.2		6.1		8.5		ns
t _{ENHZ}	Enable Pad HIGH to Z		7.34		8.2		9.3		10.9		15.3		ns
TTL Output Module Timing ⁵													
t _{ENLZ}	Enable Pad LOW to Z		6.9		7.6		8.7		10.2		14.3		ns
t _{GLH}	G-to-Pad HIGH		4.9		5.5		6.2		7.3		10.2		ns
t _{GHL}	G-to-Pad LOW		4.9		5.5		6.2		7.3		10.2		ns
t _{LSU}	I/O Latch Output Set-Up		0.7		0.7		0.8		1.0		1.4		ns
t _{LH}	I/O Latch Output Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.9		8.8		10.0		11.8		16.5		ns

Input, output, tristate or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/Os pins are configured by the Designer software as shown in Table 46, page 84.

Table 46 • Configuration of Unused I/Os

Device	Configuration
A40MX02, A40MX04	Pulled LOW
A42MX09, A42MX16	Pulled LOW
A42MX24, A42MX36	Tristated

In all cases, it is recommended to tie all unused MX I/O pins to LOW on the board. This applies to all dual-purpose pins when configured as I/Os as well.

LP, Low Power Mode

Controls the low power mode of all 42MX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation in 200 μ s after the LP pin is driven to a logic LOW.

MODE, Mode

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). The MODE pin is held HIGH to provide verification capability. The MODE pin should be terminated to GND through a 10k Ω resistor so that the MODE pin can be pulled HIGH when required.

NC, No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O

PRB, I/OProbe A/B

The Probe pin is used to output data from any user-defined design node within the device. Each diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. The Probe pin is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

QCLKA/B/C/D, I/O Quadrant Clock

Quadrant clock inputs for A42MX36 devices. When not used as a register control signal, these pins can function as user I/Os.

SDI, I/O Serial Data Input

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDO, I/O Serial Data Output

Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. SDO is available for 42MX devices only.

When Silicon Explorer II is being used, SDO will act as an output while the "checksum" command is run. It will return to user I/O when "checksum" is complete.

TCK, I/O Test Clock

Table 48 • PL68

PL68		
Pin Number	A40MX02 Function	A40MX04 Function
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	GND	GND
67	I/O	I/O
68	I/O	I/O

Figure 40 • PL84

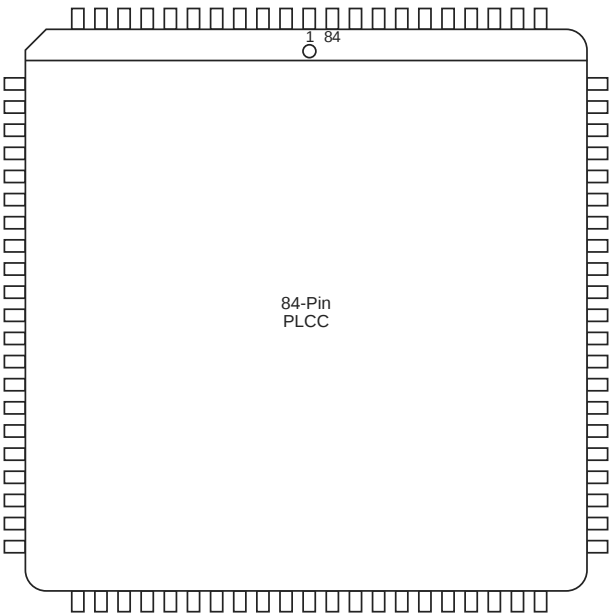
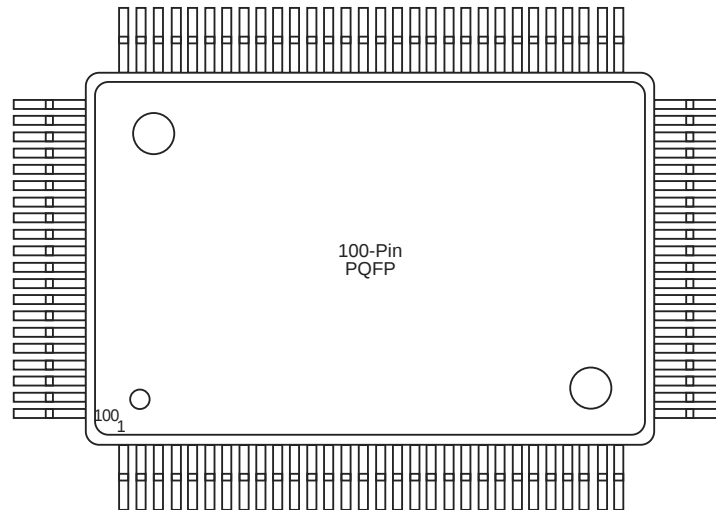


Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	I/O	I/O	I/O	I/O
2	I/O	CLKB, I/O	CLKB, I/O	CLKB, I/O
3	I/O	I/O	I/O	I/O
4	VCC	PRB, I/O	PRB, I/O	PRB, I/O
5	I/O	I/O	I/O	WD, I/O
6	I/O	GND	GND	GND
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	WD, I/O
9	I/O	I/O	I/O	WD, I/O

Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
84	I/O	VCCA	VCCA	VCCA

Figure 41 • PQ100**Table 50 • PQ 100**

PQ100				
Pin Number	A40MX02 Function	A40MX04 Function	A42MX09 Function	A42MX16 Function
1	NC	NC	I/O	I/O
2	NC	NC	DCLK, I/O	DCLK, I/O
3	NC	NC	I/O	I/O
4	NC	NC	MODE	MODE
5	NC	NC	I/O	I/O
6	PRB, I/O	PRB, I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	GND	GND
10	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O
13	GND	GND	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	VCCA	VCCA
17	I/O	I/O	VCCI	VCCA
18	I/O	I/O	I/O	I/O

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
132	VCCI	VCCI	VCCI
133	VCCA	VCCA	VCCA
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	VCCA	VCCA	VCCA
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	I/O	I/O	I/O
146	NC	I/O	I/O
147	NC	I/O	I/O
148	NC	I/O	I/O
149	NC	I/O	I/O
150	GND	GND	GND
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	I/O	I/O	I/O
156	I/O	I/O	I/O
157	GND	GND	GND
158	I/O	I/O	I/O
159	SDI, I/O	SDI, I/O	SDI, I/O
160	I/O	I/O	I/O
161	I/O	WD, I/O	WD, I/O
162	I/O	WD, I/O	WD, I/O
163	I/O	I/O	I/O
164	VCCI	VCCI	VCCI
165	NC	I/O	I/O
166	NC	I/O	I/O
167	I/O	I/O	I/O
168	I/O	WD, I/O	WD, I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
15	QCLKC, I/O
16	I/O
17	WD, I/O
18	WD, I/O
19	I/O
20	I/O
21	WD, I/O
22	WD, I/O
23	I/O
24	PRB, I/O
25	I/O
26	CLKB, I/O
27	I/O
28	GND
29	VCCA
30	VCCI
31	I/O
32	CLKA, I/O
33	I/O
34	PRA, I/O
35	I/O
36	I/O
37	WD, I/O
38	WD, I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	QCLKD, I/O
46	I/O
47	WD, I/O
48	WD, I/O
49	I/O
50	I/O
51	I/O

Table 55 • VQ80

VQ80		
Pin Number	A40MX02 Function	A40MX04 Function
13	VCC	VCC
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	NC	I/O
18	NC	I/O
19	NC	I/O
20	VCC	VCC
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	GND	GND
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	VCC	VCC
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O
41	NC	I/O
42	NC	I/O
43	NC	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	GND	GND
48	I/O	I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
1	GND
2	VCCA
3	MODE
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	VCCA
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	VCCI
29	VCCA
30	I/O
31	I/O
32	VCCA
33	I/O
34	I/O
35	I/O
36	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
170	VCCA
171	I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	I/O
177	I/O
178	I/O
179	I/O
180	GND
181	I/O
182	I/O
183	I/O
184	I/O
185	I/O
186	I/O
187	I/O
188	MODE
189	VCCA
190	GND
191	NC
192	NC
193	NC
194	I/O
195	DCLK, I/O
196	I/O
197	I/O
198	I/O
199	WD, I/O
200	WD, I/O
201	VCCI
202	I/O
203	I/O
204	I/O
205	I/O
206	GND

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
A6	I/O
A7	WD, I/O
A8	WD, I/O
A9	I/O
A10	I/O
A11	CLKA
A12	I/O
A13	I/O
A14	I/O
A15	I/O
A16	WD, I/O
A17	I/O
A18	I/O
A19	GND
A20	GND
B1	GND
B2	GND
B3	DCLK, I/O
B4	I/O
B5	I/O
B6	I/O
B7	WD, I/O
B8	I/O
B9	PRB, I/O
B10	I/O
B11	I/O
B12	WD, I/O
B13	I/O
B14	I/O
B15	WD, I/O
B16	I/O
B17	WD, I/O
B18	I/O
B19	GND
B20	GND
C1	I/O
C2	MODE

Table 62 • CQ172

21	I/O
22	GND
23	VCCI
24	VSV
25	I/O
26	I/O
27	VCC
28	I/O
29	I/O
30	I/O
31	I/O
32	GND
33	I/O
34	I/O
35	I/O
36	I/O
37	GND
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	BININ
45	BINOUT
46	I/O
47	I/O
48	I/O
49	I/O
50	VCCI
51	I/O
52	I/O
53	I/O
54	I/O
55	GND
56	I/O
57	I/O
58	I/O
59	I/O