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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	125
Number of Gates	36000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx24-1pq160m

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- The Transient Current, page 13 is new (SAR 36930).
- Package names were revised according to standards established in *Package Mechanical Drawings* (SAR 34774)

1.7 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document

- In Table 20, page 23, the limits in VI were changed from -0.5 to VCCI + 0.5 to -0.5 to VCCA + 0.5
- In Table 22, page 25, V_{OH} was changed from 3.7 to 2.4 for the min in industrial and military. V_{IH} had V_{CCI} and that was changed to VCCA

1.8 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- The Ease of Integration, page 1 was updated
- The Temperature Grade Offerings, page 5 is new
- The Speed Grade Offerings, page 5 is new
- The General Description, page 6 was updated
- The MultiPlex I/O Modules, page 11 was updated
- The User Security, page 12 was updated
- Table 6, page 13 was updated
- The Power Dissipation, page 14 was updated.
- The Static Power Component, page 14 was updated
- The Equivalent Capacitance, page 15 was updated
- Figure 13, page 17 was updated
- Table 10, page 18 was updated.
- Figure 14, page 18 was updated.
- Table 11, page 19 was updated.

2.6 Temperature Grade Offerings

Table 4 • Temperature Grade Offerings

Package	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PLCC 44	C, I, M	C, I, M				
PLCC 68	C, I, A, M	C, I, M				
PLCC 84		C, I, A, M	C, I, A, M	C, I, M	C, I, M	
PQFP 100	C, I, A, M	C, I, A, M	C, I, A, M	C, I, M		
PQFP 144			C			
PQFP 160			C, I, A, M	C, I, M	C, I, A, M	
PQFP 208				C, I, A, M	C, I, A, M	C, I, A, M
PQFP 240						C, I, A, M
VQFP 80	C, I, A, M	C, I, A, M				
VQFP 100			C, I, A, M	C, I, A, M		
TQFP 176			C, I, A, M	C, I, A, M	C, I, A, M	
PBGA 272						C, I, M
CQFP 172				C, M, B		
CQFP 208						C, M, B
CQFP 256						C, M, B
CPGA 132			C, M, B			

Note: C = Commercial
 I = Industrial
 A = Automotive
 M = Military
 B = MIL-STD-883 Class B

2.7 Speed Grade Offerings

Table 5 • Speed Grade Offerings

	– F	Std	–1	–2	–3
C	P	P	P	P	P
I		P	P	P	P
A		P			
M		P	P		
B		P	P		

Note: See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local *Microsemi Sales representative* for device availability.

3.3.7 Low Power Mode

42MX devices have been designed with a Low Power Mode. This feature, activated with setting the special LP pin to HIGH for a period longer than 800 ns, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when exiting Low Power Mode. I/Os can be driven during LP mode, and clock pins should be driven HIGH or LOW and should not float to avoid drawing current. To exit LP mode, the LP pin must be pulled LOW for over 200 μ s to allow for charge pumps to power up, and device initialization will begin.

3.4 Power Dissipation

The general power consumption of MX devices is made up of static and dynamic power and can be expressed with the following equation.

3.4.1 General Power Equation

$$P = [ICC_{\text{standby}} + ICC_{\text{active}}] \cdot V_{CCI} + I_{OL} \cdot V_{OL} \cdot N + I_{OH} \cdot (V_{CCI} - V_{OH}) \cdot M$$

EQ 1

where:

- ICC_{standby} is the current flowing when no inputs or outputs are changing.
- ICC_{active} is the current flowing due to CMOS switching.
- I_{OL} , I_{OH} are TTL sink/source currents.
- V_{OL} , V_{OH} are TTL level output voltages.
- N equals the number of outputs driving TTL loads to V_{OL} .
- M equals the number of outputs driving TTL loads to V_{OH} .

Accurate values for N and M are difficult to determine because they depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

3.4.2 Static Power Component

The static power due to standby current is typically a small component of the overall power consumption. Standby power is calculated for commercial, worst-case conditions. The static power dissipation by TTL loads depends on the number of outputs driving, and on the DC load current. For instance, a 32-bit bus sinking 4mA at 0.33V will generate 42mW with all outputs driving LOW, and 140mW with all outputs driving HIGH. The actual dissipation will average somewhere in between, as I/Os switch states with time.

3.4.3 Active Power Component

Power dissipation in CMOS devices is usually dominated by the dynamic power dissipation. Dynamic power consumption is frequency-dependent and is a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitances due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

The power dissipated by a CMOS circuit can be expressed by the equation:

$$\text{Power}(\mu\text{W}) = C_{EQ} \cdot V_{CCA}^2 \cdot F(1)$$

EQ 2

where:

- C_{EQ} = Equivalent capacitance expressed in picofarads (pF)

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 14 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCA (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V

Note: * Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

3.7.1 5 V TTL Electrical Specifications

The following tables show 5 V TTL electrical specifications.

Table 15 • 5V TTL Electrical Specifications

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	IOH = –10 mA	2.4		2.4						V
	IOH = –4 mA					3.7		3.7		V
VOL ¹	IOL = 10 mA		0.5		0.5					V
	IOL = 6 mA					0.4		0.4		V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX) ²		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL	VIN = 0.5 V		–10		–10		–10		–10	μA
IIH	VIN = 2.7 V		–10		–10		–10		–10	μA
Input Transition Time, T_R and T_F			500		500		500		500	ns
C _{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC ³	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		20		25		25		25	mA
Low power mode Standby Current	42MX devices only		0.5		ICC – 5.0		ICC – 5.0		ICC – 5.0	mA
IIO, I/O source sink current	Can be derived from the <i>IBIS model</i> (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCC/VCCI = min

2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

3. All outputs unloaded. All inputs = VCC/VCCI or GND

3.8 3.3 V Operating Conditions

The following table shows 3.3 V operating conditions.

Table 16 • Absolute Maximum Ratings for 40MX Devices*

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCC + 0.5	V
VO	Output Voltage	–0.5 to VCC + 0.5	V
t _{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 17 • Absolute Maximum Ratings for 42MX Devices*

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCCI+0.5	V
VO	Output Voltage	–0.5 to VCCI+0.5	V
t _{STG}	Storage Temperature	–65 to +150	°C

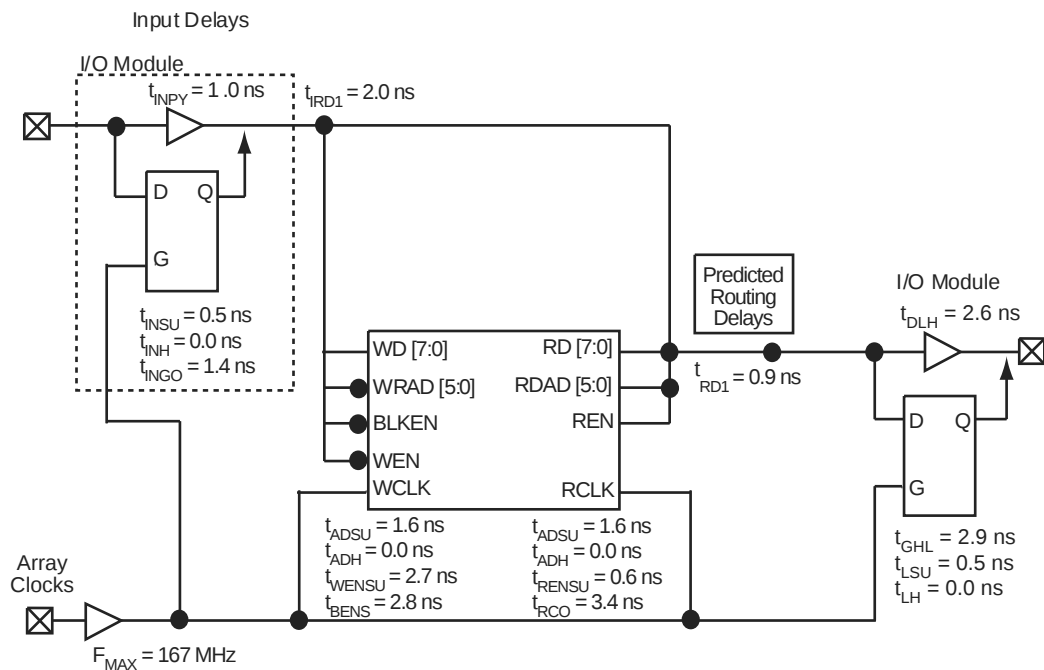
Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 18 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCA (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCI (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

All the following tables show various specifications and operating conditions of 40MX and 42MX FPGAs.

Figure 20 • 42MX Timing Model (SRAM Functions)

Note: Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions.

3.10.1 Parameter Measurement

The following figures show parameter measurement details.

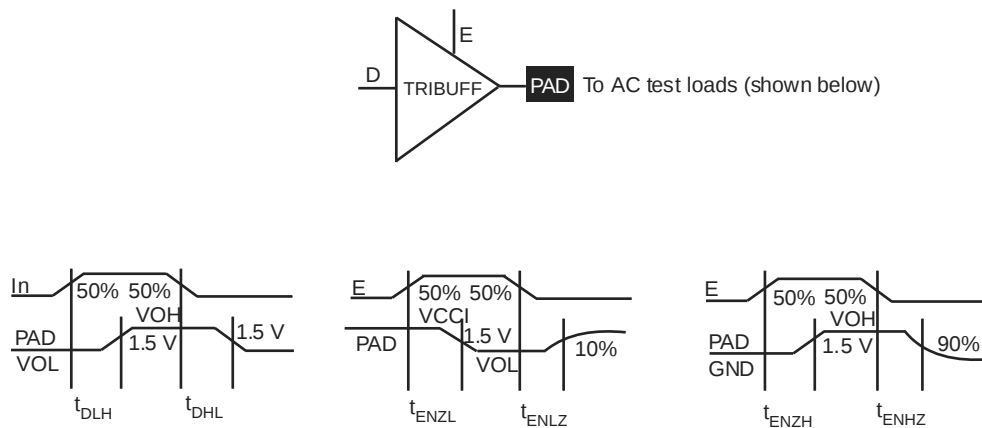
Figure 21 • Output Buffer Delays

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay		2.6		2.9		3.2		3.8		5.3		ns
t _{IRD2}	FO = 2 Routing Delay		2.9		3.2		3.6		4.3		6.0		ns
t _{IRD3}	FO = 3 Routing Delay		3.2		3.6		4.0		4.8		6.6		ns
t _{IRD4}	FO = 4 Routing Delay		3.5		3.9		4.4		5.2		7.3		ns
t _{IRD8}	FO = 8 Routing Delay		4.8		5.3		6.1		7.1		10.0		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32	4.4		4.8		5.5		6.5		9.1		ns
		FO = 486	4.8		5.3		6.0		7.1		10.0		ns
t _{CKL}	Input HIGH to LOW	FO = 32	5.1		5.7		6.4		7.6		10.6		ns
		FO = 486	6.0		6.6		7.5		8.8		12.4		ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	3.0	3.3		3.8		4.5		6.3		ns	
		FO = 486	3.3	3.7		4.2		4.9		6.9		ns	
t _{PWL}	Minimum Pulse Width LOW	FO = 32	3.0	3.4		3.8		4.5		6.3		ns	
		FO = 486	3.3	3.7		4.2		4.9		6.9		ns	
t _{CKSW}	Maximum Skew	FO = 32	0.8		0.8		1.0		1.1		1.6		ns
		FO = 486	0.8		0.8		1.0		1.1		1.6		ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0	0.0		0.0		0.0		0.0		ns	
		FO = 486	0.0	0.0		0.0		0.0		0.0		ns	
TTL Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH		3.4		3.8		4.3		5.0		7.1		ns
t _{DHL}	Data-to-Pad LOW		4.0		4.4		5.0		5.9		8.3		ns
t _{ENZH}	Enable Pad Z to HIGH		3.6		4.0		4.5		5.3		7.4		ns
t _{ENZL}	Enable Pad Z to LOW		3.9		4.4		5.0		5.8		8.2		ns
t _{ENHZ}	Enable Pad HIGH to Z		7.2		8.0		9.1		10.7		14.9		ns
t _{ENLZ}	Enable Pad LOW to Z		6.7		7.5		8.5		9.9		13.9		ns
t _{GLH}	G-to-Pad HIGH		4.8		5.3		6.0		7.2		10.0		ns
t _{GHL}	G-to-Pad LOW		4.8		5.3		6.0		7.2		10.0		ns
t _{LSU}	I/O Latch Output Set-Up		0.7		0.7		0.8		1.0		1.4		ns

Table 47 • PL44

PL44		
Pin Number	A40MX02 Function	A40MX04 Function
21	GND	GND
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	VCC	VCC
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	CLK, I/O	CLK, I/O
34	MODE	MODE
35	VCC	VCC
36	SDI, I/O	SDI, I/O
37	DCLK, I/O	DCLK, I/O
38	PRA, I/O	PRA, I/O
39	PRB, I/O	PRB, I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	GND	GND
44	I/O	I/O

Figure 43 • PQ160

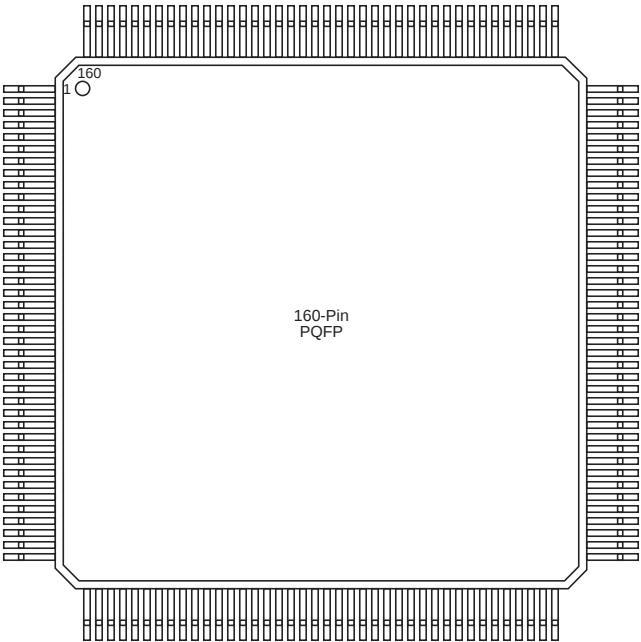


Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	I/O	I/O	I/O
2	DCLK, I/O	DCLK, I/O	DCLK, I/O
3	NC	I/O	I/O
4	I/O	I/O	WD, I/O
5	I/O	I/O	WD, I/O
6	NC	VCCI	VCCI
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	NC	I/O	I/O
11	GND	GND	GND
12	NC	I/O	I/O
13	I/O	I/O	WD, I/O
14	I/O	I/O	WD, I/O
15	I/O	I/O	I/O
16	PRB, I/O	PRB, I/O	PRB, I/O
17	I/O	I/O	I/O
18	CLKB, I/O	CLKB, I/O	CLKB, I/O
19	I/O	I/O	I/O
20	VCCA	VCCA	VCCA

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
58	I/O	WD, I/O	WD, I/O
59	I/O	I/O	I/O
60	VCCI	VCCI	VCCI
61	NC	I/O	I/O
62	NC	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	QCLKA, I/O
66	I/O	WD, I/O	WD, I/O
67	NC	WD, I/O	WD, I/O
68	NC	I/O	I/O
69	I/O	I/O	I/O
70	I/O	WD, I/O	WD, I/O
71	I/O	WD, I/O	WD, I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	GND	GND	GND
79	VCCA	VCCA	VCCA
80	NC	VCCI	VCCI
81	I/O	I/O	I/O
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	WD, I/O	WD, I/O
86	I/O	WD, I/O	WD, I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	NC	I/O	I/O
90	NC	I/O	I/O
91	I/O	I/O	QCLKB, I/O
92	I/O	I/O	I/O
93	I/O	WD, I/O	WD, I/O
94	I/O	WD, I/O	WD, I/O

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
95	NC	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	VCCI	VCCI	VCCI
99	I/O	I/O	I/O
100	I/O	WD, I/O	WD, I/O
101	I/O	WD, I/O	WD, I/O
102	I/O	I/O	I/O
103	SDO, I/O	SDO, TDO, I/O	SDO, TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	VCCA	VCCA
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	NC	I/O	I/O
113	NC	I/O	I/O
114	NC	I/O	I/O
115	NC	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	I/O	I/O	I/O
126	GND	GND	GND
127	I/O	I/O	I/O
128	I/O	TCK, I/O	TCK, I/O
129	LP	LP	LP
130	VCCA	VCCA	VCCA
131	GND	GND	GND

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
163	WD, I/O
164	WD, I/O
165	I/O
166	QCLKA, I/O
167	I/O
168	I/O
169	I/O
170	I/O
171	I/O
172	VCCI
173	I/O
174	WD, I/O
175	WD, I/O
176	I/O
177	I/O
178	TDI, I/O
179	TMS, I/O
180	GND
181	VCCA
182	GND
183	I/O
184	I/O
185	I/O
186	I/O
187	I/O
188	I/O
189	I/O
190	I/O
191	I/O
192	VCCI
193	I/O
194	I/O
195	I/O
196	I/O
197	I/O
198	I/O
199	I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
185	I/O
186	CLKB, I/O
187	I/O
188	PRB, I/O
189	I/O
190	WD, I/O
191	WD, I/O
192	I/O
193	I/O
194	WD, I/O
195	WD, I/O
196	QCLKC, I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	I/O
202	VCCI
203	WD, I/O
204	WD, I/O
205	I/O
206	I/O
207	DCLK, I/O
208	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
96	VCCA
97	GND
98	GND
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	WD, I/O
106	WD, I/O
107	I/O
108	I/O
109	WD, I/O
110	WD, I/O
111	I/O
112	QCLKA, I/O
113	I/O
114	GND
115	I/O
116	I/O
117	I/O
118	I/O
119	VCCI
120	I/O
121	WD, I/O
122	WD, I/O
123	I/O
124	I/O
125	I/O
126	I/O
127	GND
128	NC
129	NC
130	NC
131	GND
132	I/O

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
A6	I/O
A7	WD, I/O
A8	WD, I/O
A9	I/O
A10	I/O
A11	CLKA
A12	I/O
A13	I/O
A14	I/O
A15	I/O
A16	WD, I/O
A17	I/O
A18	I/O
A19	GND
A20	GND
B1	GND
B2	GND
B3	DCLK, I/O
B4	I/O
B5	I/O
B6	I/O
B7	WD, I/O
B8	I/O
B9	PRB, I/O
B10	I/O
B11	I/O
B12	WD, I/O
B13	I/O
B14	I/O
B15	WD, I/O
B16	I/O
B17	WD, I/O
B18	I/O
B19	GND
B20	GND
C1	I/O
C2	MODE

Figure 53 • CQ172

Table 62 • CQ172

CQ172	
Pin Number	A42MX16 Function
1	MODE
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	GND
8	I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	I/O
17	GND
18	I/O
19	I/O
20	I/O

Table 62 • CQ172

138	I/O
139	I/O
140	I/O
141	GND
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	PROBA
149	I/O
150	CLKA
151	VCC
152	GND
153	I/O
154	CLKB
155	I/O
156	PROBB
157	I/O
158	I/O
159	I/O
160	I/O
161	GND
162	I/O
163	I/O
164	I/O
165	I/O
166	VCCI
167	I/O
168	I/O
169	I/O
170	I/O
171	DCLK