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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	125
Number of Gates	36000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx24-2pq160

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Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary-scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

Figure 14 • 42MX IEEE 1149.1 Boundary Scan Circuitry

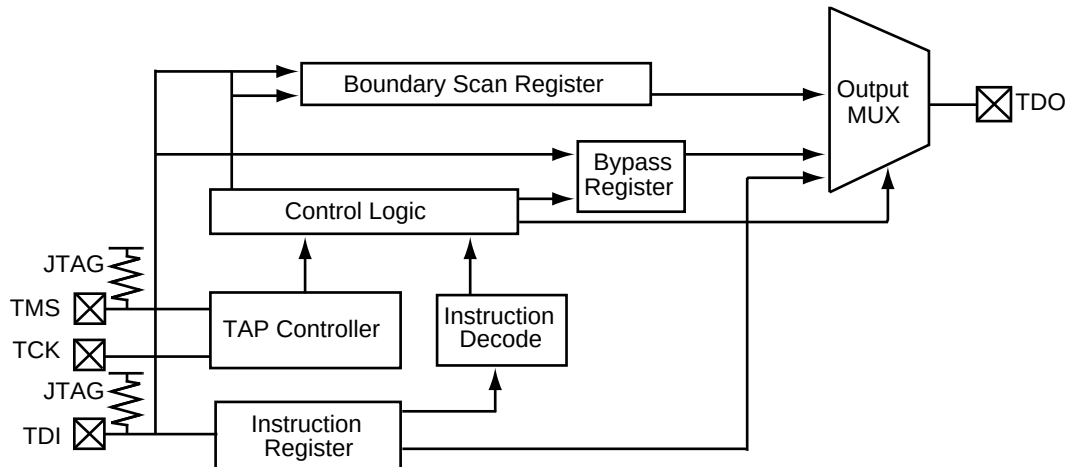


Table 9 • Test Access Port Descriptions

Port	Description
TMS (Test Mode Select)	Serial input for the test logic control bits. Data is captured on the rising edge of the test logic clock (TCK).
TCK (Test Clock Input)	Dedicated test logic clock used serially to shift test instruction, test data, and control inputs on the rising edge of the clock, and serially to shift the output data on the falling edge of the clock. The maximum clock frequency for TCK is 20 MHz.
TDI (Test Data Input)	Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock.
TDO (Test Data Output)	Serial output for test instruction and data from the test logic. TDO is set to an Inactive Drive state (high impedance) when data scanning is not in progress.

Table 10 • Supported BST Public Instructions

Instruction	IR Code (IR2.IR0)	Instruction Type	Description
EXTEST	000	Mandatory	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
SAMPLE/PRELOAD	001	Mandatory	Allows a snapshot of the signals at the device pins to be captured and examined during operation
HIGH Z	101	Optional	Tristates all I/Os to allow external signals to drive pins. See the IEEE Standard 1149.1 specification.
CLAMP	110	Optional	Allows state of signals driven from component pins to be determined from the Boundary-Scan Register. See the IEEE Standard 1149.1 specification for details.
BYPASS	111	Mandatory	Enables the bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the test chain.

3.8.1 3.3 V LVTTTL Electrical Specifications

Table 19 • 3.3V LVTTTL Electrical Specifications

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	IOH = -4 mA	2.15		2.15		2.4		2.4		V
VOL ¹	IOL = 6 mA		0.4		0.4		0.48		0.48	V
VIL		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX)		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL			-10		-10		-10		-10	μA
IIH			-10		-10		-10		-10	μA
Input Transition Time, T _R and T _F			500		500		500		500	ns
C _{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC ²	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		15		25		25		25	mA
Low-Power Mode Standby Current	42MX devices only		0.5		ICC - 5.0		ICC - 5.0		ICC - 5.0	mA
I/O, I/O source sink current	Can be derived from the <i>IBIS model</i> (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCC/VCCI = min.
2. All outputs unloaded. All inputs = VCC/VCCI or GND.

3.9 Mixed 5.0 V / 3.3 V Operating Conditions (for 42MX Devices Only)

Table 20 • Absolute Maximum Ratings*

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	-0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	-0.5 to +7.0	V
VI	Input Voltage	-0.5 to VCCA + 0.5	V
VO	Output Voltage	-0.5 to VCCI + 0.5	V
t _{STG}	Storage Temperature	-65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device

Table 23 • DC Specification (5.0 V PCI Signaling)¹

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
C _{IN}	Input Pin Capacitance			10	—	10	pF
C _{CLK}	CLK Pin Capacitance		5	12	—	10	pF
L _{PIN}	Pin Inductance			20	—	< 8 nH ⁴	nH

1. PCI Local Bus Specification, Version 2.1, Section 4.2.1.1.

2. Maximum rating for VCCI –0.5 V to 7.0 V

3. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V.

4. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

Table 24 • AC Specifications (5.0V PCI Signaling)*

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
ICL	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1) / 0.015$		–60	–10	mA
Slew (r)	Output Rise Slew Rate	0.4 V to 2.4 V load	1	5	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	2.4 V to 0.4 V load	1	5	2.8	4.3	V/ns

Note: *PCI Local Bus Specification, Version 2.1, Section 4.2.1.2.

Figure 22 • AC Test Loads

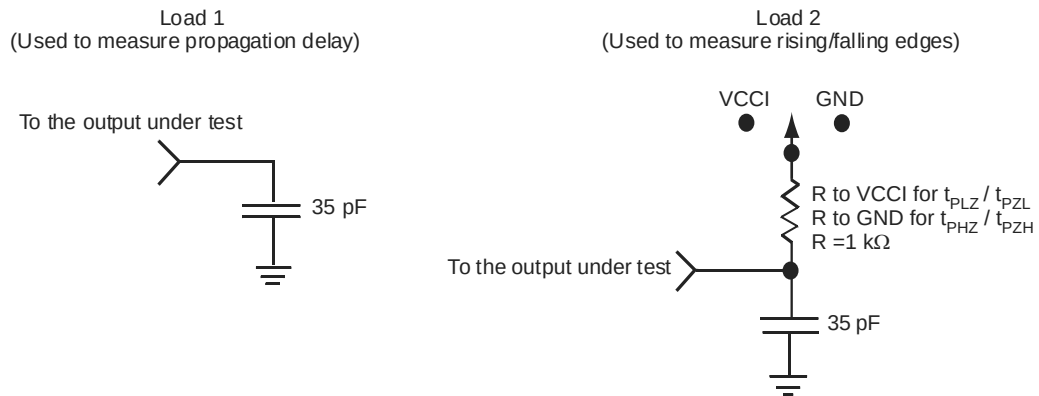


Figure 23 • Input Buffer Delays

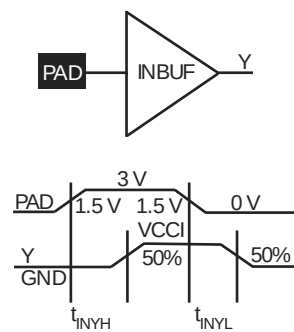
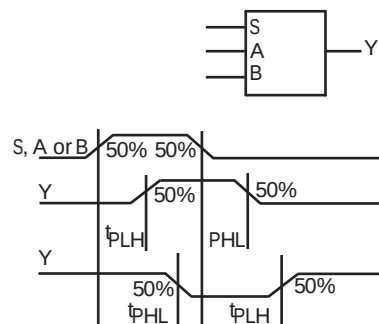


Figure 24 • Module Delays



approximately a 3 ns to a 6 ns delay, which is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section, shown in Table 34, page 41.

3.11.3 Timing Derating

MX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature and worst-case processing.

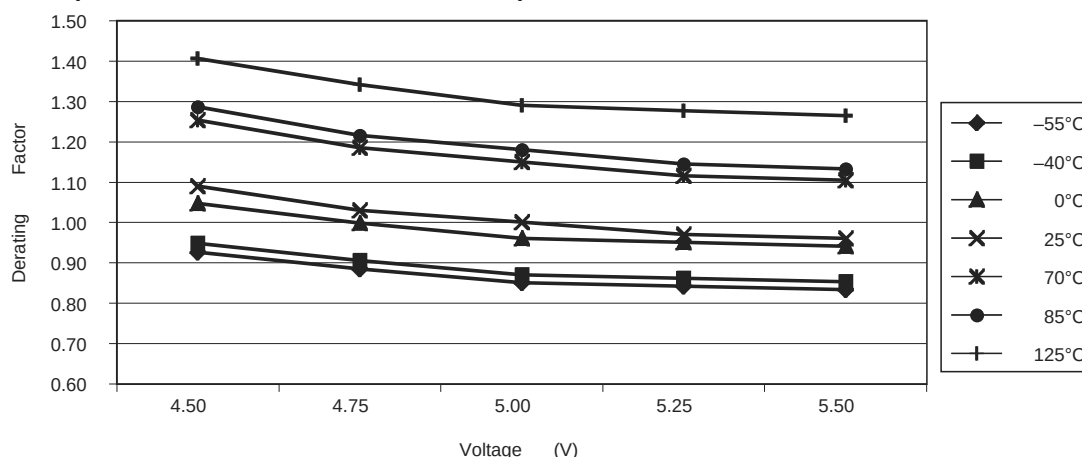
3.11.4 Temperature and Voltage Derating Factors

The following tables and figures show temperature and voltage derating factors for 40MX and 42MX FPGAs.

Table 28 • 42MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 5.0\text{ V}$)

42MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.93	0.95	1.05	1.09	1.25	1.29	1.41
4.75	0.88	0.90	1.00	1.03	1.18	1.22	1.34
5.00	0.85	0.87	0.96	1.00	1.15	1.18	1.29
5.25	0.84	0.86	0.95	0.97	1.12	1.14	1.28
5.50	0.83	0.85	0.94	0.96	1.10	1.13	1.26

Figure 34 • 42MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 5.0\text{ V}$)



Note: This derating factor applies to all routing and propagation delays

Table 29 • 40MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.89	0.93	1.02	1.09	1.25	1.31	1.45
4.75	0.84	0.88	0.97	1.03	1.18	1.24	1.37
5.00	0.82	0.85	0.94	1.00	1.15	1.20	1.33
5.25	0.80	0.82	0.91	0.97	1.12	1.16	1.29
5.50	0.79	0.82	0.90	0.96	1.10	1.15	1.28

Table 33 • Timing Parameters for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{SU(PTP)}$	Input Set-Up Time to CLK—Point-to-Point	10, 12 ²	—	1.5	—	1.5	—	ns
t_H	Input Hold to CLK	0	—	0	—	0	—	ns

1. TOFF is system dependent. MX PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.
2. REQ# and GNT# are point-to-point signals and have different output valid delay and input setup times than do bussed signals. GNT# has a setup of 10; REW# has a setup of 12.

3.11.6.1 Timing Characteristics

The following tables list the timing characteristics.

Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation)
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t _{PD2}	Dual-Module Macros		2.7		3.1		3.5		4.1		5.7	ns
t _{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays ¹												
t _{RD1}	FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.8	ns
t _{RD2}	FO = 2 Routing Delay		1.8		2.1		2.4		2.8		3.9	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.7		3.0		3.6		5.0	ns
t _{RD4}	FO = 4 Routing Delay		2.9		3.3		3.7		4.4		6.1	ns
t _{RD8}	FO = 8 Routing Delay		4.9		5.7		6.5		7.6		10.6	ns
Logic Module Sequential Timing ²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t _A	Flip-Flop Clock Input Period	4.8		5.6		6.3		7.5		10.4		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		181		168		154		134		80	MHz

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		3.3		3.8		4.3		5.0		7.0		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		3.3		3.8		4.3		5.0		7.0		ns
t _A	Flip-Flop Clock Input Period		4.8		5.6		6.3		7.5		10.4		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)			181		167		154		134		80	MHz
Input Module Propagation Delays													
t _{INYH}	Pad-to-Y HIGH			0.7		0.8		0.9		1.1		1.5	ns
t _{INYL}	Pad-to-Y LOW			0.6		0.7		0.8		1.0		1.3	ns
Input Module Predicted Routing Delays ¹													
t _{IRD1}	FO = 1 Routing Delay			2.1		2.4		2.2		3.2		4.5	ns
t _{IRD2}	FO = 2 Routing Delay			2.6		3.0		3.4		4.0		5.6	ns
t _{IRD3}	FO = 3 Routing Delay			3.1		3.6		4.1		4.8		6.7	ns
t _{IRD4}	FO = 4 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t _{IRD8}	FO = 8 Routing Delay			5.7		6.6		7.5		8.8		12.4	ns
Global Clock Network													
t _{CKH}	Input Low to HIGH	FO = 16		4.6		5.3		6.0		7.0		9.8	ns
		FO = 128		4.6		5.3		6.0		7.0		9.8	
t _{CKL}	Input High to LOW	FO = 16		4.8		5.6		6.3		7.4		10.4	ns
		FO = 128		4.8		5.6		6.3		7.4		10.4	
t _{PWH}	Minimum Pulse Width HIGH	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.1		3.6		5.1		
t _{PWL}	Minimum Pulse Width LOW	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.01		3.6		5.1		
t _{CKSW}	Maximum Skew	FO = 16		0.4		0.5		0.5		0.6		0.8	ns
		FO = 128		0.5		0.6		0.7		0.8		1.2	
t _P	Minimum Period	FO = 16	4.7		5.4		6.1		7.2		10.0		ns
		FO = 128	4.8		5.6		6.3		7.5		10.4		
f _{MAX}	Maximum Frequency	FO = 16		188		175		160		139		83	MHz
		FO = 128		181		168		154		134		80	
TTL Output Module Timing ⁴													
t _{DLH}	Data-to-Pad HIGH			3.3		3.8		4.3		5.1		7.2	ns
t _{DHL}	Data-to-Pad LOW			4.0		4.6		5.2		6.1		8.6	ns
t _{ENZH}	Enable Pad Z to HIGH			3.7		4.3		4.9		5.8		8.0	ns
t _{ENZL}	Enable Pad Z to LOW			4.7		5.4		6.1		7.2		10.1	ns
t _{ENHZ}	Enable Pad HIGH to Z			7.9		9.1		10.4		12.2		17.1	ns

Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t _A	Flip-Flop Clock Input Period	6.8		7.8		8.9		10.4		14.6		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		109		101		92		80		48	MHz
Input Module Propagation Delays												
t _{INYH}	Pad-to-Y HIGH		1.0		1.1		1.3		1.5		2.1	ns
t _{INYL}	Pad-to-Y LOW		0.9		1.0		1.1		1.3		1.9	ns

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		2.4		2.7		3.1		3.6		5.1	ns
t _{DHL}	Data-to-Pad LOW		2.8		3.2		3.6		4.2		5.9	ns
t _{ENZH}	Enable Pad Z to HIGH		2.5		2.8		3.2		3.8		5.3	ns
t _{ENZL}	Enable Pad Z to LOW		2.8		3.1		3.5		4.2		5.9	ns
t _{ENHZ}	Enable Pad HIGH to Z		5.2		5.7		6.5		7.6		10.7	ns
t _{ENLZ}	Enable Pad LOW to Z		4.8		5.3		6.0		7.1		9.9	ns
t _{GLH}	G-to-Pad HIGH		2.9		3.2		3.6		4.3		6.0	ns
t _{GHL}	G-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t _{LSU}	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.6		6.1		6.9		8.1		11.4	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.6		11.8		13.4		15.7		22.0	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
80	GNDI
81	NC
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	I/O
88	VKS
89	VPP
90	VCC
91	VCCI
92	NC
93	VSV
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	GND
101	GNDI
102	NC
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	I/O
109	I/O
110	SDI
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	GNDQ

Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
21	CLKA, I/O	CLKA, I/O	CLKA, I/O
22	I/O	I/O	I/O
23	PRA, I/O	PRA, I/O	PRA, I/O
24	NC	I/O	WD, I/O
25	I/O	I/O	WD, I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	NC	I/O	I/O
29	I/O	I/O	WD, I/O
30	GND	GND	GND
31	NC	I/O	WD, I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	VCCI	VCCI
36	I/O	I/O	WD, I/O
37	I/O	I/O	WD, I/O
38	SDI, I/O	SDI, I/O	SDI, I/O
39	I/O	I/O	I/O
40	GND	GND	GND
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	GND	GND	GND
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	NC	I/O	I/O
53	I/O	I/O	I/O
54	NC	VCCA	VCCA
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	VCCA	VCCA	VCCA

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
89	VCCI
90	VCCA
91	LP
92	TCK, I/O
93	I/O
94	GND
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	VCCI
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	VCCA
119	GND
120	GND
121	GND
122	I/O
123	SDO, TDO, I/O
124	I/O
125	WD, I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
126	WD, I/O
127	I/O
128	VCCI
129	I/O
130	I/O
131	I/O
132	WD, I/O
133	WD, I/O
134	I/O
135	QCLKB, I/O
136	I/O
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	WD, I/O
143	WD, I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	VCCI
151	VCCA
152	GND
153	I/O
154	I/O
155	I/O
156	I/O
157	I/O
158	I/O
159	WD, I/O
160	WD, I/O
161	I/O
162	I/O

Table 56 • VQ100

VQ100		
Pin Number	A42MX09 Function	A42MX16 Function
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	VCCA	VCCA
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	GND	GND
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	SDO, I/O	SDO, I/O
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	GND	GND
56	I/O	I/O

Table 56 • VQ100

VQ100		
Pin Number	A42MX09 Function	A42MX16 Function
93	I/O	I/O
94	GND	GND
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	DCLK, I/O	DCLK, I/O

Figure 48 • TQ176

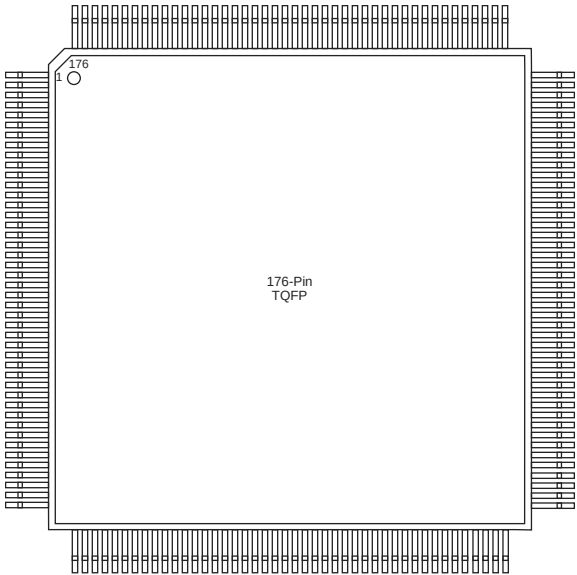


Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	GND	GND	GND
2	MODE	MODE	MODE
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	NC	NC	I/O
9	I/O	I/O	I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	GND
53	GND
54	TMS, I/O
55	TDI, I/O
56	I/O
57	WD, I/O
58	WD, I/O
59	I/O
60	VCCI
61	I/O
62	I/O
63	I/O
64	I/O
65	QCLKA, I/O
66	WD, I/O
67	WD, I/O
68	I/O
69	I/O
70	WD, I/O
71	WD, I/O
72	I/O
73	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
22	I/O
23	I/O
24	I/O
25	I/O
26	VCCA
27	I/O
28	I/O
29	VCCA
30	VCCI
31	GND
32	VCCA
33	LP
34	TCK, I/O
35	I/O
36	GND
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	GND
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O

Figure 53 • CQ172

Table 62 • CQ172

CQ172	
Pin Number	A42MX16 Function
1	MODE
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	GND
8	I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	I/O
17	GND
18	I/O
19	I/O
20	I/O

Table 62 • CQ172

99	I/O
100	I/O
101	I/O
102	I/O
103	GND
104	I/O
105	I/O
106	VKS
107	VPP
108	GND
109	VCCI
110	VSV
111	I/O
112	I/O
113	VCC
114	I/O
115	I/O
116	I/O
117	I/O
118	GND
119	I/O
120	I/O
121	I/O
122	I/O
123	GNDI
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	SDI
132	I/O
133	I/O
134	I/O
135	I/O
136	VCCI
137	I/O