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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 176 |
| Number of Gates | 36000 |
| Voltage - Supply | 3V ~ 3.6V, 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a42mx24-2pq208i |

- The Transient Current, page 13 is new (SAR 36930).
- Package names were revised according to standards established in *Package Mechanical Drawings* (SAR 34774)

## 1.7 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document

- In Table 20, page 23, the limits in VI were changed from -0.5 to VCCI + 0.5 to -0.5 to VCCA + 0.5

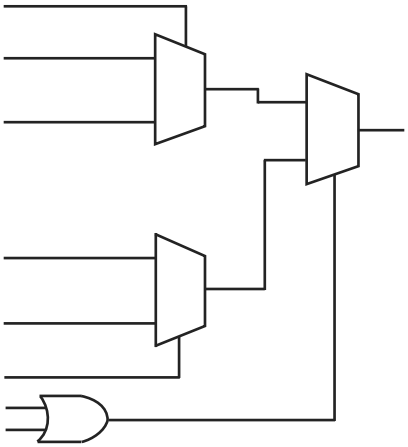
In Table 22, page 25, $V_{OH}$ was changed from 3.7 to 2.4 for the min in industrial and military. $V_{IH}$ had $V_{CCI}$ and that was changed to VCCA

## 1.8 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

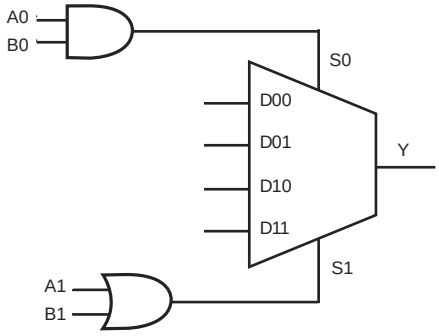
- The Ease of Integration, page 1 was updated
- The Temperature Grade Offerings, page 5 is new
- The Speed Grade Offerings, page 5 is new
- The General Description, page 6 was updated
- The MultiPlex I/O Modules, page 11 was updated
- The User Security, page 12 was updated
- Table 6, page 13 was updated
- The Power Dissipation, page 14 was updated.
- The Static Power Component, page 14 was updated
- The Equivalent Capacitance, page 15 was updated
- Figure 13, page 17 was updated
- Table 10, page 18 was updated.
- Figure 14, page 18 was updated.
- Table 11, page 19 was updated.

***Figure 2 •*** **42MX C-Module Implementation**



The 42MX devices contain three types of logic modules: combinatorial (C-modules), sequential (S-modules) and decode (D-modules). The following figure illustrates the combinatorial logic module. The S-module, shown in Figure 4, page 8, implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D-flip-flop or a transparent latch. The S-module register can be bypassed so that it implements purely combinatorial logic.

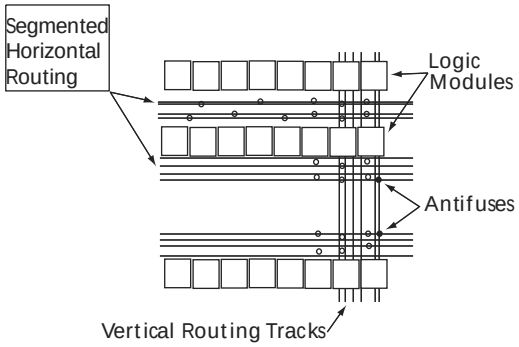
***Figure 3 •*** **42MX C-Module Implementation**



#### 3.2.3.3 Antifuse Structures

An antifuse is a “normally open” structure. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient programming algorithms. There are no pre-existing connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For instance, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

***Figure 7 •*** **MX Routing Structure**




### 3.2.4 Clock Networks

The 40MX devices have one global clock distribution network (CLK). A signal can be put on the CLK network by being routed through the CLKBUF buffer.

In 42MX devices, there are two low-skew, high-fanout clock distribution networks, referred to as CLKA and CLKB. Each network has a clock module (CLKMOD) that can select the source of the clock signal from any of the following (Figure 8, page 11):

- Externally from the CLKA pad, using CLKBUF buffer
- Externally from the CLKB pad, using CLKBUF buffer
- Internally from the CLKINTA input, using CLKINT buffer
- Internally from the CLKINTB input, using CLKINT buffer

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

Clock input pads in both 40MX and 42MX devices can also be used as normal I/Os, bypassing the clock networks.

The A42MX36 device has four additional register control resources, called quadrant clock networks (Figure 9, page 11). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

Silicon Sculptor programs devices independently to achieve the fastest programming times possible. After being programmed, each fuse is verified to insure that it has been programmed correctly. Furthermore, at the end of programming, there are integrity tests that are run to ensure no extra fuses have been programmed. Not only does it test fuses (both programmed and non-programmed), Silicon Sculptor also allows self-test to verify its own hardware extensively.

The procedure for programming an MX device using Silicon Sculptor is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via In-House Programming from the factory.

For more details on programming MX devices, see the *AC225: Programming Antifuse Devices* application note and the *Silicon Sculptor 3 Programmers User Guide*.

## 3.3.4 Power Supply

MX devices are designed to operate in both 5.0V and 3.3V environments. In particular, 42MX devices can operate in mixed 5.0 V/3.3 V systems. The following table describes the voltage support of MX devices.

***Table 6 •*** **Voltage Support of MX Devices**

| Device | VCC | VCCA | VCCI | Maximum Input Tolerance | Nominal Output Voltage |
|---|---|---|---|---|---|
| 40MX | 5.0 V | – | – | 5.5 V | 5.0 V |
| | 3.3 V | – | – | 3.6 V | 3.3 V |
| 42MX | – | 5.0 V | 5.0 V | 5.5 V | 5.0 V |
| | – | 3.3 V | 3.3 V | 3.6 V | 3.3 V |
| | – | 5.0 V | 3.3 V | 5.5 V | 3.3 V |

For A42MX24 and A42MX36 devices the VCCA supply has to be monotonic during power up in order for the POR to issue reset to the JTAG state machine correctly. For more information, see the *AC291: 42MX Family Devices Power-Up Behavior*.

## 3.3.5 Power-Up/Down in Mixed-Voltage Mode

When powering up 42MX in mixed voltage mode (VCCA = 5.0 V and VCCI = 3.3 V), VCCA must be greater than or equal to VCCI throughout the power-up sequence. If VCCI exceeds VCCA during power-up, one of two things will happen:

- The input protection diode on the I/Os will be forward biased
- The I/Os will be at logical High

In either case, ICC rises to high levels. For power-down, any sequence with VCCA and VCCI can be implemented.

## 3.3.6 Transient Current

Due to the simultaneous random logic switching activity during power-up, a transient current may appear on the core supply (VCC). Customers must use a regulator for the VCC supply that can source a minimum of 100 mA for transient current during power-up. Failure to provide enough power can prevent the system from powering up properly and result in functional failure. However, there are no reliability concerns, since transient current is distributed across the die instead of confined to a localized spot.

Since the transient current is not due to I/O switching, its value and duration are independent of the VCCI.

- VCCA = Power supply in volts (V)
- F = Switching frequency in megahertz (MHz)

### 3.4.4 Equivalent Capacitance

Equivalent capacitance is calculated by measuring ICCactive at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

### 3.4.5 $C_{EQ}$ Values for Microsemi MX FPGAs

Modules ($C_{EQM}$)3.5

Input Buffers ($C_{EQI}$)6.9

Output Buffers ($C_{EQO}$)18.2

Routed Array Clock Buffer Loads ($C_{EQCR}$)1.4

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. The equation below shows a piece-wise linear summation over all components.

$$\text{Power} = VCCA^2 * [(m \times C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} +$$
$$0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} +$$
$$0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} (2)]$$

**EQ 3**

where:

m = Number of logic modules switching at frequency $f_m$

n = Number of input buffers switching at frequency $f_n$

p = Number of output buffers switching at frequency $f_p$

$q_1$ = Number of clock loads on the first routed array clock

$q_2$ = Number of clock loads on the second routed array clock

$r_1$ = Fixed capacitance due to first routed array clock

$r_2$ = Fixed capacitance due to second routed array clock

$C_{EQM}$ = Equivalent capacitance of logic modules in pF

$C_{EQI}$ = Equivalent capacitance of input buffers in pF

$C_{EQO}$ = Equivalent capacitance of output buffers in pF

$C_{EQCR}$ = Equivalent capacitance of routed array clock in pF

$C_L$ = Output load capacitance in pF

$f_m$ = Average logic module switching rate in MHz

$f_n$ = Average input buffer switching rate in MHz

$f_p$ = Average output buffer switching rate in MHz

$f_{q1}$ = Average first routed array clock rate in MHz

Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary-scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

***Figure 14 •*** **42MX IEEE 1149.1 Boundary Scan Circuitry**

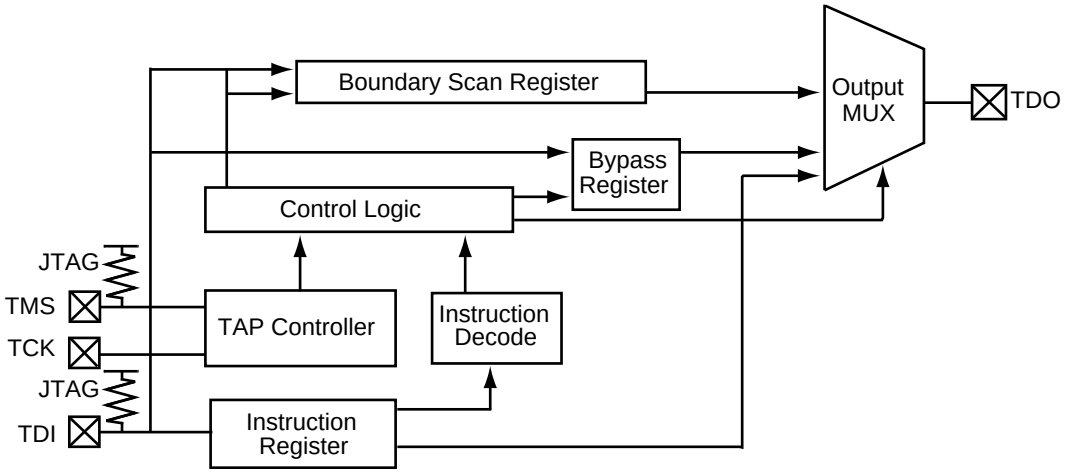



***Table 9 •*** **Test Access Port Descriptions**

| Port | Description |
|---|---|
| TMS (Test Mode Select) | Serial input for the test logic control bits. Data is captured on the rising edge of the test logic clock (TCK). |
| TCK (Test Clock Input) | Dedicated test logic clock used serially to shift test instruction, test data, and control inputs on the rising edge of the clock, and serially to shift the output data on the falling edge of the clock. The maximum clock frequency for TCK is 20 MHz. |
| TDI (Test Data Input) | Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock. |
| TDO (Test Data Output) | Serial output for test instruction and data from the test logic. TDO is set to an Inactive Drive state (high impedance) when data scanning is not in progress. |

***Table 10 •*** **Supported BST Public Instructions**

| Instruction | IR Code (IR2.IR0) | Instruction Type | Description |
|---|---|---|---|
| EXTEST | 000 | Mandatory | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| SAMPLE/PRELOAD | 001 | Mandatory | Allows a snapshot of the signals at the device pins to be captured and examined during operation |
| HIGH Z | 101 | Optional | Tristates all I/Os to allow external signals to drive pins. See the IEEE Standard 1149.1 specification. |
| CLAMP | 110 | Optional | Allows state of signals driven from component pins to be determined from the Boundary-Scan Register. See the IEEE Standard 1149.1 specification for details. |
| BYPASS | 111 | Mandatory | Enables the bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the test chain. |

**Note:** *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

***Table 14 •*** **Recommended Operating Conditions**

| Parameter | Commercial | Industrial | Military | Units |
|---|---|---|---|---|
| Temperature Range* | 0 to +70 | –40 to +85 | –55 to +125 | °C |
| VCC (40MX) | 4.75 to 5.25 | 4.5 to 5.5 | 4.5 to 5.5 | V |
| VCCA (42MX) | 4.75 to 5.25 | 4.5 to 5.5 | 4.5 to 5.5 | V |
| VCCI (42MX) | 4.75 to 5.25 | 4.5 to 5.5 | 4.5 to 5.5 | V |

**Note:** * Ambient temperature ($T_A$) is used for commercial and industrial grades; case temperature ($T_C$) is used for military grades.

## 3.7.1 5 V TTL Electrical Specifications

The following tables show 5 V TTL electrical specifications.

***Table 15 •*** **5V TTL Electrical Specifications**

| | | Commercial | | Commercial -F | | Industrial | | Military | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| VOH[1] | IOH = –10 mA | 2.4 | | 2.4 | | | | | | V |
| | IOH = –4 mA | | | | | 3.7 | | 3.7 | | V |
| VOL[1] | IOL = 10 mA | | 0.5 | | 0.5 | | | | | V |
| | IOL = 6 mA | | | | | | 0.4 | | 0.4 | V |
| VIL | | –0.3 | 0.8 | –0.3 | 0.8 | –0.3 | 0.8 | –0.3 | 0.8 | V |
| VIH (40MX) | | 2.0 | VCC + 0.3 | 2.0 | VCC + 0.3 | 2.0 | VCC + 0.3 | 2.0 | VCC + 0.3 | V |
| VIH (42MX)[2] | | 2.0 | VCCI + 0.3 | 2.0 | VCCI + 0.3 | 2.0 | VCCI + 0.3 | 2.0 | VCCI + 0.3 | V |
| IIL | VIN = 0.5 V | | –10 | | –10 | | –10 | | –10 | µA |
| IIH | VIN = 2.7 V | | –10 | | –10 | | –10 | | –10 | µA |
| Input Transition Time, $T_R$ and $T_F$ | | | 500 | | 500 | | 500 | | 500 | ns |
| $C_{IO}$ I/O Capacitance | | | 10 | | 10 | | 10 | | 10 | pF |
| Standby Current, ICC[3] | A40MX02, A40MX04 | | 3 | | 25 | | 10 | | 25 | mA |
| | A42MX09 | | 5 | | 25 | | 25 | | 25 | mA |
| | A42MX16 | | 6 | | 25 | | 25 | | 25 | mA |
| | A42MX24, A42MX36 | | 20 | | 25 | | 25 | | 25 | mA |
| Low power mode Standby Current | 42MX devices only | | 0.5 | | ICC – 5.0 | | ICC – 5.0 | | ICC – 5.0 | mA |
| IIO, I/O source sink current | Can be derived from the *IBIS model* (http://www.microsemi.com/soc/techdocs/models/ibis.html) | | | | | | | | | |

1. Only one output tested at a time. VCC/VCCI = min
2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

***Table 23 •*** **DC Specification (5.0 V PCI Signaling)[1]**

| | | | PCI | | MX | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Condition** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $C_{IN}$ | Input Pin Capacitance | | | 10 | — | 10 | pF |
| $C_{CLK}$ | CLK Pin Capacitance | | 5 | 12 | — | 10 | pF |
| $L_{PIN}$ | Pin Inductance | | | 20 | — | < 8 nH[4] | nH |

1. PCI Local Bus Specification, Version 2.1, Section 4.2.1.1.
2. Maximum rating for VCCI –0.5 V to 7.0 V
3. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V.
4. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

***Table 24 •*** **AC Specifications (5.0V PCI Signaling)***

| | | | PCI | | MX | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Condition** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| ICL | Low Clamp Current | –5 < VIN ≤ –1 | –25 + (VIN +1) /0.015 | | –60 | –10 | mA |
| Slew (r) | Output Rise Slew Rate | 0.4 V to 2.4 V load | 1 | 5 | 1.8 | 2.8 | V/ns |
| Slew (f) | Output Fall Slew Rate | 2.4 V to 0.4 V load | 1 | 5 | 2.8 | 4.3 | V/ns |

**Note:** *PCI Local Bus Specification, Version 2.1, Section 4.2.1.2.

***Figure 22 •*** **AC Test Loads**

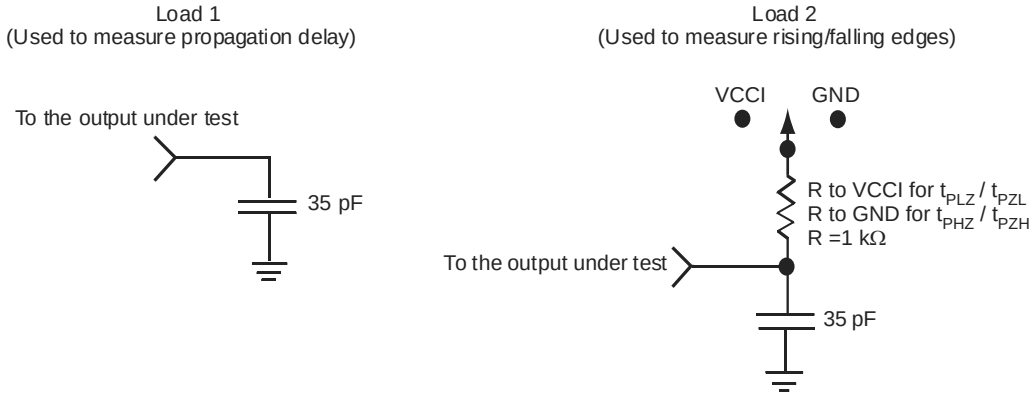



***Figure 23 •*** **Input Buffer Delays**

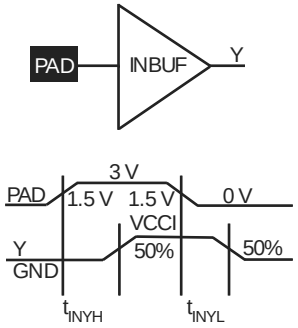



***Figure 24 •*** **Module Delays**

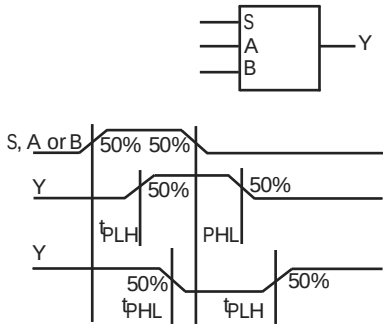


***Table 36 •*** **A40MX04 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.9 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | ns |
| $d_{TLH}$ | Delta LOW to HIGH | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |
| $d_{THL}$ | Delta HIGH to LOW | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.06 | ns/pF |

***Table 37 •*** **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.6 | | 5.3 | | 5.6 | | 7.0 | | 9.8 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.6 | | 5.3 | | 5.6 | | 7.0 | | 9.8 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 6.8 | | 7.8 | | 8.9 | | 10.4 | | 14.6 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency (FO = 128) | | 109 | | 101 | | 92 | | 80 | | 48 | MHz |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INYH}$ | Pad-to-Y HIGH | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{INYL}$ | Pad-to-Y LOW | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.9 | ns |

***Table 38 •*** **A42MX09 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.5 | | 4.9 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 3.5 | | 3.8 | | 4.3 | | 5.1 | | 7.1 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Buffer Latch Set-Up | 0.3 | | 0.3 | | 0.4 | | 0.4 | | 0.6 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTSU}$ | Output Buffer Latch Set-Up | 0.3 | | 0.3 | | 0.4 | | 0.4 | | 0.6 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 268 | | 244 | | 224 | | 195 | | 117 | MHz |

***Table 42 •*** **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INPY}$ | Input Data Pad-to-Y | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{INGO}$ | Input Latch Gate-to-Output | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.6 | ns |
| $t_{INH}$ | Input Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Latch Set-Up | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{ILA}$ | Latch Active Pulse Width | 4.7 | | 5.2 | | 5.9 | | 6.9 | | 9.7 | | ns |

Clock signal to shift the Boundary Scan Test (BST) data into the device. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

**TDI, I/OTest Data In**

Serial data input for BST instructions and data. Data is shifted in on the rising edge of TCK. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

**TDO, I/OTest Data Out**

Serial data output for BST instructions and test data. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

**TMS, I/OTest Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI and TDO pins are boundary scan pins. Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications. IEEE JTAG specification recommends a 10kΩ pull-up resistor on the pin. BST pins are only available in A42MX24 and A42MX36 devices.

**VCC, Supply Voltage**

Input supply voltage for 40MX devices

**VCCA, Supply Voltage**

Supply voltage for array in 42MX devices

**VCCI, Supply Voltage**

Supply voltage for I/Os in 42MX devices

**WD, I/OWide Decode Output**

When a wide decode module is used in a 42MX device this pin can be used as a dedicated output from the wide decode module. This direct connection eliminates additional interconnect delays associated with regular logic modules. To implement the direct I/O connection, connect an output buffer of any type to the output of the wide decode macro and place this output on one of the reserved WD pins.

# 4 Package Pin Assignments

The following figures and tables give the details of the package pin assignments.

***Figure 38 •*** **PL44**

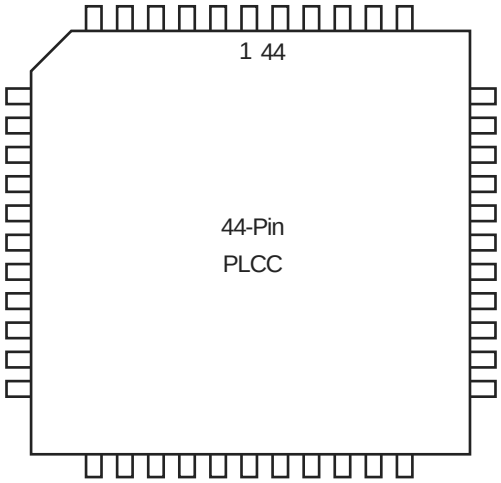



***Table 47 •*** **PL44**

| **PL44** | | |
|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** |
| 1 | I/O | I/O |
| 2 | I/O | I/O |
| 3 | VCC | VCC |
| 4 | I/O | I/O |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | I/O | I/O |
| 8 | I/O | I/O |
| 9 | I/O | I/O |
| 10 | GND | GND |
| 11 | I/O | I/O |
| 12 | I/O | I/O |
| 13 | I/O | I/O |
| 14 | VCC | VCC |
| 15 | I/O | I/O |
| 16 | VCC | VCC |
| 17 | I/O | I/O |
| 18 | I/O | I/O |
| 19 | I/O | I/O |
| 20 | I/O | I/O |

***Table 52 •*** **PQ160**

| **PQ160** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 58 | VCCI | VCCI | VCCI |
| 59 | GND | GND | GND |
| 60 | VCCA | VCCA | VCCA |
| 61 | LP | LP | LP |
| 62 | I/O | I/O | TCK, I/O |
| 63 | I/O | I/O | I/O |
| 64 | GND | GND | GND |
| 65 | I/O | I/O | I/O |
| 66 | I/O | I/O | I/O |
| 67 | I/O | I/O | I/O |
| 68 | I/O | I/O | I/O |
| 69 | GND | GND | GND |
| 70 | NC | I/O | I/O |
| 71 | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O |
| 75 | NC | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | NC | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | NC | I/O | I/O |
| 80 | GND | GND | GND |
| 81 | I/O | I/O | I/O |
| 82 | SDO, I/O | SDO, I/O | SDO, TDO, I/O |
| 83 | I/O | I/O | WD, I/O |
| 84 | I/O | I/O | WD, I/O |
| 85 | I/O | I/O | I/O |
| 86 | NC | VCCI | VCCI |
| 87 | I/O | I/O | I/O |
| 88 | I/O | I/O | WD, I/O |
| 89 | GND | GND | GND |
| 90 | NC | I/O | I/O |
| 91 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |

***Table 52 •*** **PQ160**

| **PQ160** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | WD, I/O |
| 97 | I/O | I/O | I/O |
| 98 | VCCA | VCCA | VCCA |
| 99 | GND | GND | GND |
| 100 | NC | I/O | I/O |
| 101 | I/O | I/O | I/O |
| 102 | I/O | I/O | I/O |
| 103 | NC | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | I/O | I/O | WD, I/O |
| 107 | I/O | I/O | WD, I/O |
| 108 | I/O | I/O | I/O |
| 109 | GND | GND | GND |
| 110 | NC | I/O | I/O |
| 111 | I/O | I/O | WD, I/O |
| 112 | I/O | I/O | WD, I/O |
| 113 | I/O | I/O | I/O |
| 114 | NC | VCCI | VCCI |
| 115 | I/O | I/O | WD, I/O |
| 116 | NC | I/O | WD, I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | TDI, I/O |
| 119 | I/O | I/O | TMS, I/O |
| 120 | GND | GND | GND |
| 121 | I/O | I/O | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | NC | I/O | I/O |
| 125 | GND | GND | GND |
| 126 | I/O | I/O | I/O |
| 127 | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O |
| 129 | NC | I/O | I/O |
| 130 | GND | GND | GND |
| 131 | I/O | I/O | I/O |

***Table 54 •*** **PQ240**

| **PQ240** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 237 | GND |
| 238 | MODE |
| 239 | VCCA |
| 240 | GND |

***Figure 46 •*** **VQ80**

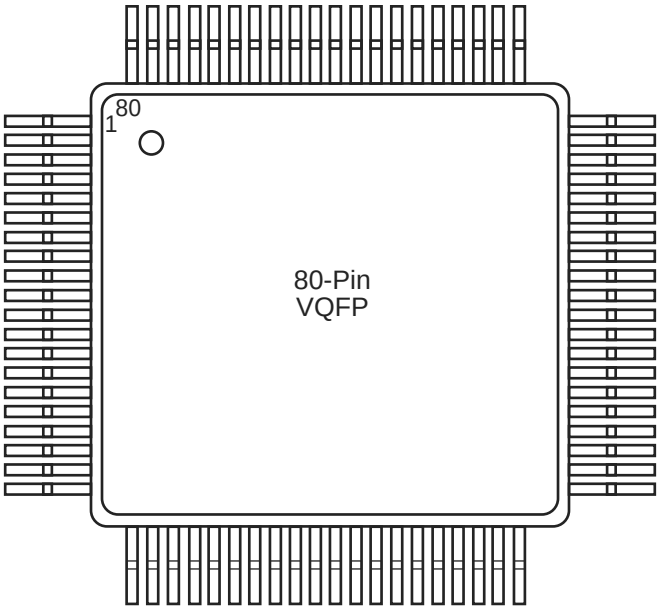



***Table 55 •*** **VQ80**

| **VQ80** | | |
|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** |
| 1 | I/O | I/O |
| 2 | NC | I/O |
| 3 | NC | I/O |
| 4 | NC | I/O |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | GND | GND |
| 8 | I/O | I/O |
| 9 | I/O | I/O |
| 10 | I/O | I/O |
| 11 | I/O | I/O |
| 12 | I/O | I/O |

***Table 56 •*** **VQ100**

| **VQ100** | | |
|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** |
| 57 | I/O | I/O |
| 58 | I/O | I/O |
| 59 | I/O | I/O |
| 60 | I/O | I/O |
| 61 | I/O | I/O |
| 62 | LP | LP |
| 63 | VCCA | VCCA |
| 64 | VCCI | VCCI |
| 65 | VCCA | VCCA |
| 66 | I/O | I/O |
| 67 | I/O | I/O |
| 68 | I/O | I/O |
| 69 | I/O | I/O |
| 70 | GND | GND |
| 71 | I/O | I/O |
| 72 | I/O | I/O |
| 73 | I/O | I/O |
| 74 | I/O | I/O |
| 75 | I/O | I/O |
| 76 | I/O | I/O |
| 77 | SDI, I/O | SDI, I/O |
| 78 | I/O | I/O |
| 79 | I/O | I/O |
| 80 | I/O | I/O |
| 81 | I/O | I/O |
| 82 | GND | GND |
| 83 | I/O | I/O |
| 84 | I/O | I/O |
| 85 | PRA, I/O | PRA, I/O |
| 86 | I/O | I/O |
| 87 | CLKA, I/O | CLKA, I/O |
| 88 | VCCA | VCCA |
| 89 | I/O | I/O |
| 90 | CLKB, I/O | CLKB, I/O |
| 91 | I/O | I/O |
| 92 | PRB, I/O | PRB, I/O |

***Table 57 •*** **TQ176**

| **TQ176** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 158 | CLKB, I/O | CLKB, I/O | CLKB, I/O |
| 159 | I/O | I/O | I/O |
| 160 | PRB, I/O | PRB, I/O | PRB, I/O |
| 161 | NC | I/O | WD, I/O |
| 162 | I/O | I/O | WD, I/O |
| 163 | I/O | I/O | I/O |
| 164 | I/O | I/O | I/O |
| 165 | NC | NC | WD, I/O |
| 166 | NC | I/O | WD, I/O |
| 167 | I/O | I/O | I/O |
| 168 | NC | I/O | I/O |
| 169 | I/O | I/O | I/O |
| 170 | NC | VCCI | VCCI |
| 171 | I/O | I/O | WD, I/O |
| 172 | I/O | I/O | WD, I/O |
| 173 | NC | I/O | I/O |
| 174 | I/O | I/O | I/O |
| 175 | DCLK, I/O | DCLK, I/O | DCLK, I/O |
| 176 | I/O | I/O | I/O |

***Figure 49 •*** **CQ208**