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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	125
Number of Gates	36000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx24-2pqg160



Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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2.3 Ordering Information

The following figure shows ordering information. All the following tables show plastic and ceramic device resources, temperature and speed grade offerings.

Figure 1 • Ordering Information

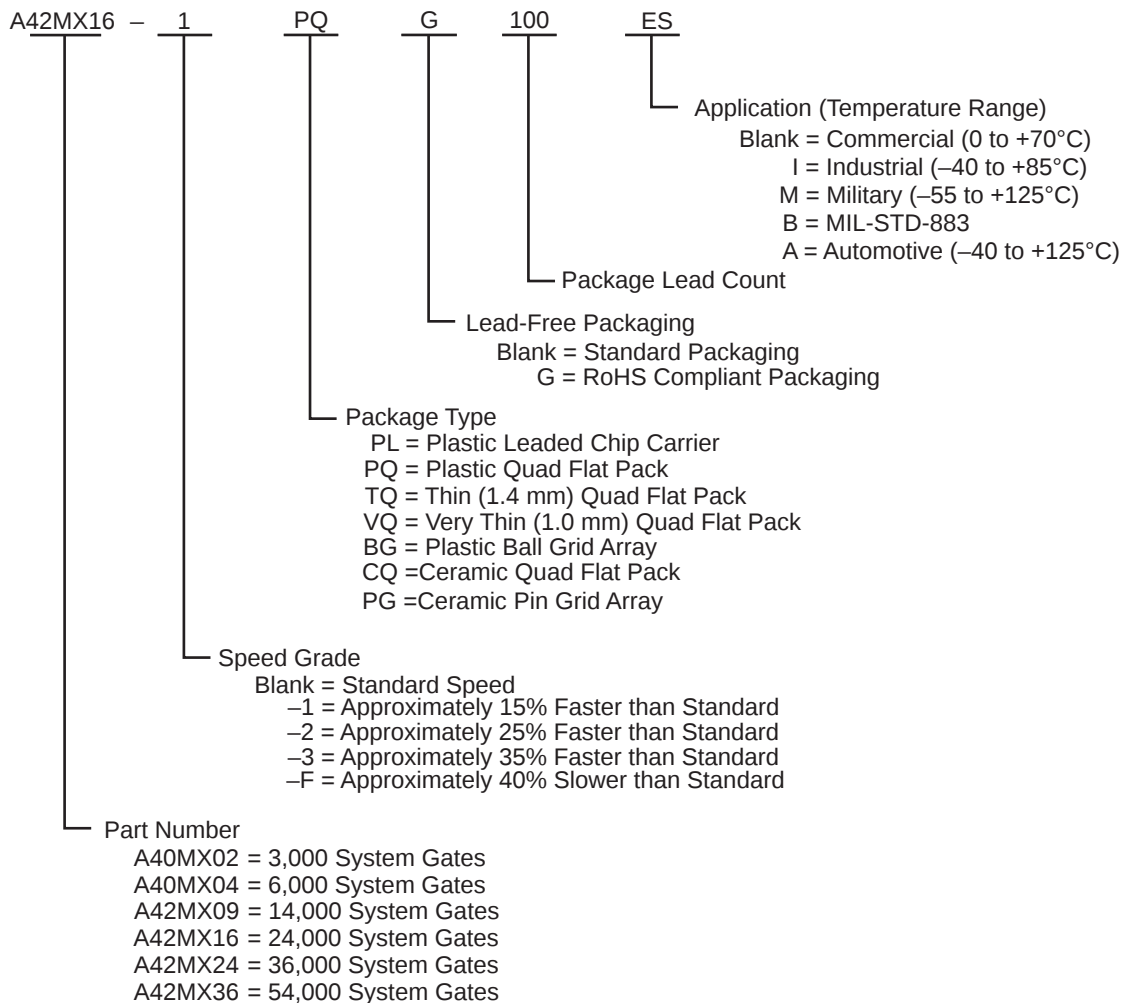
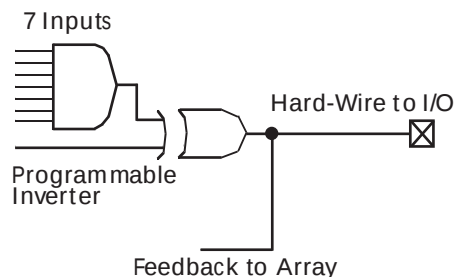
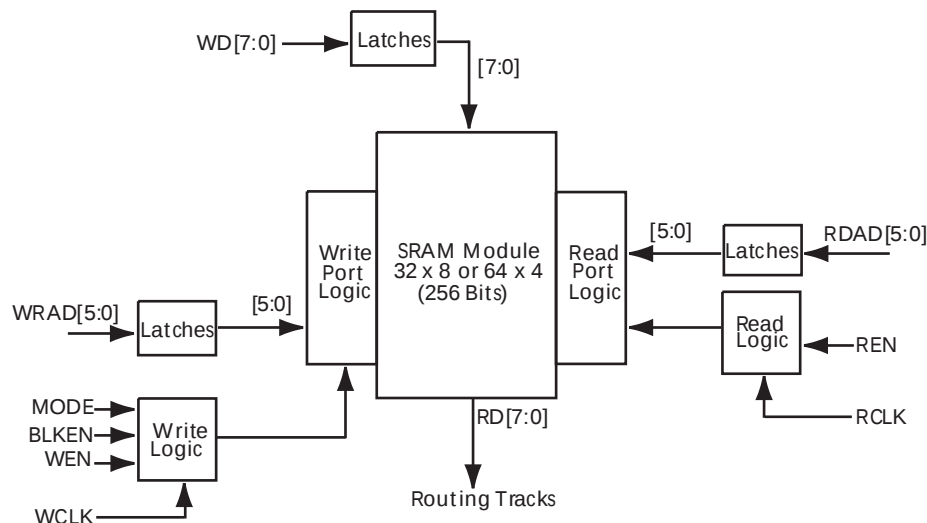


Figure 5 • A42MX24 and A42MX36 D-Module Implementation**Figure 6 • A42MX36 Dual-Port SRAM Block**

3.2.3 Routing Structure

The MX architecture uses vertical and horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may be continuous or split into segments. Varying segment lengths allow the interconnect of over 90% of design tracks to occur with only two antifuse connections. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

3.2.3.1 Horizontal Routing

Horizontal routing tracks span the whole row length or are divided into multiple segments and are located in between the rows of modules. Any segment that spans more than one-third of the row length is considered a long horizontal segment. A typical channel is shown in [Figure 7](#), page 10. Within horizontal routing, dedicated routing tracks are used for global clock networks and for power and ground tie-off tracks. Non-dedicated tracks are used for signal nets.

3.2.3.2 Vertical Routing

Another set of routing tracks run vertically through the module. There are three types of vertical tracks: input, output, and long. Long tracks span the column length of the module, and can be divided into multiple segments. Each segment in an input track is dedicated to the input of a particular module; each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing.

Each output segment spans four channels (two above and two below), except near the top and bottom of the array, where edge effects occur. Long vertical tracks contain either one or two segments. An example of vertical routing tracks and segments is shown in [Figure 7](#), page 10.

3.4.9 JTAG Mode Activation

The JTAG test logic circuit is activated in the Designer software by selecting **Tools > Device Selection**. This brings up the Device Selection dialog box as shown in the following figure. The JTAG test logic circuit can be enabled by clicking the “Reserve JTAG Pins” check box. The following table explains the pins’ behavior in either mode.

Figure 15 • Device Selection Wizard



Table 11 • Boundary Scan Pin Configuration and Functionality

Reserve JTAG	Checked	Unchecked
TCK	BST input; must be terminated to logical HIGH or LOW to avoid floating	User I/O
TDI, TMS	BST input; may float or be tied to HIGH	User I/O
TDO	BST output; may float or be connected to TDI of another device	User I/O

3.4.10 TRST Pin and TAP Controller Reset

An active reset (TRST) pin is not supported; however, MX devices contain power-on circuitry that resets the boundary scan circuitry upon power-up. Also, the TMS pin is equipped with an internal pull-up resistor. This allows the TAP controller to remain in or return to the Test-Logic-Reset state when there is no input or when a logical 1 is on the TMS pin. To reset the controller, TMS must be HIGH for at least five TCK cycles.

3.4.11 Boundary Scan Description Language (BSDL) File

Conforming to the IEEE Standard 1149.1 requires that the operation of the various JTAG components be documented. The BSDL file provides the standard format to describe the JTAG components that can be used by automatic test equipment software. The file includes the instructions that are supported, instruction bit pattern, and the boundary-scan chain order. For an in-depth discussion on BSDL files, see the [BSDL Files Format Description](#) application note.

BSDL files are grouped into two categories - generic and device-specific. The generic files assign all user I/Os as inouts. Device-specific files assign user I/Os as inputs, outputs or inouts.

Generic files for MX devices are available on the Microsemi SoC Product Group's website:

<http://www.microsemi.com/soc/techdocs/models/bsdl.html>.

3.5 Development Tool Support

The MX family of FPGAs is fully supported by Libero® Integrated Design Environment (IDE). Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes SynplifyPro from Synopsys, ModelSim® HDL Simulator from Mentor Graphics® and Viewdraw.

Libero IDE includes place-and-route and provides a comprehensive suite of backend support tools for FPGA development, including timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor.

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 14 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCA (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V

Note: * Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

3.7.1 5 V TTL Electrical Specifications

The following tables show 5 V TTL electrical specifications.

Table 15 • 5V TTL Electrical Specifications

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	IOH = –10 mA	2.4		2.4						V
	IOH = –4 mA					3.7		3.7		V
VOL ¹	IOL = 10 mA		0.5		0.5					V
	IOL = 6 mA					0.4		0.4		V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX) ²		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL	VIN = 0.5 V		–10		–10		–10		–10	μA
IIH	VIN = 2.7 V		–10		–10		–10		–10	μA
Input Transition Time, T_R and T_F			500		500		500		500	ns
C _{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC ³	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		20		25		25		25	mA
Low power mode Standby Current	42MX devices only		0.5		ICC – 5.0		ICC – 5.0		ICC – 5.0	mA
IIO, I/O source sink current	Can be derived from the IBIS model (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCC/VCCI = min

2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RD1}	FO = 1 Routing Delay		2.0		2.2		2.5		3.0		4.2	ns
t _{RD2}	FO = 2 Routing Delay		2.7		3.1		3.5		4.1		5.7	ns
t _{RD3}	FO = 3 Routing Delay		3.4		3.9		4.4		5.2		7.3	ns
t _{RD4}	FO = 4 Routing Delay		4.2		4.8		5.4		6.3		8.9	ns
t _{RD8}	FO = 8 Routing Delay		7.1		8.2		9.2		10.9		15.2	ns
Logic Module Sequential Timing²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		4.3		4.9		5.6		6.6		9.2	ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		4.3		4.9		5.6		6.6		9.2	ns
t _{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		4.6		5.3		6.0		7.0		9.8	ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		4.6		5.3		6.0		7.0		9.8	ns
t _A	Flip-Flop Clock Input Period		6.8		7.8		8.9		10.4		14.6	ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		109		101		92		80		48	MHz
Input Module Propagation Delays												
t _{INYH}	Pad-to-Y HIGH		1.0		1.1		1.3		1.5		2.1	ns
t _{INYL}	Pad-to-Y LOW		0.9		1.0		1.1		1.3		1.9	ns
Input Module Predicted Routing Delays¹												
t _{IRD1}	FO = 1 Routing Delay		2.9		3.4		3.8		4.5		6.3	ns
t _{IRD2}	FO = 2 Routing Delay		3.6		4.2		4.8		5.6		7.8	ns
t _{IRD3}	FO = 3 Routing Delay		4.4		5.0		5.7		6.7		9.4	ns
t _{IRD4}	FO = 4 Routing Delay		5.1		5.9		6.7		7.8		11.0	ns
t _{IRD8}	FO = 8 Routing Delay		8.0		9.26		10.5		12.6		17.3	ns
Global Clock Network												
t _{CKH}	Input LOW to HIGH	FO = 16	6.4		7.4		8.3		9.8		13.7	ns
		FO = 128	6.4		7.4		8.3		9.8		13.7	
t _{CKL}	Input HIGH to LOW	FO = 16	6.7		7.8		8.8		10.4		14.5	ns
		FO = 128	6.7		7.8		8.8		10.4		14.5	
t _{PWH}	Minimum Pulse Width HIGH	FO = 16	3.1		3.6		4.1		4.8		6.7	ns
		FO = 128	3.3		3.8		4.3		5.1		7.1	
t _{PWL}	Minimum Pulse Width LOW	FO = 16	3.1		3.6		4.1		4.8		6.7	ns
		FO = 128	3.3		3.8		4.3		5.1		7.1	
t _{CKSW}	Maximum Skew	FO = 16	0.6		0.6		0.7		0.8		1.2	ns
		FO = 128	0.8		0.9		1.0		1.2		1.6	

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _p	Minimum Period	FO = 16	6.5		7.5		8.5		10.1		14.1		ns
		FO = 128	6.8		7.8		8.9		10.4		14.6		
f _{MAX}	Maximum Frequency	FO = 16		113		105		96		83		50	MHz
		FO = 128		109		101		92		80		48	
TTL Output Module Timing ⁴													
t _{DLH}	Data-to-Pad HIGH			4.7		5.4		6.1		7.2		10.0	ns
t _{DHL}	Data-to-Pad LOW			5.6		6.4		7.3		8.6		12.0	ns
t _{ENZH}	Enable Pad Z to HIGH			5.2		6.0		6.8		8.1		11.3	ns
t _{ENZL}	Enable Pad Z to LOW			6.6		7.6		8.6		10.1		14.1	ns
t _{ENHZ}	Enable Pad HIGH to Z			11.1		12.8		14.5		17.1		23.9	ns
t _{ENLZ}	Enable Pad LOW to Z			8.2		9.5		10.7		12.6		17.7	ns
d _{TLH}	Delta LOW to HIGH			0.03		0.03		0.04		0.04		0.06	ns/pF
d _{THL}	Delta HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH		5.5		6.4		7.2		8.5		11.9	ns
t _{DHL}	Data-to-Pad LOW		4.8		5.5		6.2		7.3		10.2	ns
t _{ENZH}	Enable Pad Z to HIGH		4.7		5.5		6.2		7.3		10.2	ns
t _{ENZL}	Enable Pad Z to LOW		6.8		7.9		8.9		10.5		14.7	ns
t _{ENHZ}	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9	ns
t _{ENLZ}	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7	ns
d _{TLH}	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d _{THL}	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro
4. Delays based on 35 pF loading

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t _{PD2}	Dual-Module Macros		2.3		3.1		3.5		4.1		5.7	ns
t _{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays ¹												
t _{RD1}	FO = 1 Routing Delay		1.2		1.6		1.8		2.1		3.0	ns
t _{RD2}	FO = 2 Routing Delay		1.9		2.2		2.5		2.9		4.1	ns
t _{RD3}	FO = 3 Routing Delay		2.4		2.8		3.2		3.7		5.2	ns
t _{RD4}	FO = 4 Routing Delay		2.9		3.4		3.9		4.5		6.3	ns
t _{RD8}	FO = 8 Routing Delay		5.0		5.8		6.6		7.8		10.9	ns
Logic Module Sequential Timing ²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		3.1		3.5		4.0		4.7		6.6	ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		3.1		3.5		4.0		4.7		6.6	ns

Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t _A	Flip-Flop Clock Input Period	6.8		7.8		8.9		10.4		14.6		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		109		101		92		80		48	MHz
Input Module Propagation Delays												
t _{INYH}	Pad-to-Y HIGH		1.0		1.1		1.3		1.5		2.1	ns
t _{INYL}	Pad-to-Y LOW		0.9		1.0		1.1		1.3		1.9	ns

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RD3}	FO = 3 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t _{RD4}	FO = 4 Routing Delay		1.6		1.7		2.0		2.3		3.2	ns
t _{RD8}	FO = 8 Routing Delay		2.6		2.9		3.2		3.8		5.3	ns
Logic Module Sequential Timing^{3,4}												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		0.3		0.4		0.4		0.5		0.7	ns
t _{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		0.7		0.8		0.9		1.0		1.4	ns
t _{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		3.4		3.8		4.3		5.0		7.1	ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		4.5		5.0		5.6		6.6		9.2	ns
t _A	Flip-Flop Clock Input Period		6.8		7.6		8.6		10.1		14.1	ns
t _{INH}	Input Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{INSU}	Input Buffer Latch Set-Up		0.5		0.5		0.6		0.7		1.0	ns
t _{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{OUTSU}	Output Buffer Latch Set-Up		0.5		0.5		0.6		0.7		1.0	ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency		215		195		179		156		94	MHz
Input Module Propagation Delays												
t _{INYH}	Pad-to-Y HIGH		1.1		1.2		1.3		1.6		2.2	ns
t _{INYL}	Pad-to-Y LOW		0.8		0.9		1.0		1.2		1.7	ns
t _{INGH}	G to Y HIGH		1.4		1.6		1.8		2.1		2.9	ns
t _{INGL}	G to Y LOW		1.4		1.6		1.8		2.1		2.9	ns
Input Module Predicted Routing Delays²												
t _{IRD1}	FO = 1 Routing Delay		1.8		2.0		2.3		2.7		4.0	ns
t _{IRD2}	FO = 2 Routing Delay		2.1		2.3		2.6		3.1		4.3	ns
t _{IRD3}	FO = 3 Routing Delay		2.3		2.6		3.0		3.5		4.9	ns
t _{IRD4}	FO = 4 Routing Delay		2.6		3.0		3.3		3.9		5.4	ns
t _{IRD8}	FO = 8 Routing Delay		3.6		4.0		4.6		5.4		7.5	ns
Global Clock Network												
t _{CKH}	Input LOW to HIGH	FO = 32	2.6		2.9		3.3		3.9		5.4	ns
		FO = 384	2.9		3.2		3.6		4.3		6.0	ns
t _{CKL}	Input HIGH to LOW	FO = 32	3.8		4.2		4.8		5.6		7.8	ns
		FO = 384	4.5		5.0		5.6		6.6		9.2	ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	3.2		3.5		4.0		4.7		6.6	ns
		FO = 384	3.7		4.1		4.6		5.4		7.6	ns

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		3.1		3.5		3.9		4.6		6.4	ns
t _{DHL}	Data-to-Pad LOW		2.4		2.6		3.0		3.5		4.9	ns
t _{ENZH}	Enable Pad Z to HIGH		2.5		2.8		3.2		3.8		5.3	ns
t _{ENZL}	Enable Pad Z to LOW		2.8		3.1		3.5		4.2		5.8	ns
t _{ENHZ}	Enable Pad HIGH to Z		5.2		5.7		6.5		7.6		10.7	ns
t _{ENLZ}	Enable Pad LOW to Z		4.8		5.3		6.0		7.1		9.9	ns
t _{GLH}	G-to-Pad HIGH		4.9		5.4		6.2		7.2		10.1	ns
t _{GHL}	G-to-Pad LOW		4.9		5.4		6.2		7.2		10.1	ns
t _{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.5		6.1		6.9		8.1		11.3	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.6		11.8		13.4		15.7		22.0	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions ¹												
t _{PD}	Internal Array Module Delay		2.0		1.8		2.1		2.5		3.4	ns
t _{PDD}	Internal Decode Module Delay		1.1		2.2		2.5		3.0		4.2	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		1.7		1.3		1.4		1.7		2.3	ns
t _{RD2}	FO = 2 Routing Delay		2.0		1.6		1.8		2.1		3.0	ns
t _{RD3}	FO = 3 Routing Delay		1.1		2.0		2.2		2.6		3.7	ns
t _{RD4}	FO = 4 Routing Delay		1.5		2.3		2.6		3.1		4.3	ns
t _{RD5}	FO = 8 Routing Delay		1.8		3.7		4.2		5.0		7.0	ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Asynchronous SRAM Operations													
t _{RPD}	Asynchronous Access Time		8.1		9.0		10.2		12.0		16.8		ns
t _{RDADV}	Read Address Valid		8.8		9.8		11.1		13.0		18.2		ns
t _{ADSU}	Address/Data Set-Up Time		1.6		1.8		2.0		2.4		3.4		ns
t _{ADH}	Address/Data Hold Time		0.0		0.0		0.0		0.0		0.0		ns
t _{RENSUA}	Read Enable Set-Up to Address Valid		0.6		0.7		0.8		0.9		1.3		ns
t _{RENHA}	Read Enable Hold		3.4		3.8		4.3		5.0		7.0		ns
t _{WENSU}	Write Enable Set-Up		2.7		3.0		3.4		4.0		5.6		ns
t _{WENH}	Write Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{DOH}	Data Out Hold Time		1.2		1.3		1.5		1.8		2.5		ns
Input Module Propagation Delays													
t _{INPY}	Input Data Pad-to-Y		1.0		1.1		1.3		1.5		2.1		ns
t _{INGO}	Input Latch Gate-to-Output		1.4		1.6		1.8		2.1		2.9		ns
t _{INH}	Input Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Latch Set-Up		0.5		0.5		0.6		0.7		1.0		ns
t _{ILA}	Latch Active Pulse Width		4.7		5.2		5.9		6.9		9.7		ns
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay		2.0		2.2		2.5		2.9		4.1		ns
t _{IRD2}	FO = 2 Routing Delay		2.3		2.6		2.9		3.4		4.8		ns
t _{IRD3}	FO = 3 Routing Delay		2.6		2.9		3.3		3.9		5.5		ns
t _{IRD4}	FO = 4 Routing Delay		3.0		3.3		3.8		4.4		6.2		ns
t _{IRD8}	FO = 8 Routing Delay		4.3		4.8		5.5		6.4		9.0		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32	2.7	3.0	3.4	4.0	5.6	ns					
		FO = 635	3.0	3.3	3.8	4.4	6.2	ns					
t _{CKL}	Input HIGH to LOW	FO = 32	3.8	4.2	4.8	5.6	7.8	ns					
		FO = 635	4.9	5.4	6.1	7.2	10.1	ns					
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	1.8	2.0	2.2	2.6	3.6	ns					
		FO = 635	2.0	2.2	2.5	2.9	4.1	ns					
t _{PWL}	Minimum Pulse Width LOW	FO = 32	1.8	2.0	2.2	2.6	3.6	ns					
		FO = 635	2.0	2.2	2.5	2.9	4.1	ns					
t _{CKSW}	Maximum Skew	FO = 32	0.8	0.8	0.9	1.0	1.4	ns					
		FO = 635	0.8	0.8	0.9	1.0	1.4	ns					

Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
47	I/O	I/O	I/O	WD, I/O
48	I/O	I/O	I/O	I/O
49	I/O	GND	GND	GND
50	I/O	I/O	I/O	WD, I/O
51	I/O	I/O	I/O	WD, I/O
52	I/O	SDO, I/O	SDO, I/O	SDO, TDO, I/O
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	GND	I/O	I/O	I/O
61	GND	I/O	I/O	I/O
62	I/O	I/O	I/O	TCK, I/O
63	I/O	LP	LP	LP
64	CLK, I/O	VCCA	VCCA	VCCA
65	I/O	VCCI	VCCI	VCCI
66	MODE	I/O	I/O	I/O
67	VCC	I/O	I/O	I/O
68	VCC	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	GND	GND	GND
71	I/O	I/O	I/O	I/O
72	SDI, I/O	I/O	I/O	I/O
73	DCLK, I/O	I/O	I/O	I/O
74	PRA, I/O	I/O	I/O	I/O
75	PRB, I/O	I/O	I/O	I/O
76	I/O	SDI, I/O	SDI, I/O	SDI, I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	WD, I/O
79	I/O	I/O	I/O	WD, I/O
80	I/O	I/O	I/O	WD, I/O
81	I/O	PRA, I/O	PRA, I/O	PRA, I/O
82	GND	I/O	I/O	I/O
83	I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O

Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
117	GNDI
118	NC
119	I/O
120	I/O
121	I/O
122	I/O
123	PROBA
124	I/O
125	CLKA
126	VCC
127	VCCI
128	NC
129	I/O
130	CLKB
131	I/O
132	PROBB
133	I/O
134	I/O
135	I/O
136	GND
137	GNDI
138	NC
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	DCLK

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
58	I/O	WD, I/O	WD, I/O
59	I/O	I/O	I/O
60	VCCI	VCCI	VCCI
61	NC	I/O	I/O
62	NC	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	QCLKA, I/O
66	I/O	WD, I/O	WD, I/O
67	NC	WD, I/O	WD, I/O
68	NC	I/O	I/O
69	I/O	I/O	I/O
70	I/O	WD, I/O	WD, I/O
71	I/O	WD, I/O	WD, I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	GND	GND	GND
79	VCCA	VCCA	VCCA
80	NC	VCCI	VCCI
81	I/O	I/O	I/O
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	WD, I/O	WD, I/O
86	I/O	WD, I/O	WD, I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	NC	I/O	I/O
90	NC	I/O	I/O
91	I/O	I/O	QCLKB, I/O
92	I/O	I/O	I/O
93	I/O	WD, I/O	WD, I/O
94	I/O	WD, I/O	WD, I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
15	QCLKC, I/O
16	I/O
17	WD, I/O
18	WD, I/O
19	I/O
20	I/O
21	WD, I/O
22	WD, I/O
23	I/O
24	PRB, I/O
25	I/O
26	CLKB, I/O
27	I/O
28	GND
29	VCCA
30	VCCI
31	I/O
32	CLKA, I/O
33	I/O
34	PRA, I/O
35	I/O
36	I/O
37	WD, I/O
38	WD, I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	QCLKD, I/O
46	I/O
47	WD, I/O
48	WD, I/O
49	I/O
50	I/O
51	I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
185	I/O
186	CLKB, I/O
187	I/O
188	PRB, I/O
189	I/O
190	WD, I/O
191	WD, I/O
192	I/O
193	I/O
194	WD, I/O
195	WD, I/O
196	QCLKC, I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	I/O
202	VCCI
203	WD, I/O
204	WD, I/O
205	I/O
206	I/O
207	DCLK, I/O
208	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
22	I/O
23	I/O
24	I/O
25	I/O
26	VCCA
27	I/O
28	I/O
29	VCCA
30	VCCI
31	GND
32	VCCA
33	LP
34	TCK, I/O
35	I/O
36	GND
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	GND
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
J9	GND
J10	GND
J11	GND
J12	GND
J17	VCCA
J18	I/O
J19	I/O
J20	I/O
K1	I/O
K2	I/O
K3	I/O
K4	VCCI
K9	GND
K10	GND
K11	GND
K12	GND
K17	I/O
K18	VCCA
K19	VCCA
K20	LP
L1	I/O
L2	I/O
L3	VCCA
L4	VCCA
L9	GND
L10	GND
L11	GND
L12	GND
L17	VCCI
L18	I/O
L19	I/O
L20	TCK, I/O
M1	I/O
M2	I/O
M3	I/O
M4	VCCI
M9	GND

Figure 53 • CQ172

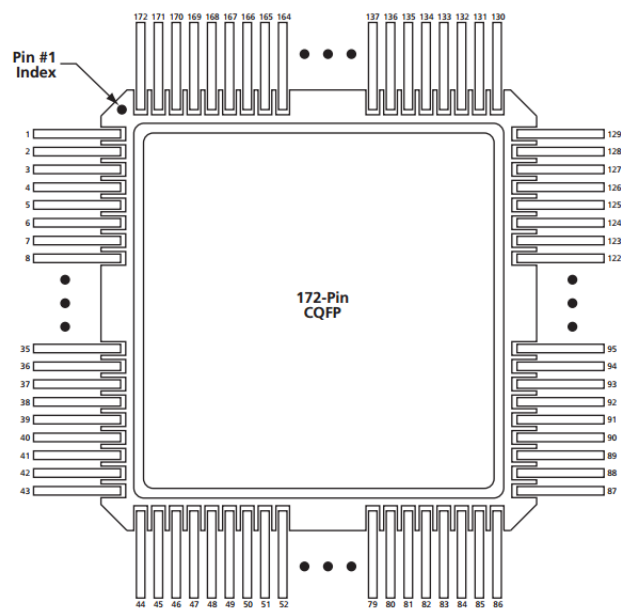


Table 62 • CQ172

CQ172	
Pin Number	A42MX16 Function
1	MODE
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	GND
8	I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	I/O
17	GND
18	I/O
19	I/O
20	I/O