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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	125
Number of Gates	36000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx24-3pqg160

2.6 Temperature Grade Offerings

Table 4 • Temperature Grade Offerings

Package	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PLCC 44	C, I, M	C, I, M				
PLCC 68	C, I, A, M	C, I, M				
PLCC 84		C, I, A, M	C, I, A, M	C, I, M	C, I, M	
PQFP 100	C, I, A, M	C, I, A, M	C, I, A, M	C, I, M		
PQFP 144			C			
PQFP 160			C, I, A, M	C, I, M	C, I, A, M	
PQFP 208				C, I, A, M	C, I, A, M	C, I, A, M
PQFP 240						C, I, A, M
VQFP 80	C, I, A, M	C, I, A, M				
VQFP 100			C, I, A, M	C, I, A, M		
TQFP 176			C, I, A, M	C, I, A, M	C, I, A, M	
PBGA 272						C, I, M
CQFP 172				C, M, B		
CQFP 208						C, M, B
CQFP 256						C, M, B
CPGA 132			C, M, B			

Note: C = Commercial
 I = Industrial
 A = Automotive
 M = Military
 B = MIL-STD-883 Class B

2.7 Speed Grade Offerings

Table 5 • Speed Grade Offerings

	– F	Std	–1	–2	–3
C	P	P	P	P	P
I		P	P	P	P
A		P			
M		P	P		
B		P	P		

Note: See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local *Microsemi Sales representative* for device availability.

3 40MX and 42MX FPGAs

3.1 General Description

Microsemi's 40MX and 42MX families offer a cost-effective design solution at 5V. The MX devices are single-chip solutions and provide high performance while shortening the system design and development cycle. MX devices can integrate and consolidate logic implemented in multiple PALs, CPLDs, and FPGAs. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

The MX device architecture is based on Microsemi's patented antifuse technology implemented in a 0.45µm triple-metal CMOS process. With capacities ranging from 3,000 to 54,000 system gates, the MX devices provide performance up to 250 MHz, are live on power-up and have one-fifth the standby power consumption of comparable FPGAs. MX FPGAs provide up to 202 user I/Os and are available in a wide variety of packages and speed grades.

A42MX24 and A42MX36 devices also feature multiPlex I/Os, which support mixed-voltage systems, enable programmable PCI, deliver high-performance operation at both 5.0V and 3.3V, and provide a low-power mode. The devices are fully compliant with the PCI local bus specification (version 2.1). They deliver 200 MHz on-chip operation and 6.1 ns clock-to-output performance.

The 42MX24 and 42MX36 devices include system-level features such as IEEE Standard 1149.1 (JTAG) Boundary Scan Testing and fast wide-decode modules. In addition, the A42MX36 device offers dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The storage elements can efficiently address applications requiring wide data path manipulation and can perform transformation functions such as those required for telecommunications, networking, and DSP.

All MX devices are fully tested over automotive and military temperature ranges. In addition, the largest member of the family, the A42MX36, is available in both CQ208 and CQ256 ceramic packages screened to MIL-STD-883 levels. For easy prototyping and conversion from plastic to ceramic, the CQ208 and PQ208 devices are pin-compatible.

3.2 MX Architectural Overview

The MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within these families are composed of logic modules, I/O modules, routing resources and clock networks, which are the building blocks for fast logic designs. In addition, the A42MX36 device contains embedded dual-port SRAM modules, which are optimized for high-speed data path functions such as FIFOs, LIFOs and scratch pad memory. A42MX24 and A42MX36 also contain wide-decode modules.

3.2.1 Logic Modules

The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources.(see the following figure).

The logic module can implement the four basic logic functions (NAND, AND, OR and NOR) in gates of two, three, or four inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array; latches and flip-flops can be constructed from logic modules whenever required in the application.

3.8.1 3.3 V LVTTTL Electrical Specifications

Table 19 • 3.3V LVTTTL Electrical Specifications

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	IOH = -4 mA	2.15		2.15		2.4		2.4		V
VOL ¹	IOL = 6 mA		0.4		0.4		0.48		0.48	V
VIL		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX)		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL			-10		-10		-10		-10	μA
IIH			-10		-10		-10		-10	μA
Input Transition Time, T _R and T _F			500		500		500		500	ns
C _{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC ²	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		15		25		25		25	mA
Low-Power Mode Standby Current	42MX devices only		0.5		ICC - 5.0		ICC - 5.0		ICC - 5.0	mA
I/O, I/O source sink current	Can be derived from the <i>IBIS model</i> (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

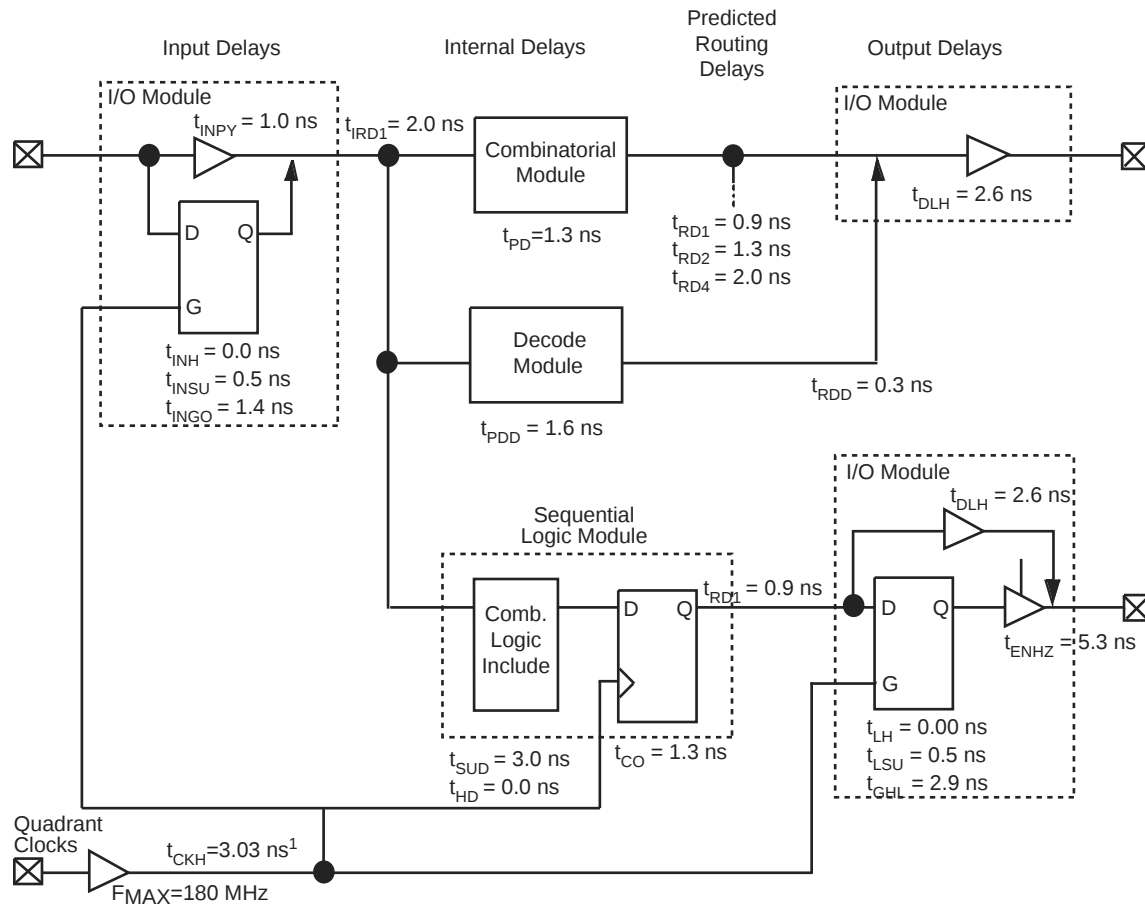
1. Only one output tested at a time. VCC/VCCI = min.
2. All outputs unloaded. All inputs = VCC/VCCI or GND.

3.9 Mixed 5.0 V / 3.3 V Operating Conditions (for 42MX Devices Only)

Table 20 • Absolute Maximum Ratings*

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	-0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	-0.5 to +7.0	V
VI	Input Voltage	-0.5 to VCCA + 0.5	V
VO	Output Voltage	-0.5 to VCCI + 0.5	V
t _{STG}	Storage Temperature	-65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device

Figure 19 • 42MX Timing Model (Logic Functions Using Quadrant Clocks)

Note: 1. Load-dependent

Note: 2. Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions

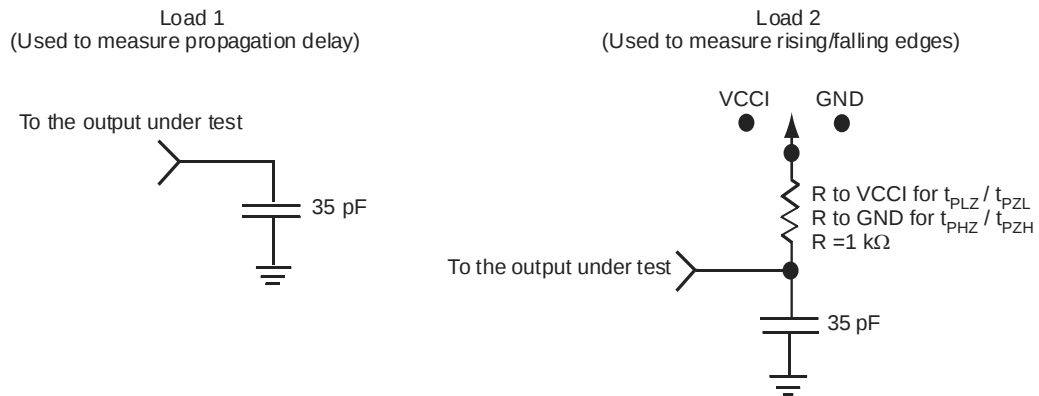
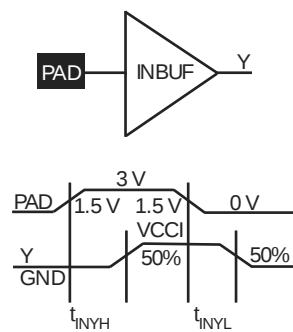
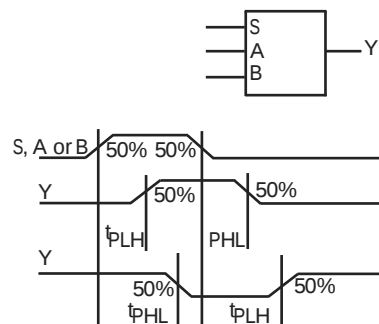
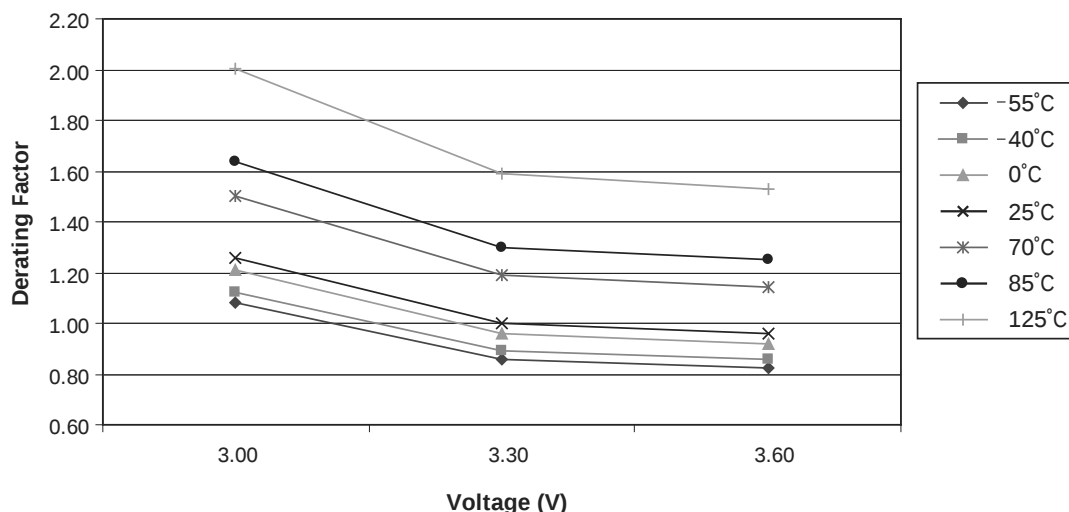
Figure 22 • AC Test Loads**Figure 23 • Input Buffer Delays****Figure 24 • Module Delays**

Table 31 • 40MX Temperature and Voltage Derating Factors (Normalized to T_J = 25°C, V_{CC} = 3.3 V)

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
3.60	0.83	0.85	0.92	0.96	1.14	1.25	1.53

Figure 37 • 40MX Junction Temperature and Voltage Derating Curves (Normalized to T_J = 25°C, V_{CC} = 3.3 V)

Note: This derating factor applies to all routing and propagation delays

3.11.5 PCI System Timing Specification

The following tables list the critical PCI timing parameters and the corresponding timing parameters for the MX PCI-compliant devices.

3.11.6 PCI Models

Microsemi provides synthesizable VHDL and Verilog-HDL models for a PCI Target interface, a PCI Target and Target+DMA Master interface. Contact the Microsemi sales representative for more details.

Table 32 • Clock Specification for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC}	CLK Cycle Time	30	–	4.0	–	4.0	–	ns
t _{HIGH}	CLK High Time	11	–	1.9	–	1.9	–	ns
t _{LOW}	CLK Low Time	11	–	1.9	–	1.9	–	ns

Table 33 • Timing Parameters for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{VAL}	CLK to Signal Valid—Bused Signals	2	11	2.0	9.0	2.0	9.0	ns
t _{VAL(PTP)}	CLK to Signal Valid—Point-to-Point	2 ²	12	2.0	9.0	2.0	9.0	ns
t _{ON}	Float to Active	2	–	2.0	4.0	2.0	4.0	ns
t _{OFF}	Active to Float	–	28	–	8.3 ¹	–	8.3 ¹	ns
t _{SU}	Input Set-Up Time to CLK—Bused Signals	7	–	1.5	–	1.5	–	ns

Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t _A	Flip-Flop Clock Input Period	6.8		7.8		8.9		10.4		14.6		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		109		101		92		80		48	MHz
Input Module Propagation Delays												
t _{INYH}	Pad-to-Y HIGH		1.0		1.1		1.3		1.5		2.1	ns
t _{INYL}	Pad-to-Y LOW		0.9		1.0		1.1		1.3		1.9	ns

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t _{INYH}	Pad-to-Y HIGH		1.5		1.6		1.8		2.17		3.0		ns
t _{INYL}	Pad-to-Y LOW		1.2		1.3		1.4		1.7		2.4		ns
t _{INGH}	G to Y HIGH		1.8		2.0		2.3		2.7		3.7		ns
t _{INGL}	G to Y LOW		1.8		2.0		2.3		2.7		3.7		ns
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay		2.8		3.2		3.6		4.2		5.9		ns
t _{IRD2}	FO = 2 Routing Delay		3.2		3.5		4.0		4.7		6.6		ns
t _{IRD3}	FO = 3 Routing Delay		3.5		3.9		4.4		5.2		7.3		ns
t _{IRD4}	FO = 4 Routing Delay		3.9		4.3		4.9		5.7		8.0		ns
t _{IRD8}	FO = 8 Routing Delay		5.2		5.8		6.6		7.7		10.8		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32	4.1		4.5		5.1		6.0		8.4		ns
		FO = 256	4.5		5.0		5.6		6.7		9.3		ns
t _{CKL}	Input HIGH to LOW	FO = 32	5.0		5.5		6.2		7.3		10.2		ns
		FO = 256	5.4		6.0		6.8		8.0		11.2		ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	1.7		1.9		2.1		2.5		3.5		ns
		FO = 256	1.9		2.1		2.3		2.7		3.8		ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	1.7		1.9		2.1		2.5		3.5		ns
		FO = 256	1.9		2.1		2.3		2.7		3.8		ns
t _{CKSW}	Maximum Skew	FO = 32	0.4		0.5		0.5		0.6		0.9		ns
		FO = 256	0.4		0.5		0.5		0.6		0.9		ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	3.3		3.7		4.2		4.9		6.9		ns
		FO = 256	3.7		4.1		4.6		5.5		7.6		ns
t _P	Minimum Period	FO = 32	5.6		6.2		6.7		7.8		12.9		ns
		FO = 256	6.1		6.8		7.4		8.5		14.2		ns
f _{MAX}	Maximum Frequency	FO = 32	177		161		148		129		77		MHz
		FO = 256	161		146		135		117		70		MHz

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH	2.5		2.8		3.2		3.7		5.2		ns
t _{DHL}	Data-to-Pad LOW	3.0		3.3		3.7		4.4		6.1		ns
t _{ENZH}	Enable Pad Z to HIGH	2.7		3.0		3.4		4.0		5.6		ns
t _{ENZL}	Enable Pad Z to LOW	3.0		3.3		3.8		4.4		6.2		ns
t _{ENHZ}	Enable Pad HIGH to Z	5.4		6.0		6.8		8.0		11.2		ns
t _{ENLZ}	Enable Pad LOW to Z	5.0		5.6		6.3		7.4		10.4		ns
t _{GLH}	G-to-Pad HIGH	2.9		3.2		3.6		4.3		6.0		ns
t _{GHL}	G-to-Pad LOW	2.9		3.2		3.6		4.3		6.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading	5.7		6.3		7.1		8.4		11.9		ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading	8.0		8.9		10.1		11.9		16.7		ns
d _{TLH}	Capacitive Loading, LOW to HIGH	0.03		0.03		0.03		0.04		0.06		ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW	0.04		0.04		0.04		0.05		0.07		ns/pF

4 Package Pin Assignments

The following figures and tables give the details of the package pin assignments.

Figure 38 • PL44

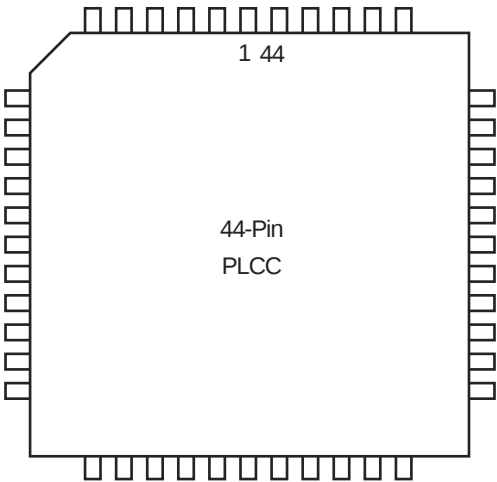


Table 47 • PL44

PL44		
Pin Number	A40MX02 Function	A40MX04 Function
1	I/O	I/O
2	I/O	I/O
3	VCC	VCC
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	GND	GND
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	VCC	VCC
15	I/O	I/O
16	VCC	VCC
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O

Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
47	I/O	I/O	I/O	WD, I/O
48	I/O	I/O	I/O	I/O
49	I/O	GND	GND	GND
50	I/O	I/O	I/O	WD, I/O
51	I/O	I/O	I/O	WD, I/O
52	I/O	SDO, I/O	SDO, I/O	SDO, TDO, I/O
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	GND	I/O	I/O	I/O
61	GND	I/O	I/O	I/O
62	I/O	I/O	I/O	TCK, I/O
63	I/O	LP	LP	LP
64	CLK, I/O	VCCA	VCCA	VCCA
65	I/O	VCCI	VCCI	VCCI
66	MODE	I/O	I/O	I/O
67	VCC	I/O	I/O	I/O
68	VCC	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	GND	GND	GND
71	I/O	I/O	I/O	I/O
72	SDI, I/O	I/O	I/O	I/O
73	DCLK, I/O	I/O	I/O	I/O
74	PRA, I/O	I/O	I/O	I/O
75	PRB, I/O	I/O	I/O	I/O
76	I/O	SDI, I/O	SDI, I/O	SDI, I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	WD, I/O
79	I/O	I/O	I/O	WD, I/O
80	I/O	I/O	I/O	WD, I/O
81	I/O	PRA, I/O	PRA, I/O	PRA, I/O
82	GND	I/O	I/O	I/O
83	I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O

Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
95	I/O	I/O	I/O
96	I/O	I/O	WD, I/O
97	I/O	I/O	I/O
98	VCCA	VCCA	VCCA
99	GND	GND	GND
100	NC	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	NC	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	WD, I/O
107	I/O	I/O	WD, I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	NC	I/O	I/O
111	I/O	I/O	WD, I/O
112	I/O	I/O	WD, I/O
113	I/O	I/O	I/O
114	NC	VCCI	VCCI
115	I/O	I/O	WD, I/O
116	NC	I/O	WD, I/O
117	I/O	I/O	I/O
118	I/O	I/O	TDI, I/O
119	I/O	I/O	TMS, I/O
120	GND	GND	GND
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	NC	I/O	I/O
125	GND	GND	GND
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	NC	I/O	I/O
130	GND	GND	GND
131	I/O	I/O	I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
89	VCCI
90	VCCA
91	LP
92	TCK, I/O
93	I/O
94	GND
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	VCCI
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	VCCA
119	GND
120	GND
121	GND
122	I/O
123	SDO, TDO, I/O
124	I/O
125	WD, I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
163	WD, I/O
164	WD, I/O
165	I/O
166	QCLKA, I/O
167	I/O
168	I/O
169	I/O
170	I/O
171	I/O
172	VCCI
173	I/O
174	WD, I/O
175	WD, I/O
176	I/O
177	I/O
178	TDI, I/O
179	TMS, I/O
180	GND
181	VCCA
182	GND
183	I/O
184	I/O
185	I/O
186	I/O
187	I/O
188	I/O
189	I/O
190	I/O
191	I/O
192	VCCI
193	I/O
194	I/O
195	I/O
196	I/O
197	I/O
198	I/O
199	I/O

Table 56 • VQ100

VQ100		
Pin Number	A42MX09 Function	A42MX16 Function
93	I/O	I/O
94	GND	GND
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	DCLK, I/O	DCLK, I/O

Figure 48 • TQ176

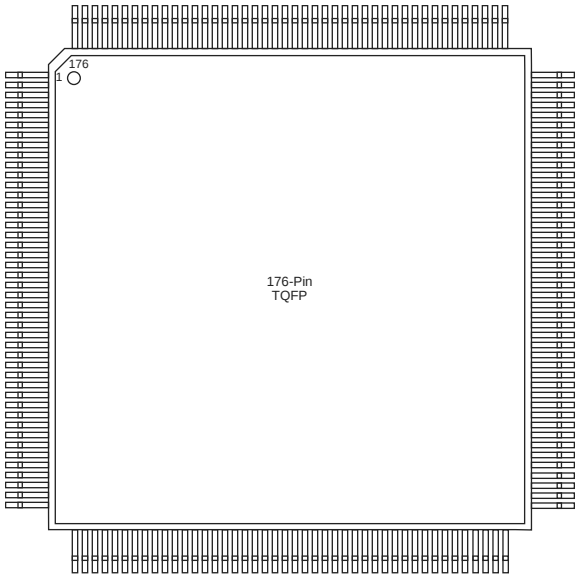


Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	GND	GND	GND
2	MODE	MODE	MODE
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	NC	NC	I/O
9	I/O	I/O	I/O

Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
47	I/O	I/O	TDI, I/O
48	I/O	I/O	I/O
49	I/O	I/O	WD, I/O
50	I/O	I/O	WD, I/O
51	I/O	I/O	I/O
52	NC	VCCI	VCCI
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	NC	I/O	WD, I/O
56	I/O	I/O	WD, I/O
57	NC	NC	I/O
58	I/O	I/O	I/O
59	I/O	I/O	WD, I/O
60	I/O	I/O	WD, I/O
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65	I/O	I/O	I/O
66	NC	I/O	I/O
67	GND	GND	GND
68	VCCA	VCCA	VCCA
69	I/O	I/O	WD, I/O
70	I/O	I/O	WD, I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	NC	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	NC	NC	WD, I/O
78	NC	I/O	WD, I/O
79	I/O	I/O	I/O
80	NC	I/O	I/O
81	I/O	I/O	I/O
82	NC	VCCI	VCCI
83	I/O	I/O	I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
74	I/O
75	I/O
76	I/O
77	I/O
78	GND
79	VCCA
80	VCCI
81	I/O
82	I/O
83	I/O
84	I/O
85	WD, I/O
86	WD, I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	QCLKB, I/O
92	I/O
93	WD, I/O
94	WD, I/O
95	I/O
96	I/O
97	I/O
98	VCCI
99	I/O
100	WD, I/O
101	WD, I/O
102	I/O
103	TDO, I/O
104	I/O
105	GND
106	VCCA
107	I/O
108	I/O
109	I/O
110	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
59	I/O
60	VCCA
61	GND
62	GND
63	NC
64	NC
65	NC
66	I/O
67	SDO, TDO, I/O
68	I/O
69	WD, I/O
70	WD, I/O
71	I/O
72	VCCI
73	I/O
74	I/O
75	I/O
76	WD, I/O
77	GND
78	WD, I/O
79	I/O
80	QCLKB, I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	WD, I/O
88	WD, I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	VCCI

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
M10	GND
M11	GND
M12	GND
M17	I/O
M18	I/O
M19	I/O
M20	I/O
N1	I/O
N2	I/O
N3	I/O
N4	VCCI
N17	VCCI
N18	I/O
N19	I/O
N20	I/O
P1	I/O
P2	I/O
P3	I/O
P4	VCCA
P17	I/O
P18	I/O
P19	I/O
P20	I/O
R1	I/O
R2	I/O
R3	I/O
R4	VCCI
R17	VCCI
R18	I/O
R19	I/O
R20	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T17	VCCA
T18	I/O

Table 61 • PG132

PG132	
Pin Number	A42MX09 Function
B3	I/O
A2	I/O
C3	DCLK
B5	GND A
E12	GND A
J2	GND A
M9	GND A
B9	GND I
C5	GND I
E11	GND I
F4	GND I
J3	GND I
J11	GND I
L5	GND I
L9	GND I
C9	GND Q
E3	GND Q
K12	GND Q
D7	VCCA
G3	VCCA
G10	VCCA
L7	VCCA
C7	VCCI
G2	VCCI
G11	VCCI
K7	VCCI