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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                                                 |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                                                        |
| Number of LABs/CLBs            | -                                                                                                                                                               |
| Number of Logic Elements/Cells | -                                                                                                                                                               |
| Total RAM Bits                 | -                                                                                                                                                               |
| Number of I/O                  | 125                                                                                                                                                             |
| Number of Gates                | 36000                                                                                                                                                           |
| Voltage - Supply               | 3V ~ 3.6V, 4.5V ~ 5.5V                                                                                                                                          |
| Mounting Type                  | Surface Mount                                                                                                                                                   |
| Operating Temperature          | -40°C ~ 85°C (TA)                                                                                                                                               |
| Package / Case                 | 160-BQFP                                                                                                                                                        |
| Supplier Device Package        | 160-PQFP (28x28)                                                                                                                                                |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/microchip-technology/a42mx24-pq160i">https://www.e-xfl.com/product-detail/microchip-technology/a42mx24-pq160i</a> |

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# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- Table 15, page 21 is edited to add the footnote,  $V_{IH}(\text{Min})$  is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 22, page 25 is edited to add the footnote,  $V_{IH}(\text{Min})$  is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 23, page 25 is edited to add the footnote,  $V_{IH}(\text{Min})$  is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

## 1.2 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Added CQFP package information for A42MX16 device in Product Profile, page 1 and Ceramic Device Resources, page 4 (SAR 79522).
- Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in Temperature Grade Offerings, page 5 (SAR 79519)
- Changed Silicon Sculptor II to Silicon Sculptor in Programming, page 12 (SAR 38754)
- Added Figure 53, page 158 CQ172 package (SAR 79522).

## 1.3 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Added Figure 42, page 97 PQ144 Package for A42MX09 device (SAR 69776)
- Added Figure 52, page 153 PQ132 Package for A42MX09 device (SAR 69776)

## 1.4 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Added information on power-up behavior for A42MX24 and A42MX36 devices to the Power Supply, page 13 (SAR 42096)
- Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793)

## 1.5 Revision 11.0

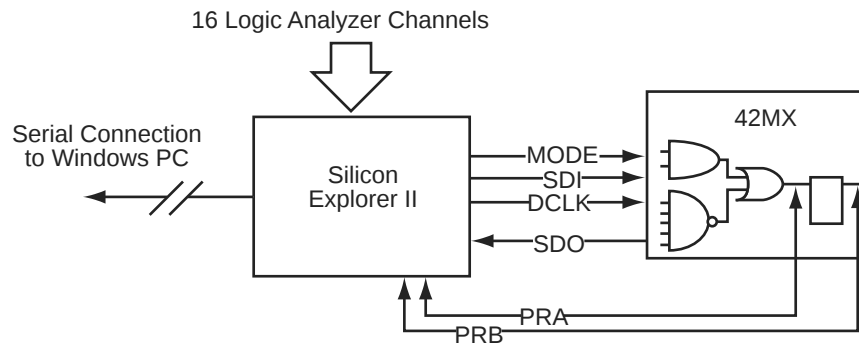
The following is a summary of the changes in revision 11.0 of this document.

- The FuseLock logo and accompanying text was removed from the User Security, page 12. This marking is no longer used on Microsemi devices (PCN 0915)
- The Development Tool Support, page 19 was updated (SAR 38512)

## 1.6 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- Ordering Information, page 3 was updated to include lead-free package ordering codes (SAR 21968)
- The User Security, page 12 was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673)

**Figure 13 • Silicon Explorer II Setup with 42MX****Table 8 • Device Configuration Options for Probe Capability**

| Security Fuse(s) Programmed | Mode | PRA, PRB <sup>1</sup>  | SDI, SDO, DCLK <sup>1</sup> |
|-----------------------------|------|------------------------|-----------------------------|
| No                          | LOW  | User I/Os <sup>2</sup> | User I/Os <sup>2</sup>      |
| No                          | HIGH | Probe Circuit Outputs  | Probe Circuit Inputs        |
| Yes                         | –    | Probe Circuit Secured  | Probe Circuit Secured       |

1. Avoid using SDI, SDO, DCLK, PRA and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.
2. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. See the Pin Descriptions, page 83 for information on unused I/O pins

### 3.4.7 Design Consideration

It is recommended to use a series 70 $\Omega$  termination resistor on every probe connector (SDI, SDO, MODE, DCLK, PRA and PRB). The 70  $\Omega$  series termination is used to prevent data transmission corruption during probing and reading back the checksum.

### 3.4.8 IEEE Standard 1149.1 Boundary Scan Test (BST) Circuitry

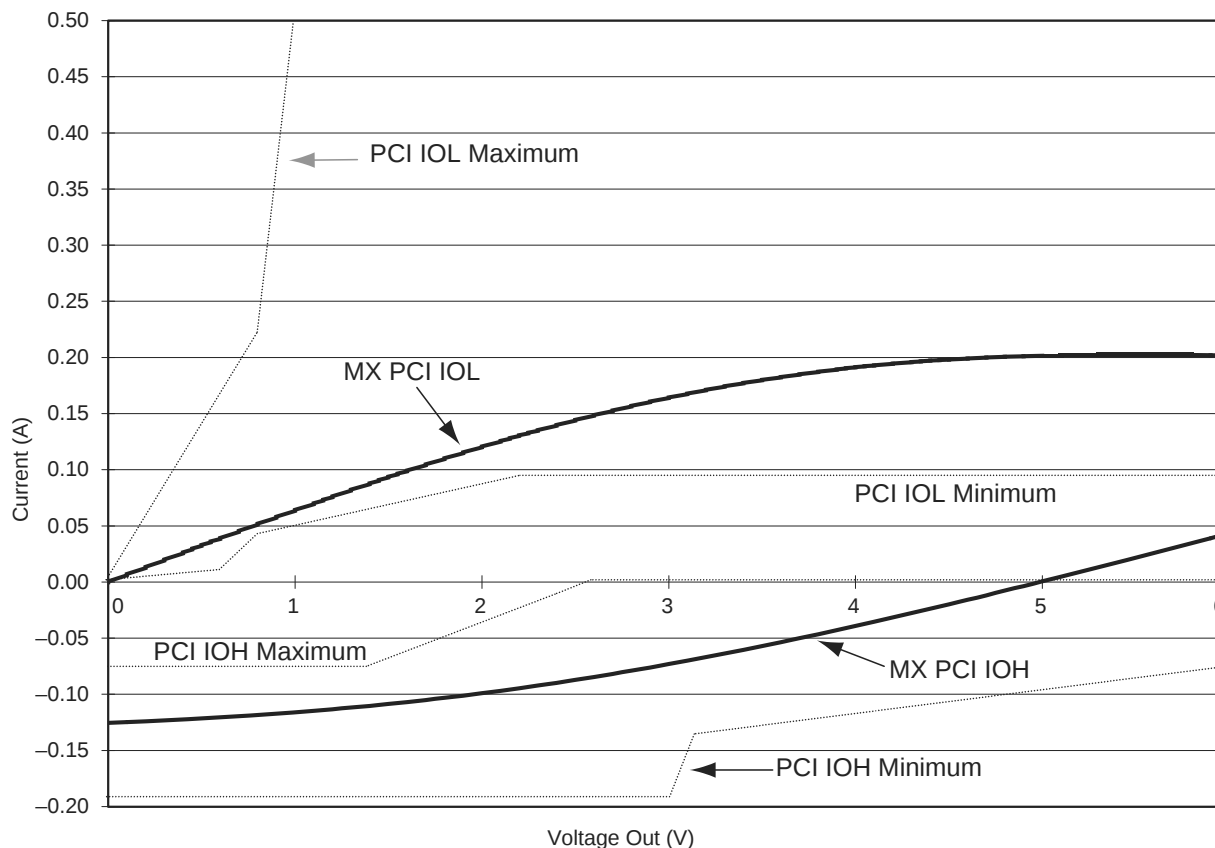
42MX24 and 42MX36 devices are compatible with IEEE Standard 1149.1 (informally known as Joint Testing Action Group Standard or JTAG), which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic MX boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers and instruction register (Figure 14, page 18). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and some optional instructions. Table 9, page 18 describes the ports that control JTAG testing, while Table 10, page 18 describes the test instructions supported by these MX devices.

Each test section is accessed through the TAP, which has four associated pins: TCK (test clock input), TDI and TDO (test data input and output), and TMS (test mode selector).

The TAP controller is a four-bit state machine. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles.

42MX24 and 42MX36 devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

**Figure 16 • Typical Output Drive Characteristics (Based Upon Measured Data)**

### 3.9.4 Junction Temperature ( $T_J$ )

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a(1)$$

EQ 4

where:

- $T_a$  = Ambient Temperature
- $\Delta T$  = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$  (2)
- $P$  = Power
- $\theta_{ja}$  = Junction to ambient of package.  $\theta_{ja}$  numbers are located in Table 27, page 29.

### 3.9.5 Package Thermal Characteristics

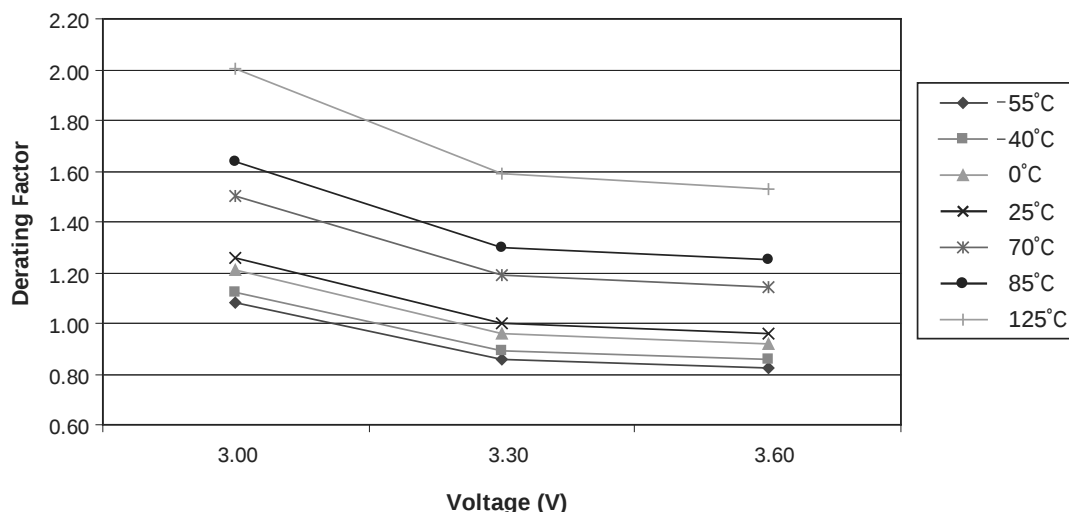
The device junction-to-case thermal characteristic is  $\theta_{jc}$ , and the junction-to-ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates.

The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of  $\theta_{ja}$ .

**Table 31 • 40MX Temperature and Voltage Derating Factors (Normalized to T<sub>J</sub> = 25°C, V<sub>CC</sub> = 3.3 V)**

| 40MX Voltage | Temperature |       |      |      |      |      |       |
|--------------|-------------|-------|------|------|------|------|-------|
|              | -55°C       | -40°C | 0°C  | 25°C | 70°C | 85°C | 125°C |
| 3.60         | 0.83        | 0.85  | 0.92 | 0.96 | 1.14 | 1.25 | 1.53  |

**Figure 37 • 40MX Junction Temperature and Voltage Derating Curves (Normalized to T<sub>J</sub> = 25°C, V<sub>CC</sub> = 3.3 V)**

**Note:** This derating factor applies to all routing and propagation delays

### 3.11.5 PCI System Timing Specification

The following tables list the critical PCI timing parameters and the corresponding timing parameters for the MX PCI-compliant devices.

### 3.11.6 PCI Models

Microsemi provides synthesizable VHDL and Verilog-HDL models for a PCI Target interface, a PCI Target and Target+DMA Master interface. Contact the Microsemi sales representative for more details.

**Table 32 • Clock Specification for 33 MHz PCI**

| Symbol            | Parameter      | PCI  |      | A42MX24 |      | A42MX36 |      | Units |
|-------------------|----------------|------|------|---------|------|---------|------|-------|
|                   |                | Min. | Max. | Min.    | Max. | Min.    | Max. |       |
| t <sub>CYC</sub>  | CLK Cycle Time | 30   | –    | 4.0     | –    | 4.0     | –    | ns    |
| t <sub>HIGH</sub> | CLK High Time  | 11   | –    | 1.9     | –    | 1.9     | –    | ns    |
| t <sub>LOW</sub>  | CLK Low Time   | 11   | –    | 1.9     | –    | 1.9     | –    | ns    |

**Table 33 • Timing Parameters for 33 MHz PCI**

| Symbol                | Parameter                              | PCI            |      | A42MX24 |                  | A42MX36 |                  | Units |
|-----------------------|----------------------------------------|----------------|------|---------|------------------|---------|------------------|-------|
|                       |                                        | Min.           | Max. | Min.    | Max.             | Min.    | Max.             |       |
| t <sub>VAL</sub>      | CLK to Signal Valid—Bused Signals      | 2              | 11   | 2.0     | 9.0              | 2.0     | 9.0              | ns    |
| t <sub>VAL(PTP)</sub> | CLK to Signal Valid—Point-to-Point     | 2 <sup>2</sup> | 12   | 2.0     | 9.0              | 2.0     | 9.0              | ns    |
| t <sub>ON</sub>       | Float to Active                        | 2              | –    | 2.0     | 4.0              | 2.0     | 4.0              | ns    |
| t <sub>OFF</sub>      | Active to Float                        | –              | 28   | –       | 8.3 <sup>1</sup> | –       | 8.3 <sup>1</sup> | ns    |
| t <sub>SU</sub>       | Input Set-Up Time to CLK—Bused Signals | 7              | –    | 1.5     | –                | 1.5     | –                | ns    |

**Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)**  
**(Worst-Case Commercial Conditions, VCC = 3.0 V, T<sub>J</sub> = 70°C)**

| Parameter / Description               |                      |          | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|---------------------------------------|----------------------|----------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                       |                      |          | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| t <sub>p</sub>                        | Minimum Period       | FO = 16  | 6.5      |      | 7.5      |      | 8.5      |      | 10.1      |      | 14.1     |      | ns    |
|                                       |                      | FO = 128 | 6.8      |      | 7.8      |      | 8.9      |      | 10.4      |      | 14.6     |      |       |
| f <sub>MAX</sub>                      | Maximum Frequency    | FO = 16  |          | 113  |          | 105  |          | 96   |           | 83   |          | 50   | MHz   |
|                                       |                      | FO = 128 |          | 109  |          | 101  |          | 92   |           | 80   |          | 48   |       |
| TTL Output Module Timing <sup>4</sup> |                      |          |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>DLH</sub>                      | Data-to-Pad HIGH     |          |          | 4.7  |          | 5.4  |          | 6.1  |           | 7.2  |          | 10.0 | ns    |
| t <sub>DHL</sub>                      | Data-to-Pad LOW      |          |          | 5.6  |          | 6.4  |          | 7.3  |           | 8.6  |          | 12.0 | ns    |
| t <sub>ENZH</sub>                     | Enable Pad Z to HIGH |          |          | 5.2  |          | 6.0  |          | 6.8  |           | 8.1  |          | 11.3 | ns    |
| t <sub>ENZL</sub>                     | Enable Pad Z to LOW  |          |          | 6.6  |          | 7.6  |          | 8.6  |           | 10.1 |          | 14.1 | ns    |
| t <sub>ENHZ</sub>                     | Enable Pad HIGH to Z |          |          | 11.1 |          | 12.8 |          | 14.5 |           | 17.1 |          | 23.9 | ns    |
| t <sub>ENLZ</sub>                     | Enable Pad LOW to Z  |          |          | 8.2  |          | 9.5  |          | 10.7 |           | 12.6 |          | 17.7 | ns    |
| d <sub>TLH</sub>                      | Delta LOW to HIGH    |          |          | 0.03 |          | 0.03 |          | 0.04 |           | 0.04 |          | 0.06 | ns/pF |
| d <sub>THL</sub>                      | Delta HIGH to LOW    |          |          | 0.04 |          | 0.04 |          | 0.05 |           | 0.06 |          | 0.08 | ns/pF |

**Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)**(Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C)

| Parameter / Description |                     | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|-------------------------|---------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                         |                     | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| t <sub>ENLZ</sub>       | Enable Pad LOW to Z |          | 5.9  |          | 6.8  |          | 7.7  |           | 9.0  |          | 12.6 | ns    |
| d <sub>TLH</sub>        | Delta LOW to HIGH   |          | 0.02 |          | 0.02 |          | 0.03 |           | 0.03 |          | 0.04 | ns/pF |
| d <sub>THL</sub>        | Delta HIGH to LOW   |          | 0.03 |          | 0.03 |          | 0.03 |           | 0.04 |          | 0.06 | ns/pF |

**Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T<sub>J</sub> = 70°C)**

| Parameter / Description               |                                                          | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|---------------------------------------|----------------------------------------------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                       |                                                          | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| TTL Output Module Timing <sup>5</sup> |                                                          |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>DLH</sub>                      | Data-to-Pad HIGH                                         |          | 2.5  |          | 2.7  |          | 3.1  |           | 3.6  |          | 5.1  | ns    |
| t <sub>DHL</sub>                      | Data-to-Pad LOW                                          |          | 2.9  |          | 3.2  |          | 3.6  |           | 4.3  |          | 6.0  | ns    |
| t <sub>ENZH</sub>                     | Enable Pad Z to HIGH                                     |          | 2.6  |          | 2.9  |          | 3.3  |           | 3.9  |          | 5.5  | ns    |
| t <sub>ENZL</sub>                     | Enable Pad Z to LOW                                      |          | 2.9  |          | 3.2  |          | 3.7  |           | 4.3  |          | 6.1  | ns    |
| t <sub>ENHZ</sub>                     | Enable Pad HIGH to Z                                     |          | 4.9  |          | 5.4  |          | 6.2  |           | 7.3  |          | 10.2 | ns    |
| t <sub>ENLZ</sub>                     | Enable Pad LOW to Z                                      |          | 5.3  |          | 5.9  |          | 6.7  |           | 7.9  |          | 11.1 | ns    |
| t <sub>GLH</sub>                      | G-to-Pad HIGH                                            |          | 2.6  |          | 2.9  |          | 3.3  |           | 3.8  |          | 5.3  | ns    |
| t <sub>GHL</sub>                      | G-to-Pad LOW                                             |          | 2.6  |          | 2.9  |          | 3.3  |           | 3.8  |          | 5.3  | ns    |
| t <sub>LSU</sub>                      | I/O Latch Set-Up                                         | 0.5      |      | 0.5      |      | 0.6      |      | 0.7       |      | 1.0      |      | ns    |
| t <sub>LH</sub>                       | I/O Latch Hold                                           | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>LCO</sub>                      | I/O Latch Clock-to-Out<br>(Pad-to-Pad), 64 Clock Loading |          | 5.2  |          | 5.8  |          | 6.6  |           | 7.7  |          | 10.8 | ns    |
| t <sub>ACO</sub>                      | Array Clock-to-Out<br>(Pad-to-Pad), 64 Clock Loading     |          | 7.4  |          | 8.2  |          | 9.3  |           | 10.9 |          | 15.3 | ns    |
| d <sub>TLH</sub>                      | Capacity Loading, LOW to HIGH                            |          | 0.03 |          | 0.03 |          | 0.03 |           | 0.04 |          | 0.06 | ns/pF |
| d <sub>THL</sub>                      | Capacity Loading, HIGH to LOW                            |          | 0.04 |          | 0.04 |          | 0.04 |           | 0.05 |          | 0.07 | ns/pF |

**Table 41 • A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T<sub>J</sub> = 70°C)**

| Parameter / Description |                                                   | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|-------------------------|---------------------------------------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                         |                                                   | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| t <sub>ACO</sub>        | Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading |          | 11.3 |          | 12.5 |          | 14.2 |           | 16.7 |          | 23.3 | ns    |
| d <sub>TLH</sub>        | Capacitive Loading, LOW to HIGH                   |          | 0.04 |          | 0.04 |          | 0.05 |           | 0.06 |          | 0.08 | ns/pF |
| d <sub>THL</sub>        | Capacitive Loading, HIGH to LOW                   |          | 0.05 |          | 0.05 |          | 0.06 |           | 0.07 |          | 0.10 | ns/pF |

1. For dual-module macros use tPD1 + tRD1 + taped, to + tRD1 + taped, or tPD1 + tRD1 + tusk, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

**Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T<sub>J</sub> = 70°C)**

| Parameter / Description                            |                                               | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|----------------------------------------------------|-----------------------------------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                                    |                                               | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| Logic Module Combinatorial Functions <sup>1</sup>  |                                               |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>PD</sub>                                    | Internal Array Module Delay                   |          | 1.2  |          | 1.3  |          | 1.5  |           | 1.8  |          | 2.5  | ns    |
| t <sub>PDD</sub>                                   | Internal Decode Module Delay                  |          | 1.4  |          | 1.6  |          | 1.8  |           | 2.1  |          | 3.0  | ns    |
| Logic Module Predicted Routing Delays <sup>2</sup> |                                               |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>RD1</sub>                                   | FO = 1 Routing Delay                          |          | 0.8  |          | 0.9  |          | 1.0  |           | 1.2  |          | 1.7  | ns    |
| t <sub>RD2</sub>                                   | FO = 2 Routing Delay                          |          | 1.0  |          | 1.2  |          | 1.3  |           | 1.5  |          | 2.1  | ns    |
| t <sub>RD3</sub>                                   | FO = 3 Routing Delay                          |          | 1.3  |          | 1.4  |          | 1.6  |           | 1.9  |          | 2.6  | ns    |
| t <sub>RD4</sub>                                   | FO = 4 Routing Delay                          |          | 1.5  |          | 1.7  |          | 1.9  |           | 2.2  |          | 3.1  | ns    |
| t <sub>RD5</sub>                                   | FO = 8 Routing Delay                          |          | 2.4  |          | 2.7  |          | 3.0  |           | 3.6  |          | 5.0  | ns    |
| Logic Module Sequential Timing <sup>3, 4</sup>     |                                               |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>CO</sub>                                    | Flip-Flop Clock-to-Output                     |          | 1.3  |          | 1.4  |          | 1.6  |           | 1.9  |          | 2.7  | ns    |
| t <sub>GO</sub>                                    | Latch Gate-to-Output                          |          | 1.2  |          | 1.3  |          | 1.5  |           | 1.8  |          | 2.5  | ns    |
| t <sub>SUD</sub>                                   | Flip-Flop (Latch) Set-Up Time                 | 0.3      |      | 0.4      |      | 0.4      |      | 0.5       |      | 0.7      |      | ns    |
| t <sub>HD</sub>                                    | Flip-Flop (Latch) Hold Time                   | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>RO</sub>                                    | Flip-Flop (Latch) Reset-to-Output             |          | 1.4  |          | 1.6  |          | 1.8  |           | 2.1  |          | 2.9  | ns    |
| t <sub>SUENA</sub>                                 | Flip-Flop (Latch) Enable Set-Up               | 0.4      |      | 0.5      |      | 0.5      |      | 0.6       |      | 0.8      |      | ns    |
| t <sub>HENA</sub>                                  | Flip-Flop (Latch) Enable Hold                 | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>WCLKA</sub>                                 | Flip-Flop (Latch)<br>Clock Active Pulse Width | 3.3      |      | 3.7      |      | 4.2      |      | 4.9       |      | 6.9      |      | ns    |
| t <sub>WASYN</sub>                                 | Flip-Flop (Latch)<br>Asynchronous Pulse Width | 4.4      |      | 4.8      |      | 5.3      |      | 6.5       |      | 9.0      |      | ns    |

**Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)**(Worst-Case Commercial Conditions, VCCA = 3.0 V, T<sub>J</sub> = 70°C)

| Parameter / Description                                       | –3 Speed |      | –2 Speed |      | –1 Speed |      | Std Speed |      | –F Speed |      | Units |
|---------------------------------------------------------------|----------|------|----------|------|----------|------|-----------|------|----------|------|-------|
|                                                               | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.      | Max. | Min.     | Max. |       |
| t <sub>ACO</sub> Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O |          | 10.9 |          | 12.1 |          | 13.7 |           | 16.1 |          | 22.5 | ns    |
| d <sub>TLH</sub> Capacitive Loading, LOW to HIGH              |          | 0.10 |          | 0.11 |          | 0.12 |           | 0.14 |          | 0.20 | ns/pF |
| d <sub>THL</sub> Capacitive Loading, HIGH to LOW              |          | 0.10 |          | 0.11 |          | 0.12 |           | 0.14 |          | 0.20 | ns/pF |
| <b>CMOS Output Module Timing<sup>5</sup></b>                  |          |      |          |      |          |      |           |      |          |      |       |
| t <sub>DLH</sub> Data-to-Pad HIGH                             |          | 4.9  |          | 5.5  |          | 6.2  |           | 7.3  |          | 10.3 | ns    |
| t <sub>DHL</sub> Data-to-Pad LOW                              |          | 3.4  |          | 3.8  |          | 4.3  |           | 5.1  |          | 7.1  | ns    |
| t <sub>ENZH</sub> Enable Pad Z to HIGH                        |          | 3.7  |          | 4.1  |          | 4.7  |           | 5.5  |          | 7.7  | ns    |
| t <sub>ENZL</sub> Enable Pad Z to LOW                         |          | 4.1  |          | 4.6  |          | 5.2  |           | 6.1  |          | 8.5  | ns    |
| t <sub>ENHZ</sub> Enable Pad HIGH to Z                        |          | 7.4  |          | 8.2  |          | 9.3  |           | 10.9 |          | 15.3 | ns    |
| t <sub>ENLZ</sub> Enable Pad LOW to Z                         |          | 6.9  |          | 7.6  |          | 8.7  |           | 10.2 |          | 14.3 | ns    |
| t <sub>GLH</sub> G-to-Pad HIGH                                |          | 7.0  |          | 7.8  |          | 8.9  |           | 10.4 |          | 14.6 | ns    |
| t <sub>GHL</sub> G-to-Pad LOW                                 |          | 7.0  |          | 7.8  |          | 8.9  |           | 10.4 |          | 14.6 | ns    |
| t <sub>LSU</sub> I/O Latch Set-Up                             | 0.7      |      | 0.7      |      | 0.8      |      | 1.0       |      | 1.4      |      | ns    |
| t <sub>LH</sub> I/O Latch Hold                                | 0.0      |      | 0.0      |      | 0.0      |      | 0.0       |      | 0.0      |      | ns    |
| t <sub>LCO</sub> I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O   |          | 7.9  |          | 8.8  |          | 10.0 |           | 11.8 |          | 16.5 | ns    |

1. For dual-module macros, use t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

## 3.12 Pin Descriptions

This section lists the pin descriptions for 40MX and 42MX series FPGAs.

### CLK/A/B, I/O Global Clock

Clock inputs for clock distribution networks. CLK is for 40MX while CLKA and CLKB are for 42MX devices. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

### DCLK, I/O Diagnostic Clock

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### GND, Ground

Input LOW supply voltage.

### I/O, Input/Output

Clock signal to shift the Boundary Scan Test (BST) data into the device. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

**TDI, I/O Test Data In**

Serial data input for BST instructions and data. Data is shifted in on the rising edge of TCK. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

**TDO, I/O Test Data Out**

Serial data output for BST instructions and test data. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

**TMS, I/O Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI and TDO pins are boundary scan pins. Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications. IEEE JTAG specification recommends a 10k $\Omega$  pull-up resistor on the pin. BST pins are only available in A42MX24 and A42MX36 devices.

**VCC, Supply Voltage**

Input supply voltage for 40MX devices

**VCCA, Supply Voltage**

Supply voltage for array in 42MX devices

**VCCI, Supply Voltage**

Supply voltage for I/Os in 42MX devices

**WD, I/O Wide Decode Output**

When a wide decode module is used in a 42MX device this pin can be used as a dedicated output from the wide decode module. This direct connection eliminates additional interconnect delays associated with regular logic modules. To implement the direct I/O connection, connect an output buffer of any type to the output of the wide decode macro and place this output on one of the reserved WD pins.

**Table 52 • PQ160**

| <b>PQ160</b>      |                         |                         |                         |
|-------------------|-------------------------|-------------------------|-------------------------|
| <b>Pin Number</b> | <b>A42MX09 Function</b> | <b>A42MX16 Function</b> | <b>A42MX24 Function</b> |
| 132               | I/O                     | I/O                     | I/O                     |
| 133               | I/O                     | I/O                     | I/O                     |
| 134               | I/O                     | I/O                     | I/O                     |
| 135               | NC                      | VCCA                    | VCCA                    |
| 136               | I/O                     | I/O                     | I/O                     |
| 137               | I/O                     | I/O                     | I/O                     |
| 138               | NC                      | VCCA                    | VCCA                    |
| 139               | VCCI                    | VCCI                    | VCCI                    |
| 140               | GND                     | GND                     | GND                     |
| 141               | NC                      | I/O                     | I/O                     |
| 142               | I/O                     | I/O                     | I/O                     |
| 143               | I/O                     | I/O                     | I/O                     |
| 144               | I/O                     | I/O                     | I/O                     |
| 145               | GND                     | GND                     | GND                     |
| 146               | NC                      | I/O                     | I/O                     |
| 147               | I/O                     | I/O                     | I/O                     |
| 148               | I/O                     | I/O                     | I/O                     |
| 149               | I/O                     | I/O                     | I/O                     |
| 150               | NC                      | VCCA                    | VCCA                    |
| 151               | NC                      | I/O                     | I/O                     |
| 152               | NC                      | I/O                     | I/O                     |
| 153               | NC                      | I/O                     | I/O                     |
| 154               | NC                      | I/O                     | I/O                     |
| 155               | GND                     | GND                     | GND                     |
| 156               | I/O                     | I/O                     | I/O                     |
| 157               | I/O                     | I/O                     | I/O                     |
| 158               | I/O                     | I/O                     | I/O                     |
| 159               | MODE                    | MODE                    | MODE                    |
| 160               | GND                     | GND                     | GND                     |

**Table 54 • PQ240**

| <b>PQ240</b>      |                         |
|-------------------|-------------------------|
| <b>Pin Number</b> | <b>A42MX36 Function</b> |
| 15                | QCLKC, I/O              |
| 16                | I/O                     |
| 17                | WD, I/O                 |
| 18                | WD, I/O                 |
| 19                | I/O                     |
| 20                | I/O                     |
| 21                | WD, I/O                 |
| 22                | WD, I/O                 |
| 23                | I/O                     |
| 24                | PRB, I/O                |
| 25                | I/O                     |
| 26                | CLKB, I/O               |
| 27                | I/O                     |
| 28                | GND                     |
| 29                | VCCA                    |
| 30                | VCCI                    |
| 31                | I/O                     |
| 32                | CLKA, I/O               |
| 33                | I/O                     |
| 34                | PRA, I/O                |
| 35                | I/O                     |
| 36                | I/O                     |
| 37                | WD, I/O                 |
| 38                | WD, I/O                 |
| 39                | I/O                     |
| 40                | I/O                     |
| 41                | I/O                     |
| 42                | I/O                     |
| 43                | I/O                     |
| 44                | I/O                     |
| 45                | QCLKD, I/O              |
| 46                | I/O                     |
| 47                | WD, I/O                 |
| 48                | WD, I/O                 |
| 49                | I/O                     |
| 50                | I/O                     |
| 51                | I/O                     |

**Table 55 • VQ80**

| <b>VQ80</b>       |                             |                             |
|-------------------|-----------------------------|-----------------------------|
| <b>Pin Number</b> | <b>A40MX02<br/>Function</b> | <b>A40MX04<br/>Function</b> |
| 49                | I/O                         | I/O                         |
| 50                | CLK, I/O                    | CLK, I/O                    |
| 51                | I/O                         | I/O                         |
| 52                | MODE                        | MODE                        |
| 53                | VCC                         | VCC                         |
| 54                | NC                          | I/O                         |
| 55                | NC                          | I/O                         |
| 56                | NC                          | I/O                         |
| 57                | SDI, I/O                    | SDI, I/O                    |
| 58                | DCLK, I/O                   | DCLK, I/O                   |
| 59                | PRA, I/O                    | PRA, I/O                    |
| 60                | NC                          | NC                          |
| 61                | PRB, I/O                    | PRB, I/O                    |
| 62                | I/O                         | I/O                         |
| 63                | I/O                         | I/O                         |
| 64                | I/O                         | I/O                         |
| 65                | I/O                         | I/O                         |
| 66                | I/O                         | I/O                         |
| 67                | I/O                         | I/O                         |
| 68                | GND                         | GND                         |
| 69                | I/O                         | I/O                         |
| 70                | I/O                         | I/O                         |
| 71                | I/O                         | I/O                         |
| 72                | I/O                         | I/O                         |
| 73                | I/O                         | I/O                         |
| 74                | VCC                         | <b>VCC</b>                  |
| 75                | I/O                         | I/O                         |
| 76                | I/O                         | I/O                         |
| 77                | I/O                         | I/O                         |
| 78                | I/O                         | I/O                         |
| 79                | I/O                         | I/O                         |
| 80                | I/O                         | I/O                         |

**Table 56 • VQ100**

| <b>VQ100</b>      |                             |                             |
|-------------------|-----------------------------|-----------------------------|
| <b>Pin Number</b> | <b>A42MX09<br/>Function</b> | <b>A42MX16<br/>Function</b> |
| 21                | I/O                         | I/O                         |
| 22                | I/O                         | I/O                         |
| 23                | I/O                         | I/O                         |
| 24                | I/O                         | I/O                         |
| 25                | I/O                         | I/O                         |
| 26                | I/O                         | I/O                         |
| 27                | I/O                         | I/O                         |
| 28                | I/O                         | I/O                         |
| 29                | I/O                         | I/O                         |
| 30                | I/O                         | I/O                         |
| 31                | I/O                         | I/O                         |
| 32                | GND                         | GND                         |
| 33                | I/O                         | I/O                         |
| 34                | I/O                         | I/O                         |
| 35                | I/O                         | I/O                         |
| 36                | I/O                         | I/O                         |
| 37                | I/O                         | I/O                         |
| 38                | VCCA                        | VCCA                        |
| 39                | I/O                         | I/O                         |
| 40                | I/O                         | I/O                         |
| 41                | I/O                         | I/O                         |
| 42                | I/O                         | I/O                         |
| 43                | I/O                         | I/O                         |
| 44                | GND                         | GND                         |
| 45                | I/O                         | I/O                         |
| 46                | I/O                         | I/O                         |
| 47                | I/O                         | I/O                         |
| 48                | I/O                         | I/O                         |
| 49                | I/O                         | I/O                         |
| 50                | SDO, I/O                    | SDO, I/O                    |
| 51                | I/O                         | I/O                         |
| 52                | I/O                         | I/O                         |
| 53                | I/O                         | I/O                         |
| 54                | I/O                         | I/O                         |
| 55                | GND                         | GND                         |
| 56                | I/O                         | I/O                         |

**Table 58 • CQ208**

| <b>CQ208</b>      |                         |
|-------------------|-------------------------|
| <b>Pin Number</b> | <b>A42MX36 Function</b> |
| 74                | I/O                     |
| 75                | I/O                     |
| 76                | I/O                     |
| 77                | I/O                     |
| 78                | GND                     |
| 79                | VCCA                    |
| 80                | VCCI                    |
| 81                | I/O                     |
| 82                | I/O                     |
| 83                | I/O                     |
| 84                | I/O                     |
| 85                | WD, I/O                 |
| 86                | WD, I/O                 |
| 87                | I/O                     |
| 88                | I/O                     |
| 89                | I/O                     |
| 90                | I/O                     |
| 91                | QCLKB, I/O              |
| 92                | I/O                     |
| 93                | WD, I/O                 |
| 94                | WD, I/O                 |
| 95                | I/O                     |
| 96                | I/O                     |
| 97                | I/O                     |
| 98                | VCCI                    |
| 99                | I/O                     |
| 100               | WD, I/O                 |
| 101               | WD, I/O                 |
| 102               | I/O                     |
| 103               | TDO, I/O                |
| 104               | I/O                     |
| 105               | GND                     |
| 106               | VCCA                    |
| 107               | I/O                     |
| 108               | I/O                     |
| 109               | I/O                     |
| 110               | I/O                     |

**Table 58 • CQ208**

| <b>CQ208</b>      |                         |
|-------------------|-------------------------|
| <b>Pin Number</b> | <b>A42MX36 Function</b> |
| 185               | I/O                     |
| 186               | CLKB, I/O               |
| 187               | I/O                     |
| 188               | PRB, I/O                |
| 189               | I/O                     |
| 190               | WD, I/O                 |
| 191               | WD, I/O                 |
| 192               | I/O                     |
| 193               | I/O                     |
| 194               | WD, I/O                 |
| 195               | WD, I/O                 |
| 196               | QCLKC, I/O              |
| 197               | I/O                     |
| 198               | I/O                     |
| 199               | I/O                     |
| 200               | I/O                     |
| 201               | I/O                     |
| 202               | VCCI                    |
| 203               | WD, I/O                 |
| 204               | WD, I/O                 |
| 205               | I/O                     |
| 206               | I/O                     |
| 207               | DCLK, I/O               |
| 208               | I/O                     |

**Table 59 • CQ256**

| <b>CQ256</b>      |                         |
|-------------------|-------------------------|
| <b>Pin Number</b> | <b>A42MX36 Function</b> |
| 133               | I/O                     |
| 134               | I/O                     |
| 135               | I/O                     |
| 136               | I/O                     |
| 137               | I/O                     |
| 138               | I/O                     |
| 139               | GND                     |
| 140               | I/O                     |
| 141               | I/O                     |
| 142               | I/O                     |
| 143               | I/O                     |
| 144               | I/O                     |
| 145               | I/O                     |
| 146               | I/O                     |
| 147               | I/O                     |
| 148               | I/O                     |
| 149               | I/O                     |
| 150               | I/O                     |
| 151               | I/O                     |
| 152               | I/O                     |
| 153               | I/O                     |
| 154               | I/O                     |
| 155               | VCCA                    |
| 156               | I/O                     |
| 157               | I/O                     |
| 158               | VCCA                    |
| 159               | VCCI                    |
| 160               | GND                     |
| 161               | I/O                     |
| 162               | I/O                     |
| 163               | I/O                     |
| 164               | I/O                     |
| 165               | GND                     |
| 166               | I/O                     |
| 167               | I/O                     |
| 168               | I/O                     |
| 169               | I/O                     |

**Table 62 • CQ172**

|    |        |
|----|--------|
| 21 | I/O    |
| 22 | GND    |
| 23 | VCCI   |
| 24 | VSV    |
| 25 | I/O    |
| 26 | I/O    |
| 27 | VCC    |
| 28 | I/O    |
| 29 | I/O    |
| 30 | I/O    |
| 31 | I/O    |
| 32 | GND    |
| 33 | I/O    |
| 34 | I/O    |
| 35 | I/O    |
| 36 | I/O    |
| 37 | GND    |
| 38 | I/O    |
| 39 | I/O    |
| 40 | I/O    |
| 41 | I/O    |
| 42 | I/O    |
| 43 | I/O    |
| 44 | BININ  |
| 45 | BINOUT |
| 46 | I/O    |
| 47 | I/O    |
| 48 | I/O    |
| 49 | I/O    |
| 50 | VCCI   |
| 51 | I/O    |
| 52 | I/O    |
| 53 | I/O    |
| 54 | I/O    |
| 55 | GND    |
| 56 | I/O    |
| 57 | I/O    |
| 58 | I/O    |
| 59 | I/O    |

**Table 62 • CQ172**

|    |      |
|----|------|
| 60 | I/O  |
| 61 | I/O  |
| 62 | I/O  |
| 63 | I/O  |
| 64 | I/O  |
| 65 | GND  |
| 66 | VCC  |
| 67 | I/O  |
| 68 | I/O  |
| 69 | I/O  |
| 70 | I/O  |
| 71 | I/O  |
| 72 | I/O  |
| 73 | I/O  |
| 74 | I/O  |
| 75 | GND  |
| 76 | I/O  |
| 77 | I/O  |
| 78 | I/O  |
| 79 | I/O  |
| 80 | VCCI |
| 81 | I/O  |
| 82 | I/O  |
| 83 | I/O  |
| 84 | I/O  |
| 85 | SDO  |
| 86 | I/O  |
| 87 | I/O  |
| 88 | I/O  |
| 89 | I/O  |
| 90 | I/O  |
| 91 | I/O  |
| 92 | I/O  |
| 93 | I/O  |
| 94 | I/O  |
| 95 | I/O  |
| 96 | I/O  |
| 97 | I/O  |
| 98 | GND  |