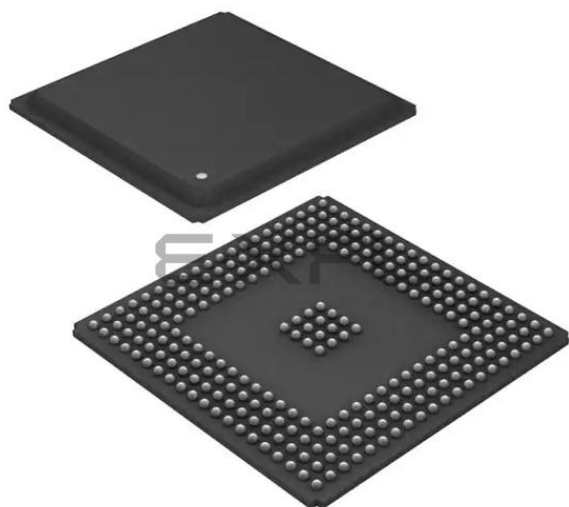




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	2560
Number of I/O	202
Number of Gates	54000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx36-1bg272m

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- Table 15, page 21 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 22, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 23, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

1.2 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Added CQFP package information for A42MX16 device in Product Profile, page 1 and Ceramic Device Resources, page 4 (SAR 79522).
- Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in Temperature Grade Offerings, page 5 (SAR 79519)
- Changed Silicon Sculptor II to Silicon Sculptor in Programming, page 12 (SAR 38754)
- Added Figure 53, page 158 CQ172 package (SAR 79522).

1.3 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Added Figure 42, page 97 PQ144 Package for A42MX09 device (SAR 69776)
- Added Figure 52, page 153 PQ132 Package for A42MX09 device (SAR 69776)

1.4 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Added information on power-up behavior for A42MX24 and A42MX36 devices to the Power Supply, page 13 (SAR 42096)
- Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793)

1.5 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- The FuseLock logo and accompanying text was removed from the User Security, page 12. This marking is no longer used on Microsemi devices (PCN 0915)
- The Development Tool Support, page 19 was updated (SAR 38512)

1.6 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- Ordering Information, page 3 was updated to include lead-free package ordering codes (SAR 21968)
- The User Security, page 12 was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673)

2.6 Temperature Grade Offerings

Table 4 • Temperature Grade Offerings

Package	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PLCC 44	C, I, M	C, I, M				
PLCC 68	C, I, A, M	C, I, M				
PLCC 84		C, I, A, M	C, I, A, M	C, I, M	C, I, M	
PQFP 100	C, I, A, M	C, I, A, M	C, I, A, M	C, I, M		
PQFP 144			C			
PQFP 160			C, I, A, M	C, I, M	C, I, A, M	
PQFP 208				C, I, A, M	C, I, A, M	C, I, A, M
PQFP 240						C, I, A, M
VQFP 80	C, I, A, M	C, I, A, M				
VQFP 100			C, I, A, M	C, I, A, M		
TQFP 176			C, I, A, M	C, I, A, M	C, I, A, M	
PBGA 272						C, I, M
CQFP 172				C, M, B		
CQFP 208						C, M, B
CQFP 256						C, M, B
CPGA 132			C, M, B			

Note: C = Commercial
 I = Industrial
 A = Automotive
 M = Military
 B = MIL-STD-883 Class B

2.7 Speed Grade Offerings

Table 5 • Speed Grade Offerings

	– F	Std	–1	–2	–3
C	P	P	P	P	P
I		P	P	P	P
A		P			
M		P	P		
B		P	P		

Note: See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local *Microsemi Sales representative* for device availability.

Table 23 • DC Specification (5.0 V PCI Signaling)¹

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
C _{IN}	Input Pin Capacitance			10	—	10	pF
C _{CLK}	CLK Pin Capacitance		5	12	—	10	pF
L _{PIN}	Pin Inductance			20	—	< 8 nH ⁴	nH

1. PCI Local Bus Specification, Version 2.1, Section 4.2.1.1.

2. Maximum rating for VCCI –0.5 V to 7.0 V

3. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V.

4. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

Table 24 • AC Specifications (5.0V PCI Signaling)*

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
ICL	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1) / 0.015$		–60	–10	mA
Slew (r)	Output Rise Slew Rate	0.4 V to 2.4 V load	1	5	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	2.4 V to 0.4 V load	1	5	2.8	4.3	V/ns

Note: *PCI Local Bus Specification, Version 2.1, Section 4.2.1.2.

3.9.3 Output Drive Characteristics for 3.3 V PCI Signaling

Table 25 • DC Specification (3.3 V PCI Signaling)¹

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
VCCI	Supply Voltage for I/Os		3.0	3.6	3.0	3.6 ²	V
VIH	Input High Voltage		0.5	VCC + 0.5	0.5	VCCI + 0.3	V
VIL	Input Low Voltage		−0.5	0.8	−0.3	0.8	V
IIH	Input High Leakage Current	VIN = 2.7 V		70		10	μA
IIL	Input Leakage Current			−70		−10	μA
VOH	Output High Voltage	IOUT = −2 mA	0.9		3.3		V
VOL	Output Low Voltage	IOUT = 3 mA, 6 mA		0.1		0.1 VCCI	V
CIN	Input Pin Capacitance			10		10	pF
CLK	CLK Pin Capacitance		5	12		10	pF
L _{PIN}	Pin Inductance			20		< 8 nH ³	nH

1. PCI Local Bus Specification, Version 2.1, Section 4.2.2.1.

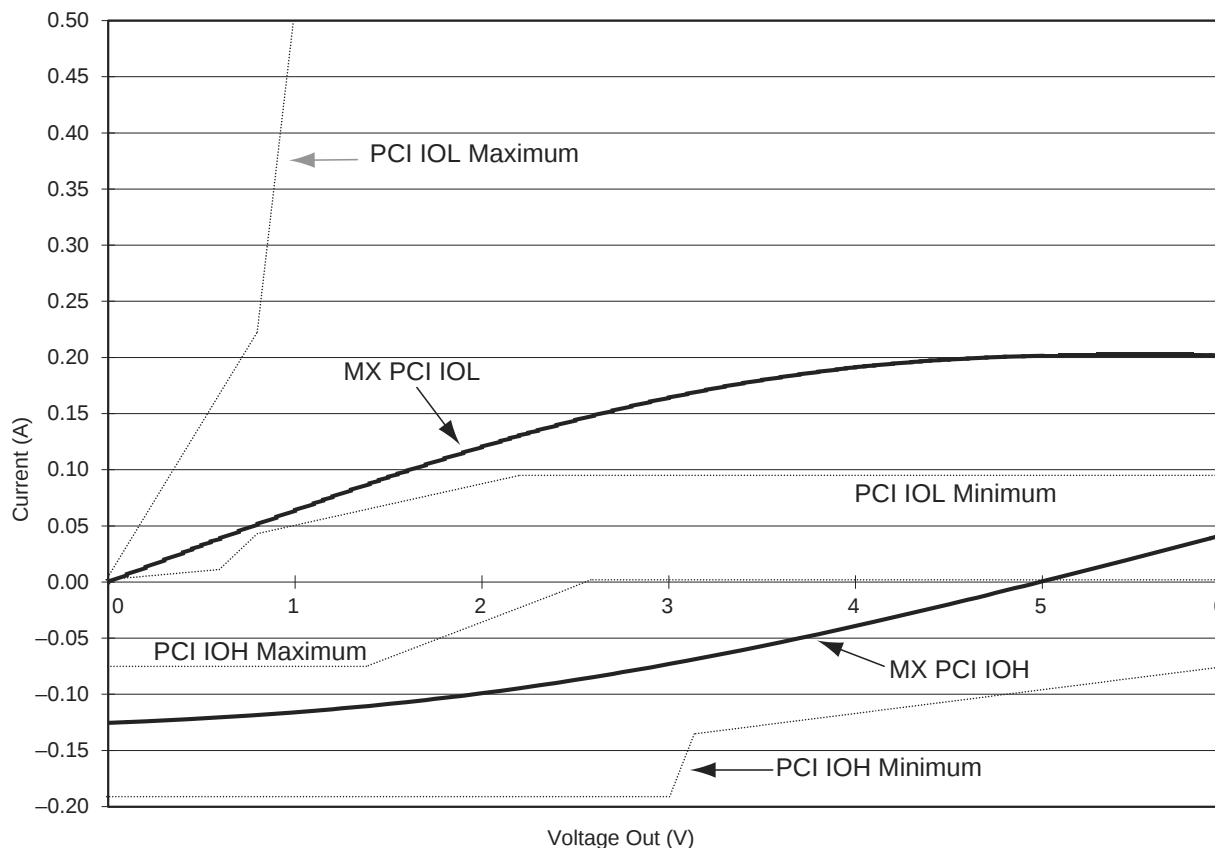
2. Maximum rating for VCCI −0.5 V to 7.0V.

3. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

Table 26 • AC Specifications for (3.3 V PCI Signaling)*

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
ICL	Low Clamp Current	−5 < VIN ≤ −1	−25 + (VIN + 1) / 0.015		−60	−10	mA
Slew (r)	Output Rise Slew Rate	0.2 V to 0.6 V load	1	4	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	0.6 V to 0.2 V load	1	4	2.8	4.0	V/ns

Note: *PCI Local Bus Specification, Version 2.1, Section 4.2.2.2.

Figure 16 • Typical Output Drive Characteristics (Based Upon Measured Data)

3.9.4 Junction Temperature (T_J)

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a(1)$$

EQ 4

where:

- T_a = Ambient Temperature
- ΔT = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$ (2)
- P = Power
- θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in Table 27, page 29.

3.9.5 Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc} , and the junction-to-ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates.

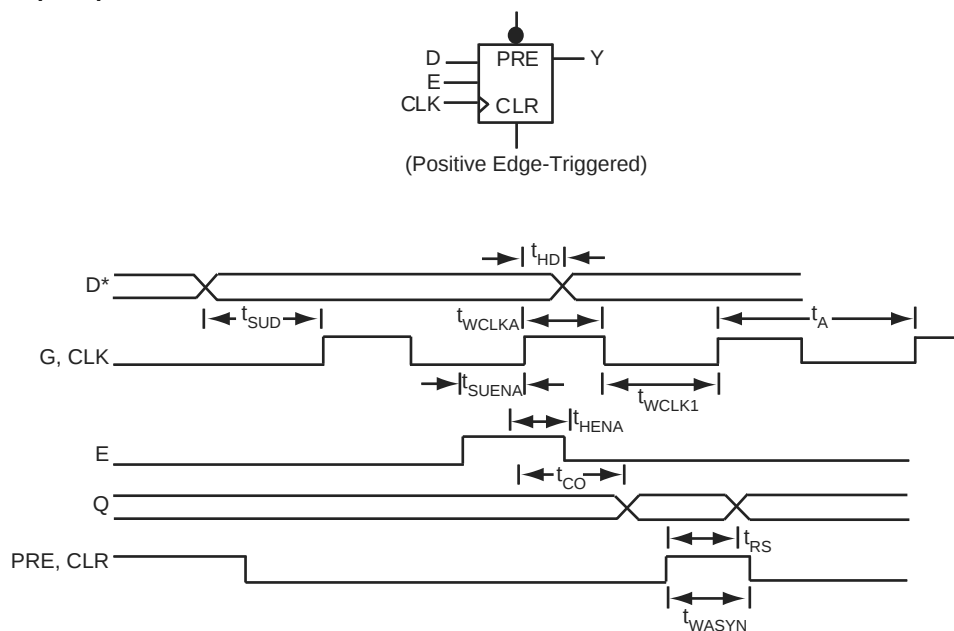
The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of θ_{ja} .

3.10.2 Sequential Module Timing Characteristics

The following figure shows sequential module timing characteristics.

Figure 25 • Flip-Flops and Latches



Note: *D represents all data functions involving A, B, and S for multiplexed flip-flops.

3.10.3 Sequential Timing Characteristics

The following figures show sequential timing characteristics.

Figure 26 • Input Buffer Latches

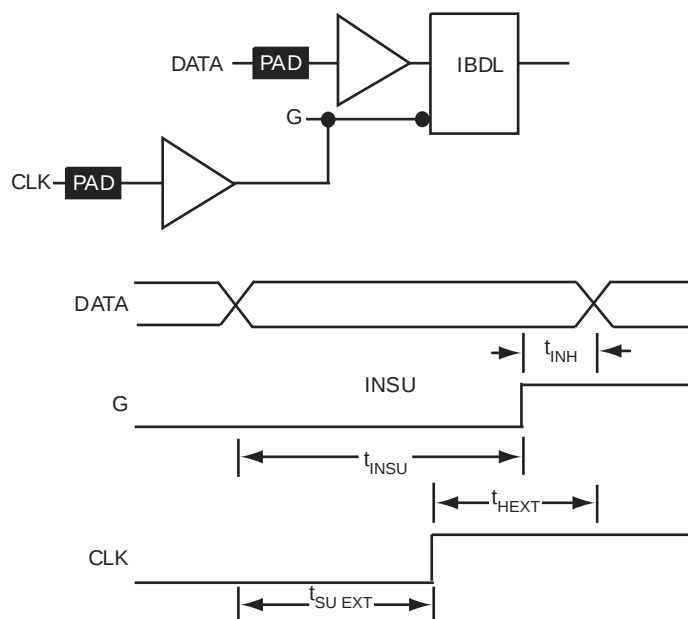
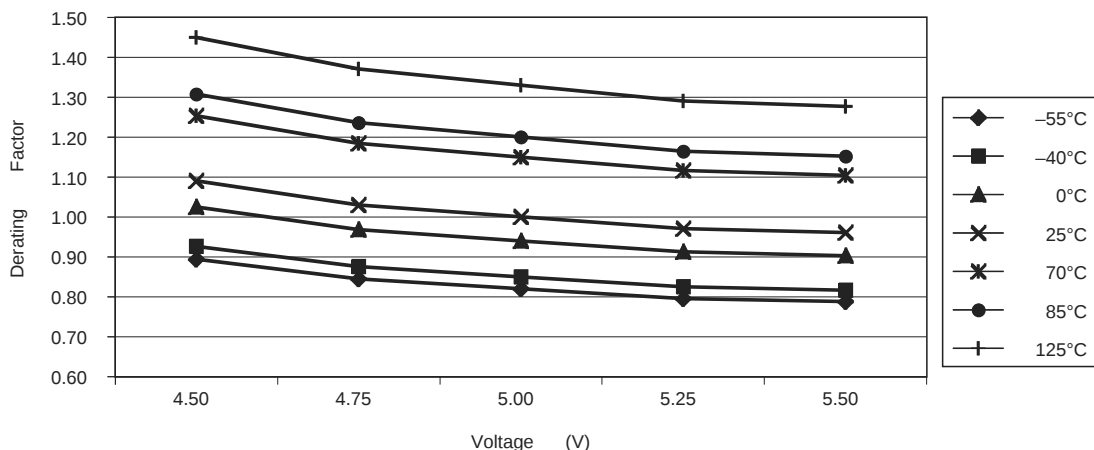
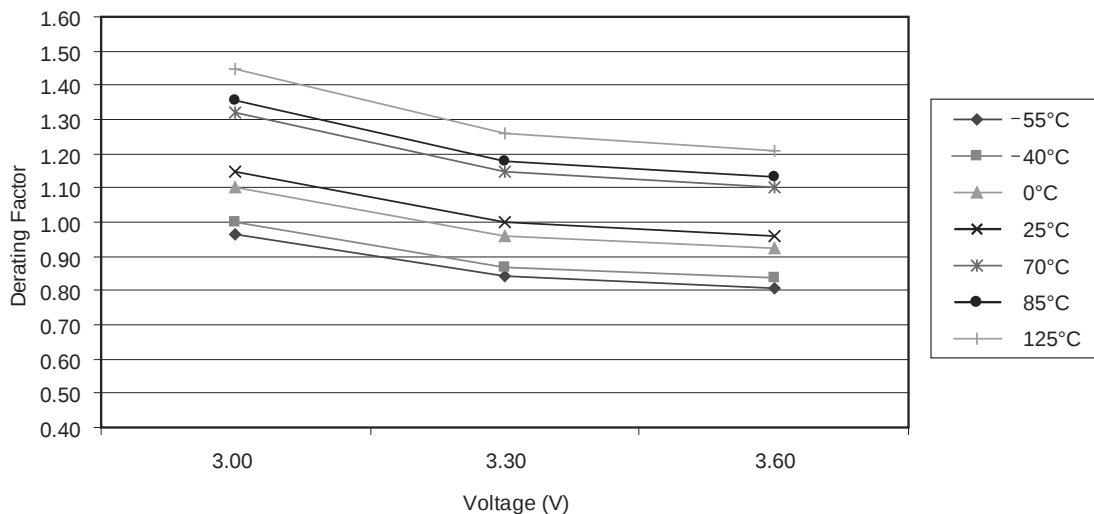


Figure 35 • 40MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Note: This derating factor applies to all routing and propagation delays

Table 30 • 42MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$)

42MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
3.00	0.97	1.00	1.10	1.15	1.32	1.36	1.45
3.30	0.84	0.87	0.96	1.00	1.15	1.18	1.26
3.60	0.81	0.84	0.92	0.96	1.10	1.13	1.21

Figure 36 • 42MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$)

Note: This derating factor applies to all routing and propagation delays

Table 31 • 40MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$)

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
3.00	1.08	1.12	1.21	1.26	1.50	1.64	2.00
3.30	0.86	0.89	0.96	1.00	1.19	1.30	1.59

Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays ¹													
t _{IRD1}	FO = 1 Routing Delay		2.9		3.3		3.8		4.5		6.3		ns
t _{IRD2}	FO = 2 Routing Delay		3.6		4.2		4.8		5.6		7.8		ns
t _{IRD3}	FO = 3 Routing Delay		4.4		5.0		5.7		6.7		9.4		ns
t _{IRD4}	FO = 4 Routing Delay		5.1		5.9		6.7		7.8		11.0		ns
t _{IRD8}	FO = 8 Routing Delay		8.0		9.3		10.5		12.4		17.2		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 16 FO = 128	6.4 6.4		7.4 7.4		8.4 8.4		9.9 9.9		13.8 13.8		ns
t _{CKL}	Input HIGH to LOW	FO = 16 FO = 128	6.8 6.8		7.8 7.8		8.9 8.9		10.4 10.4		14.6 14.6		ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 16 FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t _{PWL}	Minimum Pulse Width LOW	FO = 16 FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t _{CKSW}	Maximum Skew	FO = 16 FO = 128	0.6 0.8		0.6 0.9		0.7 1.0		0.8 1.2		1.2 1.6		ns
t _P	Minimum Period	FO = 16 FO = 128	6.5 6.8		7.5 7.8		8.5 8.9		10.1 10.4		14.1 14.6		ns
f _{MAX}	Maximum Frequency	FO = 16 FO = 128	113 109		105 101		96 92		83 80		50 48		MHz
TTL Output Module Timing ⁴													
t _{DLH}	Data-to-Pad HIGH		4.7		5.4		6.1		7.2		10.0		ns
t _{DHL}	Data-to-Pad LOW		5.6		6.4		7.3		8.6		12.0		ns
t _{ENZH}	Enable Pad Z to HIGH		5.2		6.0		6.9		8.1		11.3		ns
t _{ENZL}	Enable Pad Z to LOW		6.6		7.6		8.6		10.1		14.1		ns
t _{ENHZ}	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9		ns
t _{ENLZ}	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7		ns
d _{TLH}	Delta LOW to HIGH		0.03		0.03		0.04		0.04		0.06		ns/pF
d _{THL}	Delta HIGH to LOW		0.04		0.04		0.05		0.06		0.08		ns/pF

Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH		5.5		6.4		7.2		8.5		11.9	ns
t _{DHL}	Data-to-Pad LOW		4.8		5.5		6.2		7.3		10.2	ns
t _{ENZH}	Enable Pad Z to HIGH		4.7		5.5		6.2		7.3		10.2	ns
t _{ENZL}	Enable Pad Z to LOW		6.8		7.9		8.9		10.5		14.7	ns
t _{ENHZ}	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9	ns
t _{ENLZ}	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7	ns
d _{TLH}	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d _{THL}	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading.

Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays ¹												
t _{PD1}	Single Module		1.2		1.3		1.5		1.8		2.5	ns
t _{CO}	Sequential Clock-to-Q		1.3		1.4		1.6		1.9		2.7	ns
t _{GO}	Latch G-to-Q		1.2		1.4		1.6		1.8		2.6	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.6		1.8		2.1		2.9	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t _{RD2}	FO = 2 Routing Delay		0.9		1.0		1.2		1.4		1.9	ns
t _{RD3}	FO = 3 Routing Delay		1.2		1.3		1.5		1.7		2.4	ns
t _{RD4}	FO = 4 Routing Delay		1.4		1.5		1.7		2.0		2.9	ns
t _{RD8}	FO = 8 Routing Delay		2.3		2.6		2.9		3.4		4.8	ns
Logic Module Sequential Timing ^{3, 4}												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.3		0.4		0.4		0.5		0.7		ns
t _{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.4		0.5		0.5		0.6		0.8		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.4		3.8		4.3		5.0		7.0		ns

Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		2.5		2.7		3.1		3.6		5.1	ns
t _{DHL}	Data-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t _{ENZH}	Enable Pad Z to HIGH		2.6		2.9		3.3		3.9		5.5	ns
t _{ENZL}	Enable Pad Z to LOW		2.9		3.2		3.7		4.3		6.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		4.9		5.4		6.2		7.3		10.2	ns
t _{ENLZ}	Enable Pad LOW to Z		5.3		5.9		6.7		7.9		11.1	ns
t _{GLH}	G-to-Pad HIGH		2.6		2.9		3.3		3.8		5.3	ns
t _{GHL}	G-to-Pad LOW		2.6		2.9		3.3		3.8		5.3	ns
t _{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.2		5.8		6.6		7.7		10.8	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.4		8.2		9.3		10.9		15.3	ns
d _{TLH}	Capacity Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF
d _{THL}	Capacity Loading, HIGH to LOW		0.04		0.04		0.04		0.05		0.07	ns/pF

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		3.4		3.8		4.3		5.1		7.1	ns
t _{DHL}	Data-to-Pad LOW		4.0		4.5		5.1		6.1		8.3	ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t _{ENZL}	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t _{ENHZ}	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t _{ENLZ}	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t _{GLH}	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t _{GHL}	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t _{LSU}	I/O Latch Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad),64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d _{TLH}	Capacity Loading, LOW to HIGH		0.00		0.00		0.00		0.10		0.01	ns/pF
d _{THL}	Capacity Loading, HIGH to LOW		0.09		0.10		0.10		0.10		0.10	ns/pF

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay		1.8		2.0		2.3		2.7		3.8		ns
t _{IRD2}	FO = 2 Routing Delay		2.1		2.3		2.6		3.1		4.3		ns
t _{IRD3}	FO = 3 Routing Delay		2.3		2.5		2.9		3.4		4.8		ns
t _{IRD4}	FO = 4 Routing Delay		2.5		2.8		3.2		3.7		5.2		ns
t _{IRD8}	FO = 8 Routing Delay		3.4		3.8		4.3		5.1		7.1		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32	2.6		2.9		3.3		3.9		5.4		ns
		FO = 486	2.9		3.2		3.6		4.3		5.9		ns
t _{CKL}	Input HIGH to LOW	FO = 32	3.7		4.1		4.6		5.4		7.6		ns
		FO = 486	4.3		4.7		5.4		6.3		8.8		ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	2.2	2.4	2.7		3.2		4.5				ns
		FO = 486	2.4	2.6	3.0		3.5		4.9				ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	2.2	2.4	2.7		3.2		4.5				ns
		FO = 486	2.4	2.6	3.0		3.5		4.9				ns
t _{CKSW}	Maximum Skew	FO = 32	0.5		0.6		0.7		0.8		1.1		ns
		FO = 486	0.5		0.6		0.7		0.8		1.1		ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0	0.0	0.0		0.0		0.0				ns
		FO = 486	0.0	0.0	0.0		0.0		0.0				ns
t _{HEXT}	Input Latch External Hold	FO = 32	2.8	3.1	3.5		4.1		5.7				ns
		FO = 486	3.3	3.7	4.2		4.9		6.9				ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	4.7	5.2	5.7		6.5		10.9				ns
		FO = 486	5.1	5.7	6.2		7.1		11.9				ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		3.5		3.9		4.5		5.2		7.3	ns
t _{DHL}	Data-to-Pad LOW		2.5		2.7		3.1		3.6		5.1	ns
t _{ENZH}	Enable Pad Z to HIGH		2.7		3.0		3.3		3.9		5.5	ns
t _{ENZL}	Enable Pad Z to LOW		2.9		3.3		3.7		4.3		6.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		5.3		5.8		6.6		7.8		10.9	ns
t _{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t _{GLH}	G-to-Pad HIGH		5.0		5.6		6.3		7.5		10.4	ns
t _{GHL}	G-to-Pad LOW		5.0		5.6		6.3		7.5		10.4	ns
t _{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions ¹												
t _{PD}	Internal Array Module Delay		1.9		2.1		2.3		2.7		3.8	ns
t _{PDD}	Internal Decode Module Delay		2.2		2.5		2.8		3.3		4.7	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.7	ns
t _{RD2}	FO = 2 Routing Delay		1.8		2.0		2.3		2.7		3.7	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.5		2.8		3.4		4.7	ns
t _{RD4}	FO = 4 Routing Delay		2.8		3.1		3.5		4.1		5.7	ns

Clock signal to shift the Boundary Scan Test (BST) data into the device. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

TDI, I/O Test Data In

Serial data input for BST instructions and data. Data is shifted in on the rising edge of TCK. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

TDO, I/O Test Data Out

Serial data output for BST instructions and test data. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

TMS, I/O Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI and TDO pins are boundary scan pins. Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications. IEEE JTAG specification recommends a 10k Ω pull-up resistor on the pin. BST pins are only available in A42MX24 and A42MX36 devices.

VCC, Supply Voltage

Input supply voltage for 40MX devices

VCCA, Supply Voltage

Supply voltage for array in 42MX devices

VCCI, Supply Voltage

Supply voltage for I/Os in 42MX devices

WD, I/O Wide Decode Output

When a wide decode module is used in a 42MX device this pin can be used as a dedicated output from the wide decode module. This direct connection eliminates additional interconnect delays associated with regular logic modules. To implement the direct I/O connection, connect an output buffer of any type to the output of the wide decode macro and place this output on one of the reserved WD pins.

Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
47	I/O	I/O	I/O	WD, I/O
48	I/O	I/O	I/O	I/O
49	I/O	GND	GND	GND
50	I/O	I/O	I/O	WD, I/O
51	I/O	I/O	I/O	WD, I/O
52	I/O	SDO, I/O	SDO, I/O	SDO, TDO, I/O
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	GND	I/O	I/O	I/O
61	GND	I/O	I/O	I/O
62	I/O	I/O	I/O	TCK, I/O
63	I/O	LP	LP	LP
64	CLK, I/O	VCCA	VCCA	VCCA
65	I/O	VCCI	VCCI	VCCI
66	MODE	I/O	I/O	I/O
67	VCC	I/O	I/O	I/O
68	VCC	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	GND	GND	GND
71	I/O	I/O	I/O	I/O
72	SDI, I/O	I/O	I/O	I/O
73	DCLK, I/O	I/O	I/O	I/O
74	PRA, I/O	I/O	I/O	I/O
75	PRB, I/O	I/O	I/O	I/O
76	I/O	SDI, I/O	SDI, I/O	SDI, I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	WD, I/O
79	I/O	I/O	I/O	WD, I/O
80	I/O	I/O	I/O	WD, I/O
81	I/O	PRA, I/O	PRA, I/O	PRA, I/O
82	GND	I/O	I/O	I/O
83	I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O

Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
95	I/O	I/O	I/O
96	I/O	I/O	WD, I/O
97	I/O	I/O	I/O
98	VCCA	VCCA	VCCA
99	GND	GND	GND
100	NC	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	NC	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	WD, I/O
107	I/O	I/O	WD, I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	NC	I/O	I/O
111	I/O	I/O	WD, I/O
112	I/O	I/O	WD, I/O
113	I/O	I/O	I/O
114	NC	VCCI	VCCI
115	I/O	I/O	WD, I/O
116	NC	I/O	WD, I/O
117	I/O	I/O	I/O
118	I/O	I/O	TDI, I/O
119	I/O	I/O	TMS, I/O
120	GND	GND	GND
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	NC	I/O	I/O
125	GND	GND	GND
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	NC	I/O	I/O
130	GND	GND	GND
131	I/O	I/O	I/O

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
169	I/O	WD, I/O	WD, I/O
170	I/O	I/O	I/O
171	NC	I/O	QCLKD, I/O
172	I/O	I/O	I/O
173	I/O	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	I/O	WD, I/O	WD, I/O
177	I/O	WD, I/O	WD, I/O
178	PRA, I/O	PRA, I/O	PRA, I/O
179	I/O	I/O	I/O
180	CLKA, I/O	CLKA, I/O	CLKA, I/O
181	NC	I/O	I/O
182	NC	VCCI	VCCI
183	VCCA	VCCA	VCCA
184	GND	GND	GND
185	I/O	I/O	I/O
186	CLKB, I/O	CLKB, I/O	CLKB, I/O
187	I/O	I/O	I/O
188	PRB, I/O	PRB, I/O	PRB, I/O
189	I/O	I/O	I/O
190	I/O	WD, I/O	WD, I/O
191	I/O	WD, I/O	WD, I/O
192	I/O	I/O	I/O
193	NC	I/O	I/O
194	NC	WD, I/O	WD, I/O
195	NC	WD, I/O	WD, I/O
196	I/O	I/O	QCLKC, I/O
197	NC	I/O	I/O
198	I/O	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	NC	I/O	I/O
202	VCCI	VCCI	VCCI
203	I/O	WD, I/O	WD, I/O
204	I/O	WD, I/O	WD, I/O
205	I/O	I/O	I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
148	I/O
149	I/O
150	GND
151	I/O
152	I/O
153	I/O
154	I/O
155	I/O
156	I/O
157	GND
158	I/O
159	SDI, I/O
160	I/O
161	WD, I/O
162	WD, I/O
163	I/O
164	VCCI
165	I/O
166	I/O
167	I/O
168	WD, I/O
169	WD, I/O
170	I/O
171	QCLKD, I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	WD, I/O
177	WD, I/O
178	PRA, I/O
179	I/O
180	CLKA, I/O
181	I/O
182	VCCI
183	VCCA
184	GND

Figure 50 • CQ256

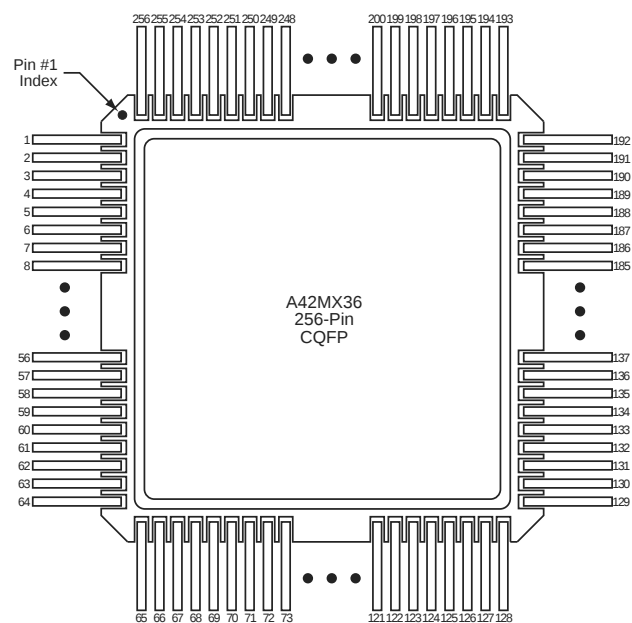


Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
1	NC
2	GND
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	GND
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O

Table 62 • CQ172

99	I/O
100	I/O
101	I/O
102	I/O
103	GND
104	I/O
105	I/O
106	VKS
107	VPP
108	GND
109	VCCI
110	VSV
111	I/O
112	I/O
113	VCC
114	I/O
115	I/O
116	I/O
117	I/O
118	GND
119	I/O
120	I/O
121	I/O
122	I/O
123	GNDI
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	SDI
132	I/O
133	I/O
134	I/O
135	I/O
136	VCCI
137	I/O