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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	2560
Number of I/O	176
Number of Gates	54000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx36-1pq208

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- Table 15, page 21 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 22, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 23, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

1.2 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Added CQFP package information for A42MX16 device in Product Profile, page 1 and Ceramic Device Resources, page 4 (SAR 79522).
- Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in Temperature Grade Offerings, page 5 (SAR 79519)
- Changed Silicon Sculptor II to Silicon Sculptor in Programming, page 12 (SAR 38754)
- Added Figure 53, page 158 CQ172 package (SAR 79522).

1.3 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Added Figure 42, page 97 PQ144 Package for A42MX09 device (SAR 69776)
- Added Figure 52, page 153 PQ132 Package for A42MX09 device (SAR 69776)

1.4 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Added information on power-up behavior for A42MX24 and A42MX36 devices to the Power Supply, page 13 (SAR 42096
- Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793)

1.5 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- The FuseLock logo and accompanying text was removed from the User Security, page 12. This marking is no longer used on Microsemi devices (PCN 0915)
- The Development Tool Support, page 19 was updated (SAR 38512)

1.6 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- Ordering Information, page 3 was updated to include lead-free package ordering codes (SAR 21968)
- The User Security, page 12 was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673)

2.4 Plastic Device Resources

Table 2 • **Plastic Device Resources**

	User I/Os											
Device	**PLCC 44-Pin**	**PLCC 68-Pin**	**PLCC 84-Pin**	**PQFP 100-Pin**	**PQFP 144-Pin**	**PQFP 160-Pin**	**PQFP 208-Pin**	**PQFP 240-Pin**	**VQFP 80-Pin**	**VQFP 100-Pin**	**TQFP 176-Pin**	**PBGA 272-Pin**
A40MX02	34	57	–	57	–	–	–	–	57	–	–	–
A40MX04	34	57	69	69	–	–	–	–	69	–	–	–
A42MX09	–	–	72	83	95	101	–	–	–	83	104	–
A42MX16	–	–	72	83	–	125	140	–	–	83	140	–
A42MX24	–	–	72	–	–	125	176	–	–	–	150	–
A42MX36	–	–	–	–	–	–	176	202	–	–	–	202

Note: Package Definitions: PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array

2.5 Ceramic Device Resources

Table 3 • **Ceramic Device Resources**

	User I/Os			
Device	**CPGA 132-Pin**	**CQFP 172-Pin**	**CQFP 208-Pin**	**CQFP 256-Pin**
A42MX09	95			
A42MX16		131		
A42MX36			176	202

Note: Package Definitions: CQFP = Ceramic Quad Flat Pack

3 40MX and 42MX FPGAs

3.1 General Description

Microsemi's 40MX and 42MX families offer a cost-effective design solution at 5V. The MX devices are single-chip solutions and provide high performance while shortening the system design and development cycle. MX devices can integrate and consolidate logic implemented in multiple PALs, CPLDs, and FPGAs. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

The MX device architecture is based on Microsemi's patented antifuse technology implemented in a 0.45µm triple-metal CMOS process. With capacities ranging from 3,000 to 54,000 system gates, the MX devices provide performance up to 250 MHz, are live on power-up and have one-fifth the standby power consumption of comparable FPGAs. MX FPGAs provide up to 202 user I/Os and are available in a wide variety of packages and speed grades.

A42MX24 and A42MX36 devices also feature multiPlex I/Os, which support mixed-voltage systems, enable programmable PCI, deliver high-performance operation at both 5.0V and 3.3V, and provide a low-power mode. The devices are fully compliant with the PCI local bus specification (version 2.1). They deliver 200 MHz on-chip operation and 6.1 ns clock-to-output performance.

The 42MX24 and 42MX36 devices include system-level features such as IEEE Standard 1149.1 (JTAG) Boundary Scan Testing and fast wide-decode modules. In addition, the A42MX36 device offers dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The storage elements can efficiently address applications requiring wide data path manipulation and can perform transformation functions such as those required for telecommunications, networking, and DSP.

All MX devices are fully tested over automotive and military temperature ranges. In addition, the largest member of the family, the A42MX36, is available in both CQ208 and CQ256 ceramic packages screened to MIL-STD-883 levels. For easy prototyping and conversion from plastic to ceramic, the CQ208 and PQ208 devices are pin-compatible.

3.2 MX Architectural Overview

The MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within these families are composed of logic modules, I/O modules, routing resources and clock networks, which are the building blocks for fast logic designs. In addition, the A42MX36 device contains embedded dual-port SRAM modules, which are optimized for high-speed data path functions such as FIFOs, LIFOs and scratch pad memory. A42MX24 and A42MX36 also contain wide-decode modules.

3.2.1 Logic Modules

The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources.(see the following figure).

The logic module can implement the four basic logic functions (NAND, AND, OR and NOR) in gates of two, three, or four inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array; latches and flip-flops can be constructed from logic modules whenever required in the application.

Figure 8 • **Clock Networks of 42MX Devices**

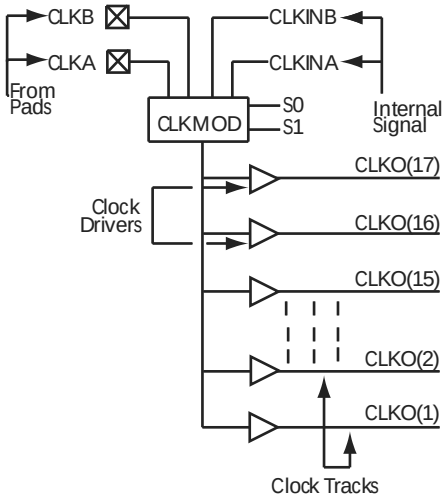
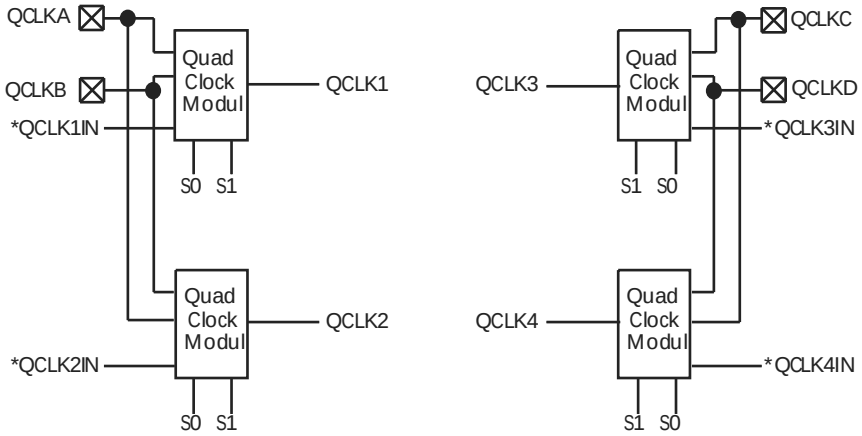


Figure 9 • **Quadrant Clock Network of A42MX36 Devices**



Note: *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

3.2.5 MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 10, page 12 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (See the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 10, page 12). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. See the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 µA.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 11, page 12). When the PCI fuse is not programmed, the output drive is standard.

reliability. Devices should not be operated outside the recommended operating conditions.

Table 21 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCCA	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI	3.14 to 3.47	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

A sample calculation of the absolute maximum power dissipation allowed for a TQ176 package at commercial temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (°\text{C})}{\theta_{ja}(°(\text{C}/\text{W}))} = \frac{150°\text{C} - 70°\text{C}}{(28°\text{C})/\text{W}} = 2.86\text{W}$$

EQ 5

The maximum power dissipation for military-grade devices is a function of θ_{jc}. A sample calculation of the absolute maximum power dissipation allowed for CQFP 208-pin package at military temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (°\text{C})}{\theta_{jc}(°(\text{C}/\text{W}))} = \frac{150°\text{C} - 125°\text{C}}{(6.3°\text{C})/\text{W}} = 3.97\text{W}$$

EQ 6

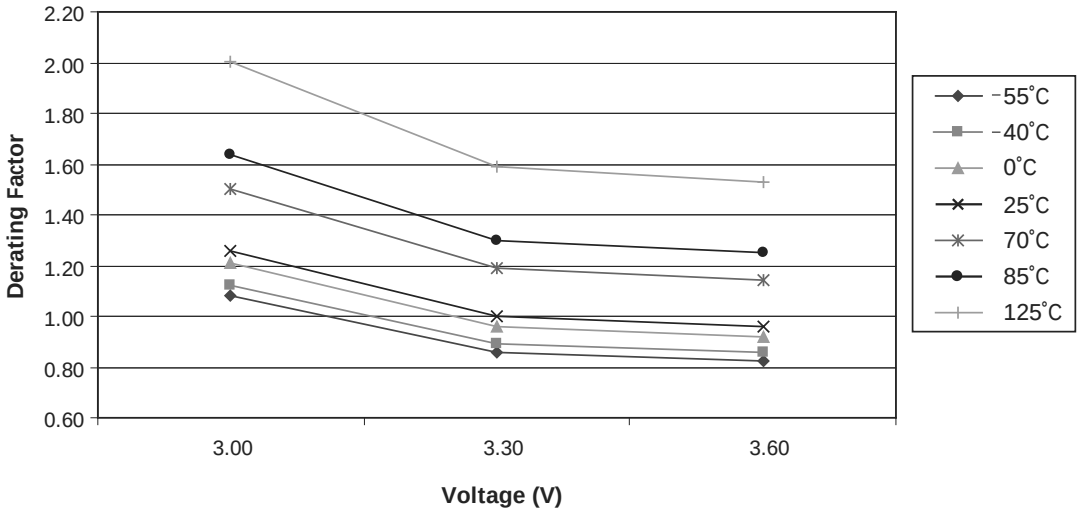
Table 27 • **Package Thermal Characteristics**

			θ_{ja}			
Plastic Packages	**Pin Count**	θ_{jc}	**Still Air**	**1.0 m/s 200 ft/min.**	**2.5 m/s 500 ft/min.**	**Units**
Plastic Quad Flat Pack	100	12.0	27.8	23.4	21.2	°C/W
Plastic Quad Flat Pack	144	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	160	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	208	8.0	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack	240	8.5	25.6	22.3	20.8	°C/W
Plastic Leaded Chip Carrier	44	16.0	20.0	24.5	22.0	°C/W
Plastic Leaded Chip Carrier	68	13.0	25.0	21.0	19.4	°C/W
Plastic Leaded Chip Carrier	84	12.0	22.5	18.9	17.6	°C/W
Thin Plastic Quad Flat Pack	176	11.0	24.7	19.9	18.0	°C/W
Very Thin Plastic Quad Flat Pack	80	12.0	38.2	31.9	29.4	°C/W
Very Thin Plastic Quad Flat Pack	100	10.0	35.3	29.4	27.1	°C/W
Plastic Ball Grid Array	272	3.0	18.3	14.9	13.9	°C/W
Ceramic Packages						
Ceramic Pin Grid Array	132	4.8	25.0	20.6	18.7	°C/W
Ceramic Quad Flat Pack	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack	256	2.0	20.0	16.5	15.0	°C/W

Table 31 • **40MX Temperature and Voltage Derating Factors (Normalized to TJ = 25°C, VCC = 3.3 V)**

	Temperature						
40MX Voltage	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
3.60	0.83	0.85	0.92	0.96	1.14	1.25	1.53

Figure 37 • **40MX Junction Temperature and Voltage Derating Curves (Normalized to TJ = 25°C, VCC = 3.3 V)**



Note: This derating factor applies to all routing and propagation delays

3.11.5 PCI System Timing Specification

The following tables list the critical PCI timing parameters and the corresponding timing parameters for the MX PCI-compliant devices.

3.11.6 PCI Models

Microsemi provides synthesizable VHDL and Verilog-HDL models for a PCI Target interface, a PCI Target and Target+DMA Master interface. Contact the Microsemi sales representative for more details.

Table 32 • **Clock Specification for 33 MHz PCI**

		PCI		A42MX24		A42MX36		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{CYC}	CLK Cycle Time	30	–	4.0	–	4.0	–	ns
t_{HIGH}	CLK High Time	11	–	1.9	–	1.9	–	ns
t_{LOW}	CLK Low Time	11	–	1.9	–	1.9	–	ns

Table 33 • **Timing Parameters for 33 MHz PCI**

		PCI		A42MX24		A42MX36		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{VAL}	CLK to Signal Valid—Bused Signals	2	11	2.0	9.0	2.0	9.0	ns
$t_{VAL(PTP)}$	CLK to Signal Valid—Point-to-Point	2 [2]	12	2.0	9.0	2.0	9.0	ns
t_{ON}	Float to Active	2	–	2.0	4.0	2.0	4.0	ns
t_{OFF}	Active to Float	–	28	–	8.3[1]	–	8.3[1]	ns
t_{SU}	Input Set-Up Time to CLK—Bused Signals	7	–	1.5	–	1.5	–	ns

Table 35 • **A40MX02 Timing Characteristics (Nominal 3.3 V Operation) *(continued)***
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[4]												
t_{DLH}	Data-to-Pad HIGH		5.5		6.4		7.2		8.5		11.9	ns
t_{DHL}	Data-to-Pad LOW		4.8		5.5		6.2		7.3		10.2	ns
t_{ENZH}	Enable Pad Z to HIGH		4.7		5.5		6.2		7.3		10.2	ns
t_{ENZL}	Enable Pad Z to LOW		6.8		7.9		8.9		10.5		14.7	ns
t_{ENHZ}	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9	ns
t_{ENLZ}	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7	ns
d_{TLH}	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro
4. Delays based on 35 pF loading

Table 36 • **A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t_{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t_{PD2}	Dual-Module Macros		2.3		3.1		3.5		4.1		5.7	ns
t_{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays[1]												
t_{RD1}	FO = 1 Routing Delay		1.2		1.6		1.8		2.1		3.0	ns
t_{RD2}	FO = 2 Routing Delay		1.9		2.2		2.5		2.9		4.1	ns
t_{RD3}	FO = 3 Routing Delay		2.4		2.8		3.2		3.7		5.2	ns
t_{RD4}	FO = 4 Routing Delay		2.9		3.4		3.9		4.5		6.3	ns
t_{RD8}	FO = 8 Routing Delay		5.0		5.8		6.6		7.8		10.9	ns
Logic Module Sequential Timing[2]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	3.1		3.5		4.0		4.7		6.6		ns

Table 41 • **A42MX16 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Sequential Timing[3, 4]													
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up		0.5		0.5		0.6		0.7		0.9		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up		1.0		1.1		1.2		1.4		2.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		4.8		5.3		6.0		7.1		9.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		6.2		6.9		7.9		9.2		12.9		ns
t_A	Flip-Flop Clock Input Period		9.5		10.6		12.0		14.1		19.8		ns
t_{INH}	Input Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Set-Up		0.7		0.8		0.9		1.01		1.4		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up		0.7		0.8		0.89		1.01		1.4		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency			129		117		108		94		56	MHz
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			1.5		1.6		1.9		2.2		3.1	ns
t_{INYL}	Pad-to-Y LOW			1.1		1.3		1.4		1.7		2.4	ns
t_{INGH}	G to Y HIGH			2.0		2.2		2.5		2.9		4.1	ns
t_{INGL}	G to Y LOW			2.0		2.2		2.5		2.9		4.1	ns
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			2.6		2.9		3.2		3.8		5.3	ns
t_{IRD2}	FO = 2 Routing Delay			2.9		3.2		3.7		4.3		6.1	ns
t_{IRD3}	FO = 3 Routing Delay			3.3		3.6		4.1		4.9		6.8	ns
t_{IRD4}	FO = 4 Routing Delay			3.6		4.0		4.6		5.4		7.6	ns
t_{IRD8}	FO = 8 Routing Delay			5.1		5.6		6.4		7.5		10.5	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		4.4		4.8		5.5		6.5		9.0	ns
		FO = 384		4.8		5.3		6.0		7.1		9.9	ns
t_{CKL}	Input HIGH to LOW	FO = 32		5.3		5.9		6.7		7.8		11.0	ns
		FO = 384		6.2		6.9		7.9		9.2		12.9	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	5.7		6.3		7.1		8.4		11.8		ns
		FO = 384	6.6		7.4		8.3		9.8		13.7		ns

Table 41 • **A42MX16 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO}	Array Clock-to-Out (Pad-to-Pad),64 Clock Loading		11.3		12.5		14.2		16.7		23.3	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

1. For dual-module macros use tPD1 + tRD1 + taped, to + tRD1 + taped, or tPD1 + tRD1 + tusk, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing ansalysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 42 • **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions[1]												
t_{PD}	Internal Array Module Delay		1.2		1.3		1.5		1.8		2.5	ns
t_{PDD}	Internal Decode Module Delay		1.4		1.6		1.8		2.1		3.0	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.8		0.9		1.0		1.2		1.7	ns
t_{RD2}	FO = 2 Routing Delay		1.0		1.2		1.3		1.5		2.1	ns
t_{RD3}	FO = 3 Routing Delay		1.3		1.4		1.6		1.9		2.6	ns
t_{RD4}	FO = 4 Routing Delay		1.5		1.7		1.9		2.2		3.1	ns
t_{RD5}	FO = 8 Routing Delay		2.4		2.7		3.0		3.6		5.0	ns
Logic Module Sequential Timing[3, 4]												
t_{CO}	Flip-Flop Clock-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch Gate-to-Output		1.2		1.3		1.5		1.8		2.5	ns
t_{SUD}	Flip-Flop (Latch) Set-Up Time	0.3		0.4		0.4		0.5		0.7		ns
t_{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		1.4		1.6		1.8		2.1		2.9	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.4		0.5		0.5		0.6		0.8		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.3		6.5		9.0		ns

Table 42 • **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		3.1		3.5		3.9		4.6		6.4	ns
t_{DHL}	Data-to-Pad LOW		2.4		2.6		3.0		3.5		4.9	ns
t_{ENZH}	Enable Pad Z to HIGH		2.5		2.8		3.2		3.8		5.3	ns
t_{ENZL}	Enable Pad Z to LOW		2.8		3.1		3.5		4.2		5.8	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.2		5.7		6.5		7.6		10.7	ns
t_{ENLZ}	Enable Pad LOW to Z		4.8		5.3		6.0		7.1		9.9	ns
t_{GLH}	G-to-Pad HIGH		4.9		5.4		6.2		7.2		10.1	ns
t_{GHL}	G-to-Pad LOW		4.9		5.4		6.2		7.2		10.1	ns
t_{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.5		6.1		6.9		8.1		11.3	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.6		11.8		13.4		15.7		22.0	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. D*ata applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

Table 43 • **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Combinatorial Functions[1]												
t_{PD}	Internal Array Module Delay		2.0		1.8		2.1		2.5		3.4	ns
t_{PDD}	Internal Decode Module Delay		1.1		2.2		2.5		3.0		4.2	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		1.7		1.3		1.4		1.7		2.3	ns
t_{RD2}	FO = 2 Routing Delay		2.0		1.6		1.8		2.1		3.0	ns
t_{RD3}	FO = 3 Routing Delay		1.1		2.0		2.2		2.6		3.7	ns
t_{RD4}	FO = 4 Routing Delay		1.5		2.3		2.6		3.1		4.3	ns
t_{RD5}	FO = 8 Routing Delay		1.8		3.7		4.2		5.0		7.0	ns

Table 45 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			2.8		3.1		3.5		4.1		5.7	ns
t_{IRD2}	FO = 2 Routing Delay			3.2		3.5		4.1		4.8		6.7	ns
t_{IRD3}	FO = 3 Routing Delay			3.7		4.1		4.7		5.5		7.7	ns
t_{IRD4}	FO = 4 Routing Delay			4.2		4.6		5.3		6.2		8.7	ns
t_{IRD8}	FO = 8 Routing Delay			6.1		6.8		7.7		9.0		12.6	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		4.6		5.1		5.7		6.7		9.3	ns
		FO = 635		5.0		5.6		6.3		7.4		10.3	ns
t_{CKL}	Input HIGH to LOW	FO = 32		5.3		5.9		6.7		7.8		11.0	ns
		FO = 635		6.8		7.6		8.6		10.1		14.1	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	2.5		2.7		3.1		3.6		5.1		ns
		FO = 635	2.8		3.1		3.5		4.1		5.7		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	2.5		2.7		3.1		3.6		5.1		ns
		FO = 635	2.8		3.1		3.5		4.1		5.7		ns
t_{CKSW}	Maximum Skew	FO = 32		1.0		1.2		1.3		1.5		2.2	ns
		FO = 635		1.0		1.2		1.3		1.5		2.2	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 635	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	4.0		4.4		5.0		5.9		8.2		ns
		FO = 635	4.6		5.2		5.9		6.9		9.6		ns
t_P	Minimum Period ($1/f_{MAX}$)	FO = 32	9.2		10.2		11.1		12.7		21.2		ns
		FO = 635	9.9		11.0		12.0		13.8		23.0		ns
f_{MAX}	Maximum Datapath Frequency	FO = 32		108		98		90		79		47	MHz
		FO = 635		100		91		83		73		44	MHz
TTL Output Module Timing[5]													
t_{DLH}	Data-to-Pad HIGH			3.6		4.0		4.5		5.3		7.4	ns
t_{DHL}	Data-to-Pad LOW			4.2		4.6		5.2		6.2		8.6	ns
t_{ENZH}	Enable Pad Z to HIGH			3.7		4.2		4.7		5.5		7.7	ns
t_{ENZL}	Enable Pad Z to LOW			4.1		4.6		5.2		6.1		8.5	ns
t_{ENHZ}	Enable Pad HIGH to Z			7.34		8.2		9.3		10.9		15.3	ns
TTL Output Module Timing[5]													
t_{ENLZ}	Enable Pad LOW to Z			6.9		7.6		8.7		10.2		14.3	ns
t_{GLH}	G-to-Pad HIGH			4.9		5.5		6.2		7.3		10.2	ns
t_{GHL}	G-to-Pad LOW			4.9		5.5		6.2		7.3		10.2	ns
t_{LSU}	I/O Latch Output Set-Up		0.7		0.7		0.8		1.0		1.4		ns
t_{LH}	I/O Latch Output Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.9		8.8		10.0		11.8		16.5	ns

Table 50 • **PQ 100**

PQ100				
Pin Number	**A40MX02 Function**	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**
93	VCC	VCC	I/O	I/O
94	VCC	VCC	PRB, I/O	PRB, I/O
95	NC	I/O	I/O	I/O
96	NC	I/O	GND	GND
97	NC	I/O	I/O	I/O
98	SDI, I/O	SDI, I/O	I/O	I/O
99	DCLK, I/O	DCLK, I/O	I/O	I/O
100	PRA, I/O	PRA, I/O	I/O	I/O

Figure 42 • **PQ144**

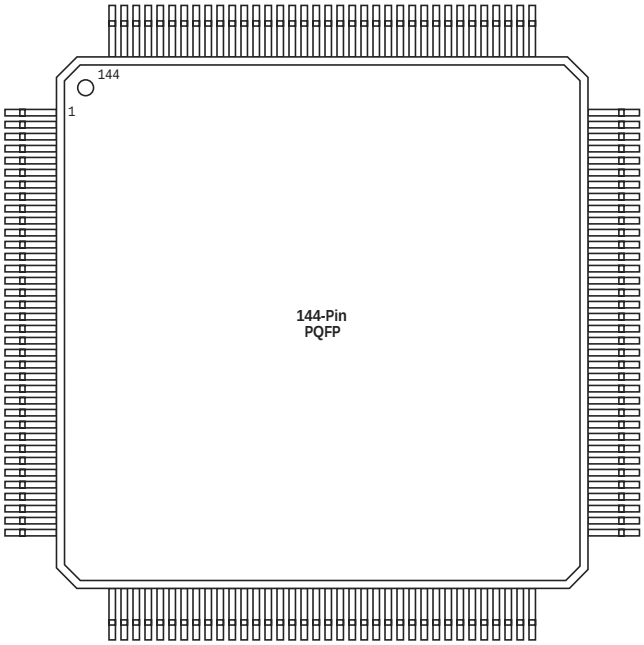


Table 51 • **PQ144**

PQ144	
Pin Number	**A42MX09 Function**
1	I/O
2	MODE
3	I/O
4	I/O
5	I/O

Table 53 • **PQ208**

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
95	NC	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	VCCI	VCCI	VCCI
99	I/O	I/O	I/O
100	I/O	WD, I/O	WD, I/O
101	I/O	WD, I/O	WD, I/O
102	I/O	I/O	I/O
103	SDO, I/O	SDO, TDO, I/O	SDO, TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	VCCA	VCCA
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	NC	I/O	I/O
113	NC	I/O	I/O
114	NC	I/O	I/O
115	NC	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	I/O	I/O	I/O
126	GND	GND	GND
127	I/O	I/O	I/O
128	I/O	TCK, I/O	TCK, I/O
129	LP	LP	LP
130	VCCA	VCCA	VCCA
131	GND	GND	GND

Table 54 • **PQ240**

PQ240	
Pin Number	**A42MX36 Function**
200	I/O
201	I/O
202	I/O
203	I/O
204	I/O
205	I/O
206	VCCA
207	I/O
208	I/O
209	VCCA
210	VCCI
211	I/O
212	I/O
213	I/O
214	I/O
215	I/O
216	I/O
217	I/O
218	I/O
219	VCCA
220	I/O
221	I/O
222	I/O
223	I/O
224	I/O
225	I/O
226	I/O
227	VCCI
228	I/O
229	I/O
230	I/O
231	I/O
232	I/O
233	I/O
234	I/O
235	I/O
236	I/O

Table 58 • **CQ208**

CQ208	
Pin Number	**A42MX36 Function**
148	I/O
149	I/O
150	GND
151	I/O
152	I/O
153	I/O
154	I/O
155	I/O
156	I/O
157	GND
158	I/O
159	SDI, I/O
160	I/O
161	WD, I/O
162	WD, I/O
163	I/O
164	VCCI
165	I/O
166	I/O
167	I/O
168	WD, I/O
169	WD, I/O
170	I/O
171	QCLKD, I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	WD, I/O
177	WD, I/O
178	PRA, I/O
179	I/O
180	CLKA, I/O
181	I/O
182	VCCI
183	VCCA
184	GND

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
207	I/O
208	I/O
209	QCLKC, I/O
210	I/O
211	WD, I/O
212	WD, I/O
213	I/O
214	I/O
215	WD, I/O
216	WD, I/O
217	I/O
218	PRB, I/O
219	I/O
220	CLKB, I/O
221	I/O
222	GND
223	GND
224	VCCA
225	VCCI
226	I/O
227	CLKA, I/O
228	I/O
229	PRA, I/O
230	I/O
231	I/O
232	WD, I/O
233	WD, I/O
234	I/O
235	I/O
236	I/O
237	I/O
238	I/O
239	I/O
240	QCLKD, I/O
241	I/O
242	WD, I/O
243	GND

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
Y13	I/O
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	WD, I/O
Y19	GND
Y20	GND

Figure 52 • **PG132**

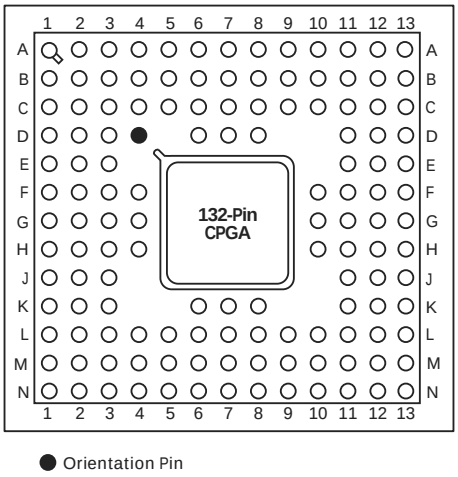


Table 61 • **PG132**

PG132	
Pin Number	**A42MX09 Function**
–	PMPOUT
B2	I/O
A1	MODE
B1	I/O
D3	I/O
C2	I/O
C1	I/O
D2	I/O
D1	I/O
E2	I/O
E1	I/O
F3	I/O

Table 61 • **PG132**

PG132	
Pin Number	**A42MX09 Function**
N10	I/O
M10	I/O
N11	I/O
L10	I/O
M11	I/O
N12	SDO
M12	I/O
L11	I/O
N13	I/O
M13	I/O
K11	I/O
L12	I/O
L13	I/O
K13	I/O
H10	I/O
J12	I/O
J13	I/O
H11	I/O
H12	I/O
H13	VKS
G13	VPP