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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	2560
Number of I/O	176
Number of Gates	54000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx36-1pqg208m

2.4 Plastic Device Resources

Table 2 • **Plastic Device Resources**

	User I/Os											
Device	**PLCC 44-Pin**	**PLCC 68-Pin**	**PLCC 84-Pin**	**PQFP 100-Pin**	**PQFP 144-Pin**	**PQFP 160-Pin**	**PQFP 208-Pin**	**PQFP 240-Pin**	**VQFP 80-Pin**	**VQFP 100-Pin**	**TQFP 176-Pin**	**PBGA 272-Pin**
A40MX02	34	57	–	57	–	–	–	–	57	–	–	–
A40MX04	34	57	69	69	–	–	–	–	69	–	–	–
A42MX09	–	–	72	83	95	101	–	–	–	83	104	–
A42MX16	–	–	72	83	–	125	140	–	–	83	140	–
A42MX24	–	–	72	–	–	125	176	–	–	–	150	–
A42MX36	–	–	–	–	–	–	176	202	–	–	–	202

Note: Package Definitions: PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array

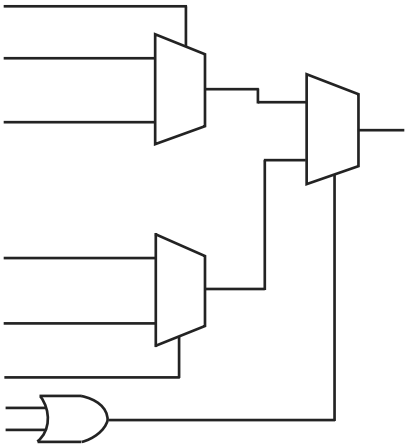
2.5 Ceramic Device Resources

Table 3 • **Ceramic Device Resources**

	User I/Os			
Device	**CPGA 132-Pin**	**CQFP 172-Pin**	**CQFP 208-Pin**	**CQFP 256-Pin**
A42MX09	95			
A42MX16		131		
A42MX36			176	202

Note: Package Definitions: CQFP = Ceramic Quad Flat Pack

Figure 2 • **42MX C-Module Implementation**



The 42MX devices contain three types of logic modules: combinatorial (C-modules), sequential (S-modules) and decode (D-modules). The following figure illustrates the combinatorial logic module. The S-module, shown in Figure 4, page 8, implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D-flip-flop or a transparent latch. The S-module register can be bypassed so that it implements purely combinatorial logic.

Figure 3 • **42MX C-Module Implementation**

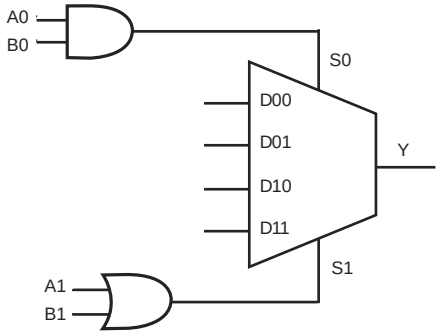


Figure 8 • **Clock Networks of 42MX Devices**

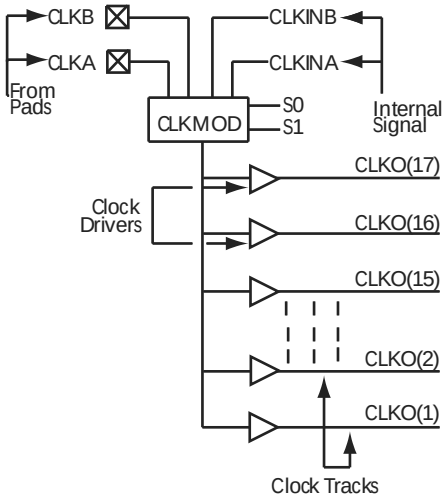
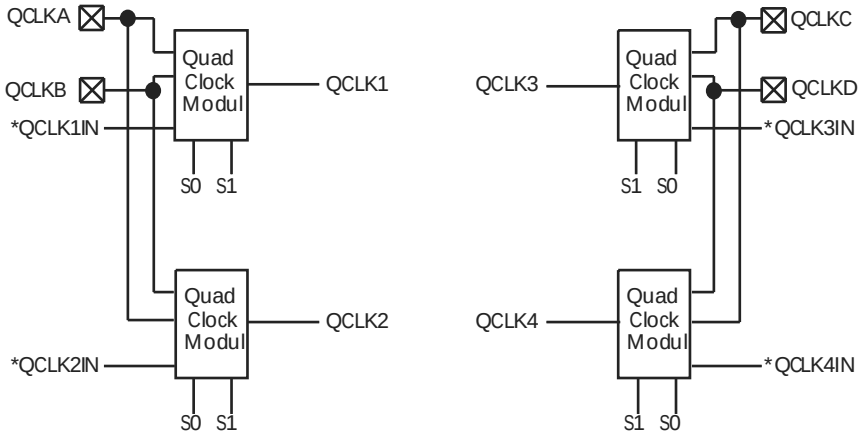


Figure 9 • **Quadrant Clock Network of A42MX36 Devices**



Note: *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

3.2.5 MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 10, page 12 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (See the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 10, page 12). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. See the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 µA.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 11, page 12). When the PCI fuse is not programmed, the output drive is standard.

3.3.7 Low Power Mode

42MX devices have been designed with a Low Power Mode. This feature, activated with setting the special LP pin to HIGH for a period longer than 800 ns, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when exiting Low Power Mode. I/Os can be driven during LP mode, and clock pins should be driven HIGH or LOW and should not float to avoid drawing current. To exit LP mode, the LP pin must be pulled LOW for over 200 µs to allow for charge pumps to power up, and device initialization will begin.

3.4 Power Dissipation

The general power consumption of MX devices is made up of static and dynamic power and can be expressed with the following equation.

3.4.1 General Power Equation

$$P = [ICCstandby + ICCactive]*VCCI + IOL*VOL*N + IOH*(VCCI - VOH)*M$$

EQ 1

where:

- ICCstandby is the current flowing when no inputs or outputs are changing.
- ICCactive is the current flowing due to CMOS switching.
- IOL, IOH are TTL sink/source currents.
- VOL, VOH are TTL level output voltages.
- N equals the number of outputs driving TTL loads to VOL.
- M equals the number of outputs driving TTL loads to VOH.

Accurate values for N and M are difficult to determine because they depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

3.4.2 Static Power Component

The static power due to standby current is typically a small component of the overall power consumption. Standby power is calculated for commercial, worst-case conditions. The static power dissipation by TTL loads depends on the number of outputs driving, and on the DC load current. For instance, a 32-bit bus sinking 4mA at 0.33V will generate 42mW with all outputs driving LOW, and 140mW with all outputs driving HIGH. The actual dissipation will average somewhere in between, as I/Os switch states with time.

3.4.3 Active Power Component

Power dissipation in CMOS devices is usually dominated by the dynamic power dissipation. Dynamic power consumption is frequency-dependent and is a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitances due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

The power dissipated by a CMOS circuit can be expressed by the equation:

$$Power(\mu W) = C_{EQ} * VCCA2 * F(1)$$

EQ 2

where:

- C_{EQ} = Equivalent capacitance expressed in picofarads (pF)

Table 34 • **A40MX02 Timing Characteristics (Nominal 5.0 V Operation) *(continued)***
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			0.7		0.8		0.9		1.1		1.5	ns
t_{INYL}	Pad-to-Y LOW			0.6		0.7		0.8		1.0		1.3	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO = 1 Routing Delay			2.1		2.4		2.2		3.2		4.5	ns
t_{IRD2}	FO = 2 Routing Delay			2.6		3.0		3.4		4.0		5.6	ns
t_{IRD3}	FO = 3 Routing Delay			3.1		3.6		4.1		4.8		6.7	ns
t_{IRD4}	FO = 4 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t_{IRD8}	FO = 8 Routing Delay			5.7		6.6		7.5		8.8		12.4	ns
Global Clock Network													
t_{CKH}	Input Low to HIGH	FO = 16		4.6		5.3		6.0		7.0		9.8	ns
		FO = 128		4.6		5.3		6.0		7.0		9.8	
t_{CKL}	Input High to LOW	FO = 16		4.8		5.6		6.3		7.4		10.4	ns
		FO = 128		4.8		5.6		6.3		7.4		10.4	
t_{PWH}	Minimum Pulse Width HIGH	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.1		3.6		5.1		
t_{PWL}	Minimum Pulse Width LOW	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.01		3.6		5.1		
t_{CKSW}	Maximum Skew	FO = 16		0.4		0.5		0.5		0.6		0.8	ns
		FO = 128		0.5		0.6		0.7		0.8		1.2	
t_P	Minimum Period	FO = 16	4.7		5.4		6.1		7.2		10.0		ns
		FO = 128	4.8		5.6		6.3		7.5		10.4		
f_{MAX}	Maximum Frequency	FO = 16		188		175		160		139		83	MHz
		FO = 128		181		168		154		134		80	

Table 37 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t_A	Flip-Flop Clock Input Period	6.8		7.8		8.9		10.4		14.6		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		109		101		92		80		48	MHz
Input Module Propagation Delays												
t_{INYH}	Pad-to-Y HIGH		1.0		1.1		1.3		1.5		2.1	ns
t_{INYL}	Pad-to-Y LOW		0.9		1.0		1.1		1.3		1.9	ns

Table 38 • **A42MX09 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		2.5		2.7		3.1		3.6		5.1	ns
t_{DHL}	Data-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t_{ENZH}	Enable Pad Z to HIGH		2.6		2.9		3.3		3.9		5.5	ns
t_{ENZL}	Enable Pad Z to LOW		2.9		3.2		3.7		4.3		6.1	ns
t_{ENHZ}	Enable Pad HIGH to Z		4.9		5.4		6.2		7.3		10.2	ns
t_{ENLZ}	Enable Pad LOW to Z		5.3		5.9		6.7		7.9		11.1	ns
t_{GLH}	G-to-Pad HIGH		2.6		2.9		3.3		3.8		5.3	ns
t_{GHL}	G-to-Pad LOW		2.6		2.9		3.3		3.8		5.3	ns
t_{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.2		5.8		6.6		7.7		10.8	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.4		8.2		9.3		10.9		15.3	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.04		0.04		0.04		0.05		0.07	ns/pF

Table 43 • **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			2.6		2.9		3.2		3.8		5.3	ns
t_{IRD2}	FO = 2 Routing Delay			2.9		3.2		3.6		4.3		6.0	ns
t_{IRD3}	FO = 3 Routing Delay			3.2		3.6		4.0		4.8		6.6	ns
t_{IRD4}	FO = 4 Routing Delay			3.5		3.9		4.4		5.2		7.3	ns
t_{IRD8}	FO = 8 Routing Delay			4.8		5.3		6.1		7.1		10.0	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		4.4		4.8		5.5		6.5		9.1	ns
		FO = 486		4.8		5.3		6.0		7.1		10.0	ns
t_{CKL}	Input HIGH to LOW	FO = 32		5.1		5.7		6.4		7.6		10.6	ns
		FO = 486		6.0		6.6		7.5		8.8		12.4	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	3.0		3.3		3.8		4.5		6.3		ns
		FO = 486	3.3		3.7		4.2		4.9		6.9		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	3.0		3.4		3.8		4.5		6.3		ns
		FO = 486	3.3		3.7		4.2		4.9		6.9		ns
t_{CKSW}	Maximum Skew	FO = 32		0.8		0.8		1.0		1.1		1.6	ns
		FO = 486		0.8		0.8		1.0		1.1		1.6	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 486	0.0		0.0		0.0		0.0		0.0		ns
TTL Output Module Timing[5]													
t_{DLH}	Data-to-Pad HIGH			3.4		3.8		4.3		5.0		7.1	ns
t_{DHL}	Data-to-Pad LOW			4.0		4.4		5.0		5.9		8.3	ns
t_{ENZH}	Enable Pad Z to HIGH			3.6		4.0		4.5		5.3		7.4	ns
t_{ENZL}	Enable Pad Z to LOW			3.9		4.4		5.0		5.8		8.2	ns
t_{ENHZ}	Enable Pad HIGH to Z			7.2		8.0		9.1		10.7		14.9	ns
t_{ENLZ}	Enable Pad LOW to Z			6.7		7.5		8.5		9.9		13.9	ns
t_{GLH}	G-to-Pad HIGH			4.8		5.3		6.0		7.2		10.0	ns
t_{GHL}	G-to-Pad LOW			4.8		5.3		6.0		7.2		10.0	ns
t_{LSU}	I/O Latch Output Set-Up		0.7		0.7		0.8		1.0		1.4		ns

Table 45 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
Parameter / Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations (continued)												
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Set-Up	0.9		1.0		1.1		1.3		1.8		ns
t_{RENH}	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t_{WENSU}	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Set-Up	3.9		4.3		4.9		5.7		8.0		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations												
t_{RPD}	Asynchronous Access Time		11.3		12.6		14.3		16.8		23.5	ns
t_{RDADV}	Read Address Valid	12.3		13.7		15.5		18.2		25.5		ns
t_{ADSU}	Address/Data Set-Up Time	2.3		2.5		2.8		3.4		4.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RENSUA}	Read Enable Set-Up to Address Valid	0.9		1.0		1.1		1.3		1.8		ns
t_{RENHA}	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t_{WENSU}	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.8		2.0		2.1		2.5		3.5	ns
Input Module Propagation Delays												
t_{INPY}	Input Data Pad-to-Y		1.4		1.6		1.8		2.1		3.0	ns
t_{INGO}	Input Latch Gate-to-Output		2.0		2.2		2.5		2.9		4.1	ns
t_{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t_{ILA}	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

Table 53 • **PQ208**

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
21	I/O	I/O	I/O
22	GND	GND	GND
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	GND	GND	GND
28	VCCI	VCCI	VCCI
29	VCCA	VCCA	VCCA
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	VCCA	VCCA	VCCA
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	NC	I/O	I/O
42	NC	I/O	I/O
43	NC	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	NC	I/O	I/O
52	GND	GND	GND
53	GND	GND	GND
54	I/O	TMS, I/O	TMS, I/O
55	I/O	TDI, I/O	TDI, I/O
56	I/O	I/O	I/O
57	I/O	WD, I/O	WD, I/O

Table 53 • **PQ208**

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
58	I/O	WD, I/O	WD, I/O
59	I/O	I/O	I/O
60	VCCI	VCCI	VCCI
61	NC	I/O	I/O
62	NC	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	QCLKA, I/O
66	I/O	WD, I/O	WD, I/O
67	NC	WD, I/O	WD, I/O
68	NC	I/O	I/O
69	I/O	I/O	I/O
70	I/O	WD, I/O	WD, I/O
71	I/O	WD, I/O	WD, I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	GND	GND	GND
79	VCCA	VCCA	VCCA
80	NC	VCCI	VCCI
81	I/O	I/O	I/O
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	WD, I/O	WD, I/O
86	I/O	WD, I/O	WD, I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	NC	I/O	I/O
90	NC	I/O	I/O
91	I/O	I/O	QCLKB, I/O
92	I/O	I/O	I/O
93	I/O	WD, I/O	WD, I/O
94	I/O	WD, I/O	WD, I/O

Table 54 • **PQ240**

PQ240	
Pin Number	**A42MX36 Function**
52	VCCI
53	I/O
54	WD, I/O
55	WD, I/O
56	I/O
57	SDI, I/O
58	I/O
59	VCCA
60	GND
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	VCCI
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	VCCA
86	I/O
87	I/O
88	VCCA

Figure 47 • **VQ100**

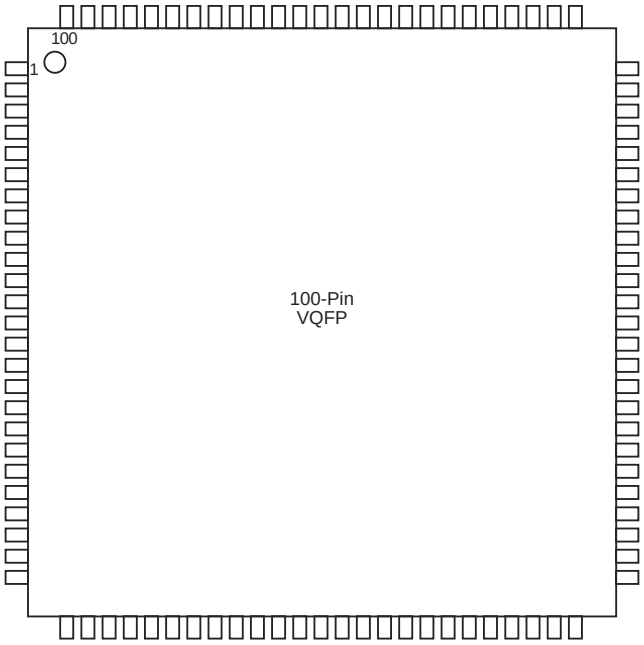


Table 56 • **VQ100**

VQ100		
Pin Number	**A42MX09 Function**	**A42MX16 Function**
1	I/O	I/O
2	MODE	MODE
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	GND
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	VCCA	NC
15	VCCI	VCCI
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	GND	GND

Table 56 • **VQ100**

VQ100		
Pin Number	**A42MX09 Function**	**A42MX16 Function**
93	I/O	I/O
94	GND	GND
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	DCLK, I/O	DCLK, I/O

Figure 48 • **TQ176**

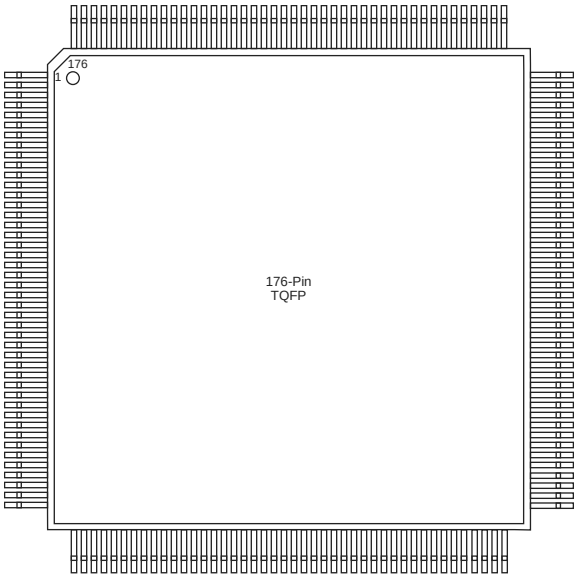


Table 57 • **TQ176**

TQ176			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
1	GND	GND	GND
2	MODE	MODE	MODE
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	NC	NC	I/O
9	I/O	I/O	I/O

Table 58 • **CQ208**

CQ208	
Pin Number	**A42MX36 Function**
74	I/O
75	I/O
76	I/O
77	I/O
78	GND
79	VCCA
80	VCCI
81	I/O
82	I/O
83	I/O
84	I/O
85	WD, I/O
86	WD, I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	QCLKB, I/O
92	I/O
93	WD, I/O
94	WD, I/O
95	I/O
96	I/O
97	I/O
98	VCCI
99	I/O
100	WD, I/O
101	WD, I/O
102	I/O
103	TDO, I/O
104	I/O
105	GND
106	VCCA
107	I/O
108	I/O
109	I/O
110	I/O

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
M10	GND
M11	GND
M12	GND
M17	I/O
M18	I/O
M19	I/O
M20	I/O
N1	I/O
N2	I/O
N3	I/O
N4	VCCI
N17	VCCI
N18	I/O
N19	I/O
N20	I/O
P1	I/O
P2	I/O
P3	I/O
P4	VCCA
P17	I/O
P18	I/O
P19	I/O
P20	I/O
R1	I/O
R2	I/O
R3	I/O
R4	VCCI
R17	VCCI
R18	I/O
R19	I/O
R20	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T17	VCCA
T18	I/O

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
T19	I/O
T20	I/O
U1	I/O
U2	I/O
U3	I/O
U4	I/O
U5	VCCI
U6	WD, I/O
U7	I/O
U8	I/O
U9	WD, I/O
U10	VCCA
U11	VCCI
U12	I/O
U13	I/O
U14	QCLKB, I/O
U15	I/O
U16	VCCI
U17	I/O
U18	GND
U19	I/O
U20	I/O
V1	I/O
V2	I/O
V3	GND
V4	GND
V5	I/O
V6	I/O
V7	I/O
V8	WD, I/O
V9	I/O
V10	I/O
V11	I/O
V12	I/O
V13	WD, I/O
V14	I/O
V15	WD, I/O

Figure 53 • **CQ172**

Table 62 • **CQ172**

CQ172	
Pin Number	**A42MX16 Function**
1	MODE
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	GND
8	I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	I/O
17	GND
18	I/O
19	I/O
20	I/O

Table 62 • **CQ172**

60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	GND
66	VCC
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	GND
76	I/O
77	I/O
78	I/O
79	I/O
80	VCCI
81	I/O
82	I/O
83	I/O
84	I/O
85	SDO
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	GND