Microchip Technology - A42MX36-2PQG208 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	2560
Number of I/O	176
Number of Gates	54000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx36-2pqg208

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2.6 Temperature Grade Offerings

Table 4 • **Temperature Grade Offerings**

Package	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PLCC 44	C, I, M	C, I, M				
PLCC 68	C, I, A, M	C, I, M				
PLCC 84		C, I, A, M	C, I, A, M	C, I, M	C, I, M	
PQFP 100	C, I, A, M	C, I, A, M	C, I, A, M	C, I, M		
PQFP 144			C			
PQFP 160			C, I, A, M	C, I, M	C, I, A, M	
PQFP 208				C, I, A, M	C, I, A, M	C, I, A, M
PQFP 240						C, I, A, M
VQFP 80	C, I, A, M	C, I, A, M				
VQFP 100			C, I, A, M	C, I, A, M		
TQFP 176			C, I, A, M	C, I, A, M	C, I, A, M	
PBGA 272						C, I, M
CQFP 172				C, M, B		
CQFP 208						C, M, B
CQFP 256						C, M, B
CPGA 132			C, M, B			

Note: C = Commercial
I = Industrial
A = Automotive
M = Military
B = MIL-STD-883 Class B

2.7 Speed Grade Offerings

Table 5 • **Speed Grade Offerings**

	– F	Std	–1	–2	–3
C	P	P	P	P	P
I		P	P	P	P
A		P			
M		P	P		
B		P	P		

Note: See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local *Microsemi Sales representative* for device availability.

3. All outputs unloaded. All inputs = VCC/VCCI or GND

3.8 3.3 V Operating Conditions

The following table shows 3.3 V operating conditions.

Table 16 • **Absolute Maximum Ratings for 40MX Devices***

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCC + 0.5	V
VO	Output Voltage	–0.5 to VCC + 0.5	V
t_{STG}	Storage Temperature	–65 to + 150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 17 • **Absolute Maximum Ratings for 42MX Devices***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCCI+0.5	V
VO	Output Voltage	–0.5 to VCCI+0.5	V
t_{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 18 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCA (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCI (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

All the following tables show various specifications and operating conditions of 40MX and 42MX FPGAs.

reliability. Devices should not be operated outside the recommended operating conditions.

Table 21 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCCA	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI	3.14 to 3.47	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

3.9.3 Output Drive Characteristics for 3.3 V PCI Signaling

***Table 25* • DC Specification (3.3 V PCI Signaling)[1]**

			PCI		MX		
Symbol	**Parameter**	**Condition**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
VCCI	Supply Voltage for I/Os		3.0	3.6	3.0	3.6[2]	V
VIH	Input High Voltage		0.5	VCC + 0.5	0.5	VCCI + 0.3	V
VIL	Input Low Voltage		–0.5	0.8	–0.3	0.8	V
IIH	Input High Leakage Current	VIN = 2.7 V		70		10	µA
IIL	Input Leakage Current			–70		–10	µA
VOH	Output High Voltage	IOUT = –2 mA	0.9		3.3		V
VOL	Output Low Voltage	IOUT = 3 mA, 6 mA		0.1		0.1 VCCI	V
C_{IN}	Input Pin Capacitance			10		10	pF
C_{CLK}	CLK Pin Capacitance		5	12		10	pF
L_{PIN}	Pin Inductance			20		< 8 nH[3]	nH

1. PCI Local Bus Specification, Version 2.1, Section 4.2.2.1.
2. Maximum rating for VCCI –0.5 V to 7.0V.
3. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

Table 26* • AC Specifications for (3.3 V PCI Signaling)

			PCI		MX		
Symbol	**Parameter**	**Condition**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
ICL	Low Clamp Current	–5 < VIN ≤ –1	–25 + (VIN +1) /0.015		–60	–10	mA
Slew (r)	Output Rise Slew Rate	0.2 V to 0.6 V load	1	4	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	0.6 V to 0.2 V load	1	4	2.8	4.0	V/ns

Note: *PCI Local Bus Specification, Version 2.1, Section 4.2.2.2.

A sample calculation of the absolute maximum power dissipation allowed for a TQ176 package at commercial temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max}\cdot\text{junction temp}\cdot(°\text{C}) - \text{Max}\cdot\text{ambient temp}\cdot(°\text{C})}{\theta_{ja}(°\text{C}/\text{W}))} = \frac{150°\text{C} - 70°\text{C}}{(28°\text{C})/\text{W}} = 2.86\text{W}$$

EQ 5

The maximum power dissipation for military-grade devices is a function of θ_{jc}. A sample calculation of the absolute maximum power dissipation allowed for CQFP 208-pin package at military temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max}\cdot\text{junction temp}\cdot(°\text{C}) - \text{Max}\cdot\text{ambient temp}\cdot(°\text{C})}{\theta_{jc}(°\text{C}/\text{W}))} = \frac{150°\text{C} - 125°\text{C}}{(6.3°\text{C})/\text{W}} = 3.97\text{W}$$

EQ 6

Table 27 • **Package Thermal Characteristics**

			θ_{ja}			
Plastic Packages	**Pin Count**	θ_{jc}	**Still Air**	**1.0 m/s 200 ft/min.**	**2.5 m/s 500 ft/min.**	**Units**
Plastic Quad Flat Pack	100	12.0	27.8	23.4	21.2	°C/W
Plastic Quad Flat Pack	144	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	160	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	208	8.0	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack	240	8.5	25.6	22.3	20.8	°C/W
Plastic Leaded Chip Carrier	44	16.0	20.0	24.5	22.0	°C/W
Plastic Leaded Chip Carrier	68	13.0	25.0	21.0	19.4	°C/W
Plastic Leaded Chip Carrier	84	12.0	22.5	18.9	17.6	°C/W
Thin Plastic Quad Flat Pack	176	11.0	24.7	19.9	18.0	°C/W
Very Thin Plastic Quad Flat Pack	80	12.0	38.2	31.9	29.4	°C/W
Very Thin Plastic Quad Flat Pack	100	10.0	35.3	29.4	27.1	°C/W
Plastic Ball Grid Array	272	3.0	18.3	14.9	13.9	°C/W
Ceramic Packages						
Ceramic Pin Grid Array	132	4.8	25.0	20.6	18.7	°C/W
Ceramic Quad Flat Pack	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack	256	2.0	20.0	16.5	15.0	°C/W

Table 34 • **A40MX02 Timing Characteristics (Nominal 5.0 V Operation)** ***(continued)***
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

			–3 Speed		**–2 Speed**		**–1 Speed**		**Std Speed**		**–F Speed**		
Parameter / Description			**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			0.7		0.8		0.9		1.1		1.5	ns
t_{INYL}	Pad-to-Y LOW			0.6		0.7		0.8		1.0		1.3	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO = 1 Routing Delay			2.1		2.4		2.2		3.2		4.5	ns
t_{IRD2}	FO = 2 Routing Delay			2.6		3.0		3.4		4.0		5.6	ns
t_{IRD3}	FO = 3 Routing Delay			3.1		3.6		4.1		4.8		6.7	ns
t_{IRD4}	FO = 4 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t_{IRD8}	FO = 8 Routing Delay			5.7		6.6		7.5		8.8		12.4	ns
Global Clock Network													
t_{CKH}	Input Low to HIGH	FO = 16 FO = 128		4.6 4.6		5.3 5.3		6.0 6.0		7.0 7.0		9.8 9.8	ns
t_{CKL}	Input High to LOW	FO = 16 FO = 128		4.8 4.8		5.6 5.6		6.3 6.3		7.4 7.4		10.4 10.4	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 16 FO = 128	2.2 2.4		2.6 2.7		2.9 3.1		3.4 3.6		4.8 5.1		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 16 FO = 128	2.2 2.4		2.6 2.7		2.9 3.01		3.4 3.6		4.8 5.1		ns
t_{CKSW}	Maximum Skew	FO = 16 FO = 128		0.4 0.5		0.5 0.6		0.5 0.7		0.6 0.8		0.8 1.2	ns
t_P	Minimum Period	FO = 16 FO = 128	4.7 4.8		5.4 5.6		6.1 6.3		7.2 7.5		10.0 10.4		ns
f_{MAX}	Maximum Frequency	FO = 16 FO = 128		188 181		175 168		160 154		139 134		83 80	MHz

Table 34 • **A40MX02 Timing Characteristics (Nominal 5.0 V Operation) *(continued)***
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad HIGH		3.3		3.8		4.3		5.1		7.2	ns
t_{DHL}	Data-to-Pad LOW		4.0		4.6		5.2		6.1		8.6	ns
t_{ENZH}	Enable Pad Z to HIGH		3.7		4.3		4.9		5.8		8.0	ns
t_{ENZL}	Enable Pad Z to LOW		4.7		5.4		6.1		7.2		10.1	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.1	ns
t_{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing[4]												
t_{DLH}	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t_{DHL}	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZH}	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZL}	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t_{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35pF loading

Table 35 • **A40MX02 Timing Characteristics (Nominal 3.3 V Operation)**
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays												
t_{PD1}	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t_{PD2}	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t_{CO}	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t_{GO}	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays[1]												

Table 37 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t_A	Flip-Flop Clock Input Period	6.8		7.8		8.9		10.4		14.6		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		109		101		92		80		48	MHz
Input Module Propagation Delays												
t_{INYH}	Pad-to-Y HIGH		1.0		1.1		1.3		1.5		2.1	ns
t_{INYL}	Pad-to-Y LOW		0.9		1.0		1.1		1.3		1.9	ns

Table 37 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation)** ***(continued)*****(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Predicted Routing Delays1													
t_{IRD1}	FO = 1 Routing Delay			2.9		3.3		3.8		4.5		6.3	ns
t_{IRD2}	FO = 2 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t_{IRD3}	FO = 3 Routing Delay			4.4		5.0		5.7		6.7		9.4	ns
t_{IRD4}	FO = 4 Routing Delay			5.1		5.9		6.7		7.8		11.0	ns
t_{IRD8}	FO = 8 Routing Delay			8.0		9.3		10.5		12.4		17.2	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 16		6.4		7.4		8.4		9.9		13.8	ns
		FO = 128		6.4		7.4		8.4		9.9		13.8	
t_{CKL}	Input HIGH to LOW	FO = 16		6.8		7.8		8.9		10.4		14.6	ns
		FO = 128		6.8		7.8		8.9		10.4		14.6	
t_{PWH}	Minimum Pulse Width HIGH	FO = 16	3.1		3.6		4.1		4.8		6.7		ns
		FO = 128	3.3		3.8		4.3		5.1		7.1		
t_{PWL}	Minimum Pulse Width LOW	FO = 16	3.1		3.6		4.1		4.8		6.7		ns
		FO = 128	3.3		3.8		4.3		5.1		7.1		
t_{CKSW}	Maximum Skew	FO = 16		0.6		0.6		0.7		0.8		1.2	ns
		FO = 128		0.8		0.9		1.0		1.2		1.6	
t_P	Minimum Period	FO = 16	6.5		7.5		8.5		10.1		14.1		ns
		FO = 128	6.8		7.8		8.9		10.4		14.6		
f_{MAX}	Maximum Frequency	FO = 16		113		105		96		83		50	MHz
		FO = 128		109		101		92		80		48	
TTL Output Module Timing[4]													
t_{DLH}	Data-to-Pad HIGH			4.7		5.4		6.1		7.2		10.0	ns
t_{DHL}	Data-to-Pad LOW			5.6		6.4		7.3		8.6		12.0	ns
t_{ENZH}	Enable Pad Z to HIGH			5.2		6.0		6.9		8.1		11.3	ns
t_{ENZL}	Enable Pad Z to LOW			6.6		7.6		8.6		10.1		14.1	ns
t_{ENHZ}	Enable Pad HIGH to Z			11.1		12.8		14.5		17.1		23.9	ns
t_{ENLZ}	Enable Pad LOW to Z			8.2		9.5		10.7		12.6		17.7	ns
d_{TLH}	Delta LOW to HIGH			0.03		0.03		0.04		0.04		0.06	ns/pF
d_{THL}	Delta HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.9		12.1		13.7		16.1		22.5	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.10		0.11		0.12		0.14		0.20	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.10		0.11		0.12		0.14		0.20	ns/pF
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		4.9		5.5		6.2		7.3		10.3	ns
t_{DHL}	Data-to-Pad LOW		3.4		3.8		4.3		5.1		7.1	ns
t_{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.7		5.5		7.7	ns
t_{ENZL}	Enable Pad Z to LOW		4.1		4.6		5.2		6.1		8.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.4		8.2		9.3		10.9		15.3	ns
t_{ENLZ}	Enable Pad LOW to Z		6.9		7.6		8.7		10.2		14.3	ns
t_{GLH}	G-to-Pad HIGH		7.0		7.8		8.9		10.4		14.6	ns
t_{GHL}	G-to-Pad LOW		7.0		7.8		8.9		10.4		14.6	ns
t_{LSU}	I/O Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.9		8.8		10.0		11.8		16.5	ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. Delays based on 35 pF loading.

3.12 Pin Descriptions

This section lists the pin descriptions for 40MX and 42MX series FPGAs.

CLK/A/B, I/O Global Clock

Clock inputs for clock distribution networks. CLK is for 40MX while CLKA and CLKB are for 42MX devices. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK, I/ODiagnostic Clock

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND, Ground

Input LOW supply voltage.

I/O, Input/Output

Input, output, tristate or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/Os pins are configured by the Designer software as shown in Table 46, page 84.

Table 46 • **Configuration of Unused I/Os**

Device	Configuration
A40MX02, A40MX04	Pulled LOW
A42MX09, A42MX16	Pulled LOW
A42MX24, A42MX36	Tristated

In all cases, it is recommended to tie all unused MX I/O pins to LOW on the board. This applies to all dual-purpose pins when configured as I/Os as well.

LP, Low Power Mode

Controls the low power mode of all 42MX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation in 200 µs after the LP pin is driven to a logic LOW.

MODE, Mode

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). The MODE pin is held HIGH to provide verification capability. The MODE pin should be terminated to GND through a 10kΩ resistor so that the MODE pin can be pulled HIGH when required.

NC, No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O

PRB, I/OProbe A/B

The Probe pin is used to output data from any user-defined design node within the device. Each diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. The Probe pin is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

QCLKA/B/C/D, I/O Quadrant Clock

Quadrant clock inputs for A42MX36 devices. When not used as a register control signal, these pins can function as user I/Os.

SDI, I/OSerial Data Input

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDO, I/OSerial Data Output

Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. SDO is available for 42MX devices only.

When Silicon Explorer II is being used, SDO will act as an output while the "checksum" command is run. It will return to user I/O when "checksum" is complete.

TCK, I/O Test Clock

Table 50 • **PQ 100**

PQ100				
Pin Number	**A40MX02 Function**	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**
93	VCC	VCC	I/O	I/O
94	VCC	VCC	PRB, I/O	PRB, I/O
95	NC	I/O	I/O	I/O
96	NC	I/O	GND	GND
97	NC	I/O	I/O	I/O
98	SDI, I/O	SDI, I/O	I/O	I/O
99	DCLK, I/O	DCLK, I/O	I/O	I/O
100	PRA, I/O	PRA, I/O	I/O	I/O

Figure 42 • **PQ144**

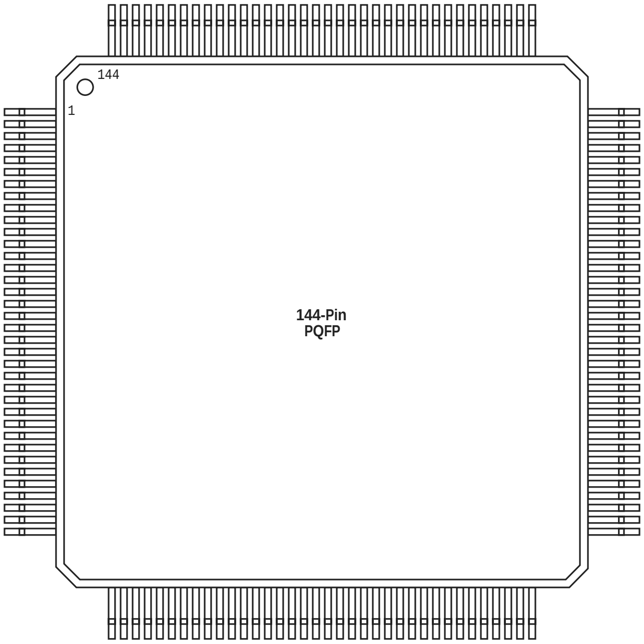

Table 51 • **PQ144**

PQ144	
Pin Number	**A42MX09 Function**
1	I/O
2	MODE
3	I/O
4	I/O
5	I/O

Table 52 • **PQ160**

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
21	CLKA, I/O	CLKA, I/O	CLKA, I/O
22	I/O	I/O	I/O
23	PRA, I/O	PRA, I/O	PRA, I/O
24	NC	I/O	WD, I/O
25	I/O	I/O	WD, I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	NC	I/O	I/O
29	I/O	I/O	WD, I/O
30	GND	GND	GND
31	NC	I/O	WD, I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	VCCI	VCCI
36	I/O	I/O	WD, I/O
37	I/O	I/O	WD, I/O
38	SDI, I/O	SDI, I/O	SDI, I/O
39	I/O	I/O	I/O
40	GND	GND	GND
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	GND	GND	GND
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	NC	I/O	I/O
53	I/O	I/O	I/O
54	NC	VCCA	VCCA
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	VCCA	VCCA	VCCA

Table 52 • **PQ160**

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
58	VCCI	VCCI	VCCI
59	GND	GND	GND
60	VCCA	VCCA	VCCA
61	LP	LP	LP
62	I/O	I/O	TCK, I/O
63	I/O	I/O	I/O
64	GND	GND	GND
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	I/O	I/O	I/O
69	GND	GND	GND
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	I/O	I/O	I/O
77	NC	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	GND	GND	GND
81	I/O	I/O	I/O
82	SDO, I/O	SDO, I/O	SDO, TDO, I/O
83	I/O	I/O	WD, I/O
84	I/O	I/O	WD, I/O
85	I/O	I/O	I/O
86	NC	VCCI	VCCI
87	I/O	I/O	I/O
88	I/O	I/O	WD, I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O

Table 52 • **PQ160**

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	VCCA	VCCA
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	VCCA	VCCA
139	VCCI	VCCI	VCCI
140	GND	GND	GND
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	GND	GND	GND
146	NC	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	NC	VCCA	VCCA
151	NC	I/O	I/O
152	NC	I/O	I/O
153	NC	I/O	I/O
154	NC	I/O	I/O
155	GND	GND	GND
156	I/O	I/O	I/O
157	I/O	I/O	I/O
158	I/O	I/O	I/O
159	MODE	MODE	MODE
160	GND	GND	GND

Table 53 • **PQ208**

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
95	NC	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	VCCI	VCCI	VCCI
99	I/O	I/O	I/O
100	I/O	WD, I/O	WD, I/O
101	I/O	WD, I/O	WD, I/O
102	I/O	I/O	I/O
103	SDO, I/O	SDO, TDO, I/O	SDO, TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	VCCA	VCCA
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	NC	I/O	I/O
113	NC	I/O	I/O
114	NC	I/O	I/O
115	NC	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	I/O	I/O	I/O
126	GND	GND	GND
127	I/O	I/O	I/O
128	I/O	TCK, I/O	TCK, I/O
129	LP	LP	LP
130	VCCA	VCCA	VCCA
131	GND	GND	GND

Table 54 • **PQ240**

PQ240	
Pin Number	**A42MX36 Function**
15	QCLKC, I/O
16	I/O
17	WD, I/O
18	WD, I/O
19	I/O
20	I/O
21	WD, I/O
22	WD, I/O
23	I/O
24	PRB, I/O
25	I/O
26	CLKB, I/O
27	I/O
28	GND
29	VCCA
30	VCCI
31	I/O
32	CLKA, I/O
33	I/O
34	PRA, I/O
35	I/O
36	I/O
37	WD, I/O
38	WD, I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	QCLKD, I/O
46	I/O
47	WD, I/O
48	WD, I/O
49	I/O
50	I/O
51	I/O

Table 55 • **VQ80**

VQ80		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
49	I/O	I/O
50	CLK, I/O	CLK, I/O
51	I/O	I/O
52	MODE	MODE
53	VCC	VCC
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	GND	GND
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	VCC	**VCC**
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
59	I/O
60	VCCA
61	GND
62	GND
63	NC
64	NC
65	NC
66	I/O
67	SDO, TDO, I/O
68	I/O
69	WD, I/O
70	WD, I/O
71	I/O
72	VCCI
73	I/O
74	I/O
75	I/O
76	WD, I/O
77	GND
78	WD, I/O
79	I/O
80	QCLKB, I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	WD, I/O
88	WD, I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	VCCI